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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ V_S = ±15.0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.2	0.5	mV
		−40°C ≤ T_A ≤ +85°C			1	mV
Input Bias Current	I_B	V_{CM} = 0 V		150	600	nA
		V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C		150	700	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		10	100	nA
		V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C		10	150	nA
Common-Mode Rejection	CMR	V_{CM} = ±12 V	80	90		dB
	CMR	V_{CM} = ±12 V, −40°C ≤ T_A ≤ +85°C	80	88		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	83	86		dB
		R_L = 2 kΩ, −40°C ≤ T_A ≤ +85°C	77.5			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			0.2		pA/°C
Long-Term Offset Voltage Drift[1]	$\Delta V_{OS}/\Delta T$				750	µV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	±13.0	±13.5		V
		R_L = 2 kΩ, −40°C ≤ T_A ≤ +85°C	±12.9	±13.12		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±4.5 V ≤ V_S ≤ ±18 V	96	120		dB
		−40°C ≤ T_A ≤ +85°C	86	115		dB
Supply Current	I_{SY}	V_O = 0 V		8	10	mA
		V_O = 0 V, −40°C ≤ T_A ≤ +85°C			13	mA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	A_V = +1, C_L = 30 pF		28		MHz
Slew Rate	SR	V_{IN} = 10 V step, R_L = 2 kΩ, C_L = 30 pF				
		A_V = +1	125	170		V/µs
		A_V = −1		350		V/µs
Full-Power Bandwidth	BW_P	V_{IN} = 10 V step		2.7		MHz
Settling Time	t_S	To 0.01%, V_{IN} = 10 V step		200		ns
Phase Margin	θ_0			45		Degrees
Input Capacitance						
Common Mode				2.0		pF
Differential				1.0		pF
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		0.15		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		6		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.8		pA/√Hz

[1] Long-term offset voltage drift is guaranteed by 1000 hrs. Life test performed on three independent wafer lots at 125°C, with an LTPD of 1.3.

@ V_S = ±5.0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.3	0.5	mV
		−40°C ≤ T_A ≤ +85°C			1	mV
Input Bias Current	I_B	V_{CM} = 0 V		125	600	nA
		V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C		150	700	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		20	100	nA
		V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C			150	nA
Common-Mode Rejection	CMR	V_{CM} = ±2.0 V	76	85		dB
	CMR	V_{CM} = ±2.0 V, −40°C ≤ T_A ≤ +85°C	76	80		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	80	83		dB
		R_L = 2 kΩ, −40°C ≤ T_A ≤ +85°C	74			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			0.2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	±3.0	±3.5		V
		R_L = 2 kΩ, −40°C ≤ T_A ≤ +85°C	±3.0	±3.20		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±4.5 V ≤ V_S ≤ ±5.5 V	92	107		dB
		−40°C ≤ T_A ≤ +85°C	83	105		dB
Supply Current	I_{SY}	V_O = 0 V		8	10	mA
		V_O = 0 V, −40°C ≤ T_A ≤ +85°C			12	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	A_V = +1		22		MHz
Slew Rate	SR	V_{IN} = 5 V step, R_L = 2 kΩ, C_L = 39 pF				
		A_V = +1		90		V/µs
		A_V = −1		90		V/µs
Full-Power Bandwidth	BW_P	V_{IN} = 5 V step		2.5		MHz
Settling Time	t_S	To 0.01%, V_{IN} = 5 V step		280		ns
Phase Margin	θ_0			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		0.15		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		7		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.8		pA/√Hz

WAFER TEST LIMITS[1]

@ V_S = ±15.0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Limit	Unit
Offset Voltage	V_{OS}		±0.5	mV max
Input Bias Current	I_B	V_{CM} = 0 V	600	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	100	nA max
Input Voltage Range[2]			±12	V min/max
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V	80	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	96	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	83	dB min
Output Voltage Range	V_O	R_L = 2 kΩ	±13.0	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞	10	mA max

[1] Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult sales to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[2] Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter[1]	Rating
Supply Voltage	±18 V
Input Voltage[2]	±18 V
Differential Input Voltage[2]	±26 V
Output Short-Circuit Duration	Limited
Storage Temperature Range	
14-Lead CERDIP and 20-Terminal LCC	−65°C to +175°C
14-Lead PDIP and 16-Lead SOIC	−65°C to +150°C
Operating Temperature Range	
OP467A	−55°C to +125°C
OP467G	−40°C to +85°C
Junction Temperature Range	
14-Lead CERDIP and 20-Terminal LCC	−65°C to +175°C
14-Lead PDIP and 16-Lead SOIC	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
14-Lead CERDIP (Y)	94	10	°C/W
14-Lead PDIP (P)	76	33	°C/W
16-Lead SOIC (S)	88	23	°C/W
20-Terminal LCC (RC)	78	33	°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device in socket for CERDIP, PDIP, and LCC packages, and θ_{JA} is specified for device soldered in circuit board for the SOIC package.

DICE CHARACTERISTICS

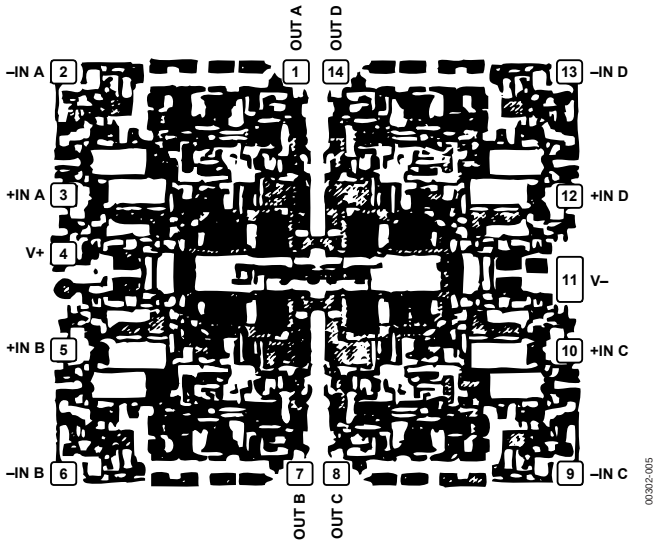


Figure 5. 0.111 Inch × 0.100 Inch DIE Size, 11,100 sq. mils, Substrate Connected to V+, 165 Transistors

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

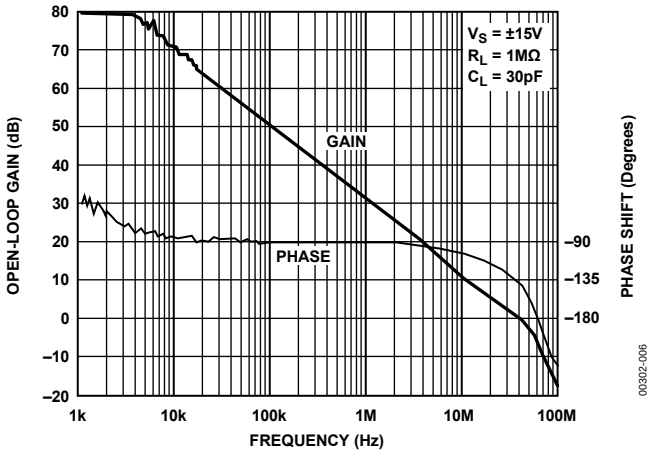


Figure 6. Open-Loop Gain, Phase vs. Frequency

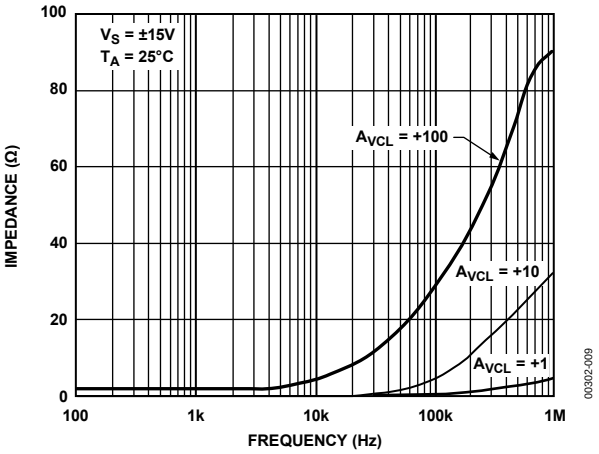


Figure 9. Closed-Loop Output Impedance vs. Frequency

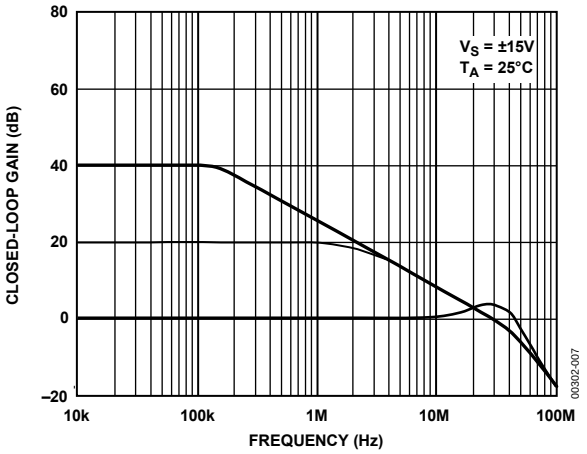


Figure 7. Closed-Loop Gain vs. Frequency

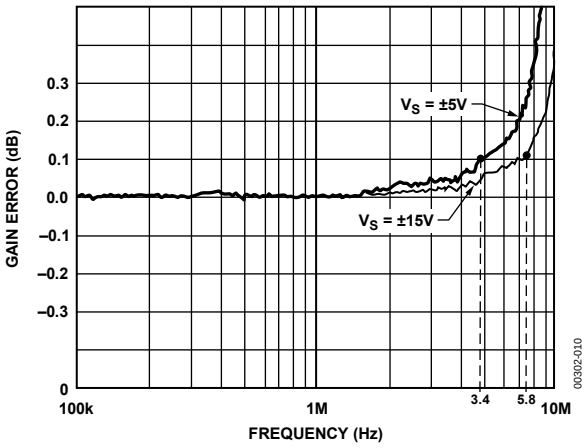


Figure 10. Gain Error vs. Frequency

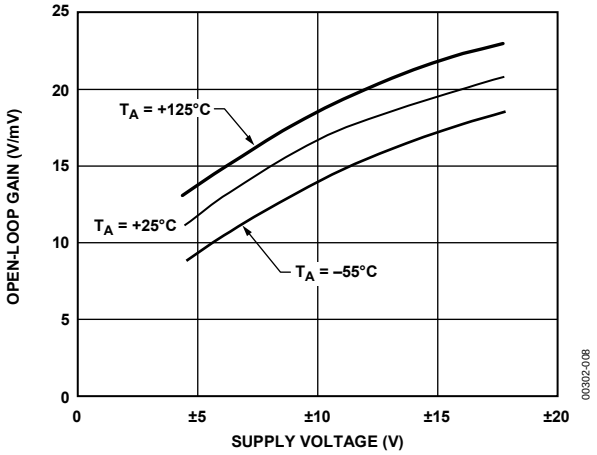


Figure 8. Open-Loop Gain vs. Supply Voltage

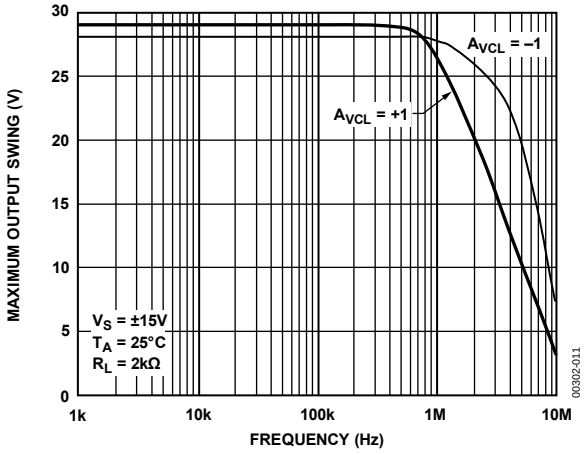


Figure 11. Maximum V_{OUT} Swing vs. Frequency

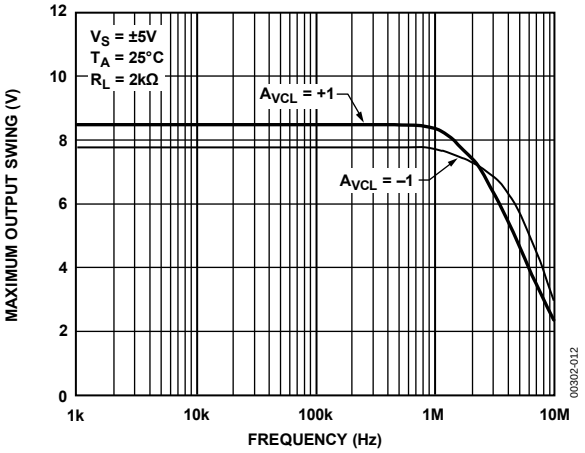


Figure 12. Maximum V_{OUT} Swing vs. Frequency

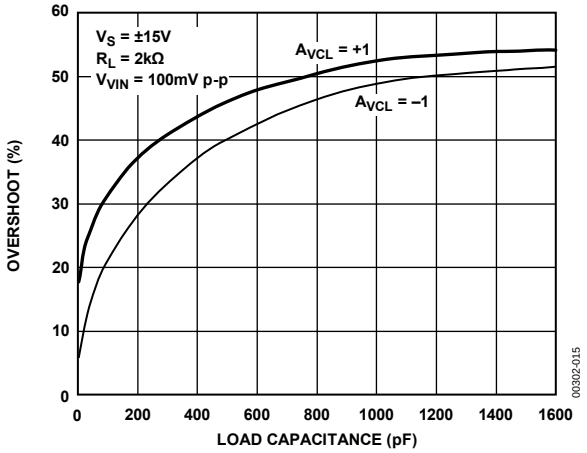


Figure 15. Small Signal Overshoot vs. Load Capacitance

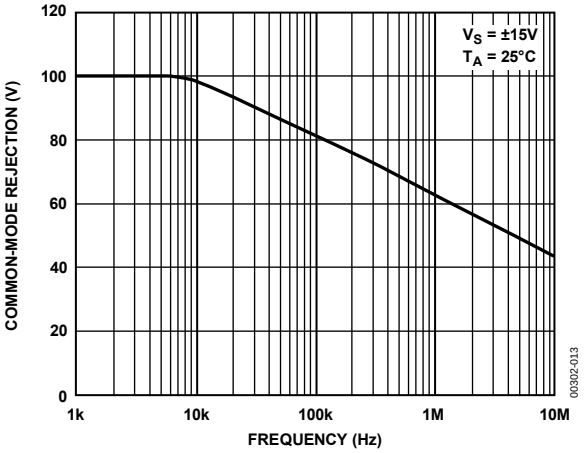


Figure 13. Common-Mode Rejection vs. Frequency

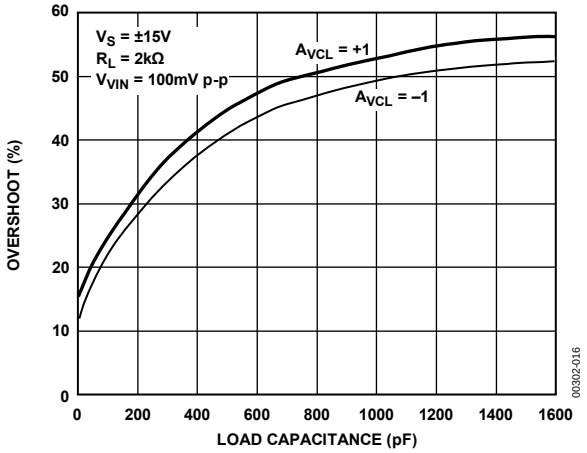


Figure 16. Small Signal Overshoot vs. Load Capacitance

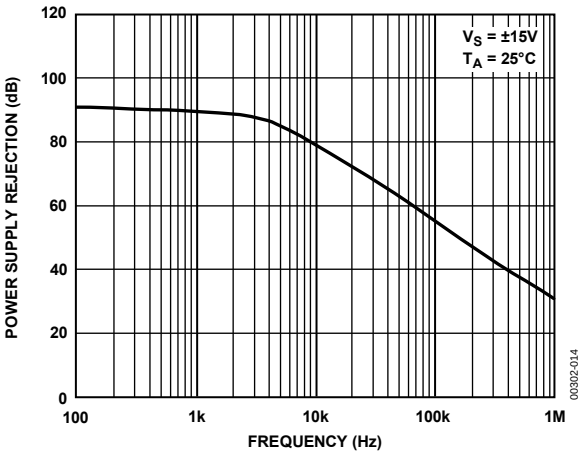


Figure 14. Power-Supply Rejection vs. Frequency

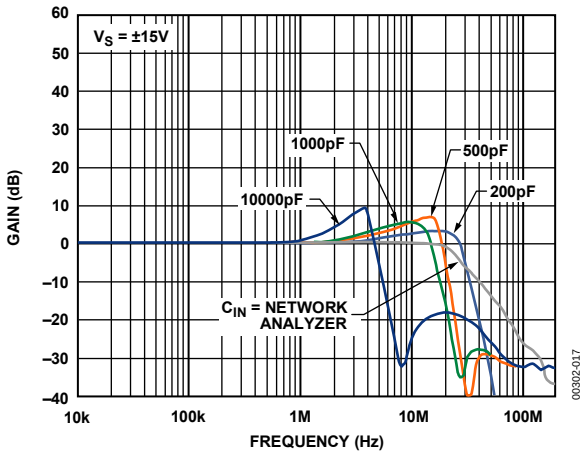


Figure 17. Noninverting Gain vs. Capacitive Loads

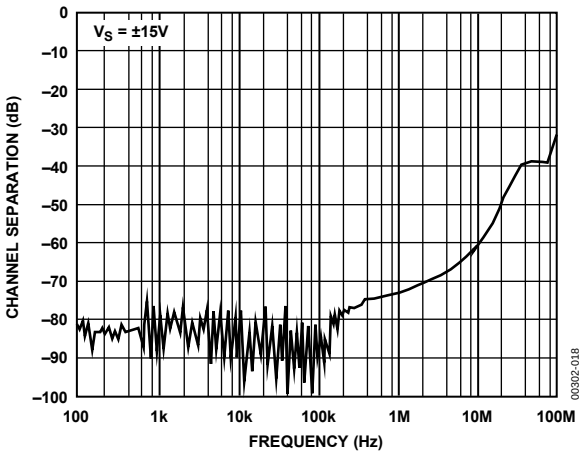


Figure 18. Channel Separation vs. Frequency

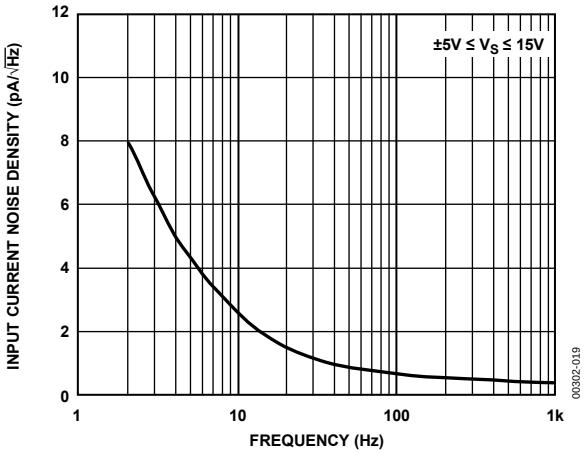


Figure 19. Input Current Noise Density vs. Frequency

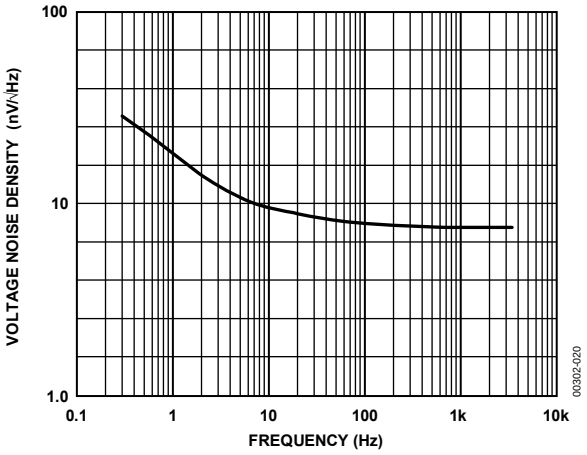


Figure 20. Voltage Noise Density vs. Frequency

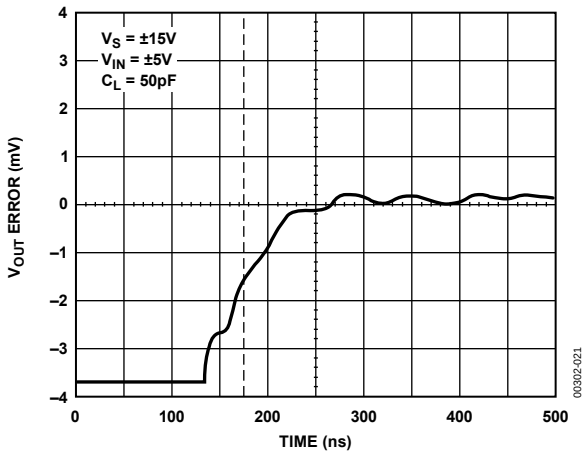


Figure 21. Settling Time, Negative Edge

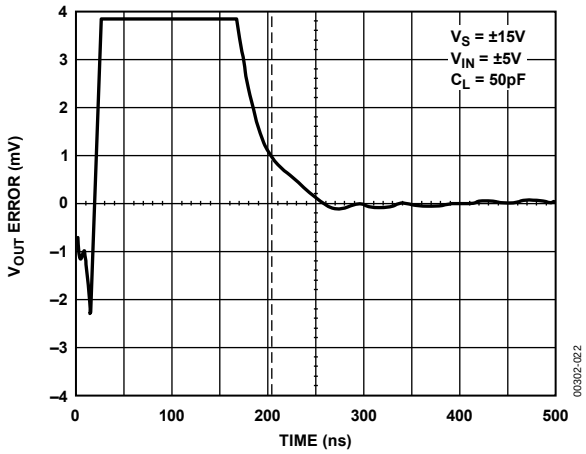


Figure 22. Settling Time, Positive Edge

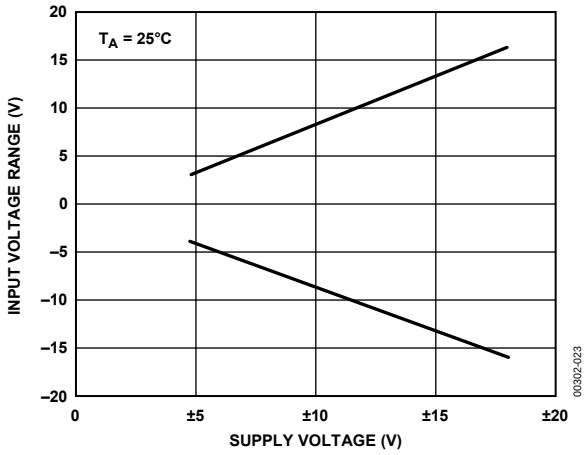


Figure 23. Input Voltage Range vs. Supply Voltage

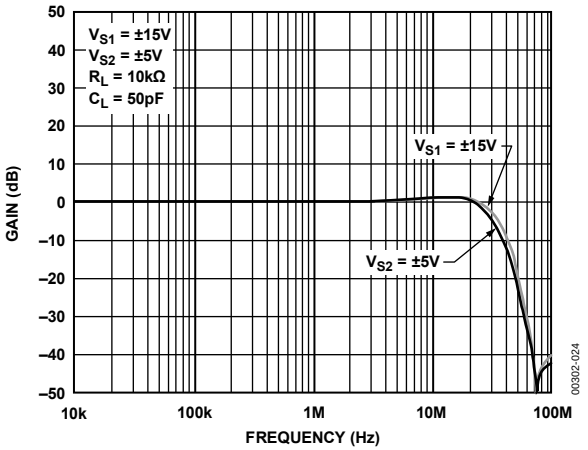


Figure 24. Noninverting Gain vs. Supply Voltage

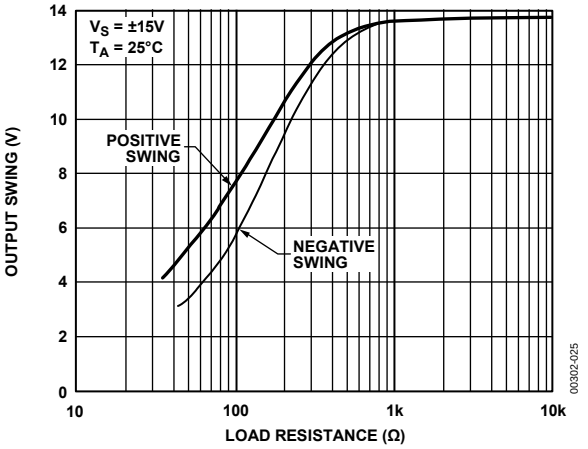


Figure 25. Output Swing vs. Load Resistance

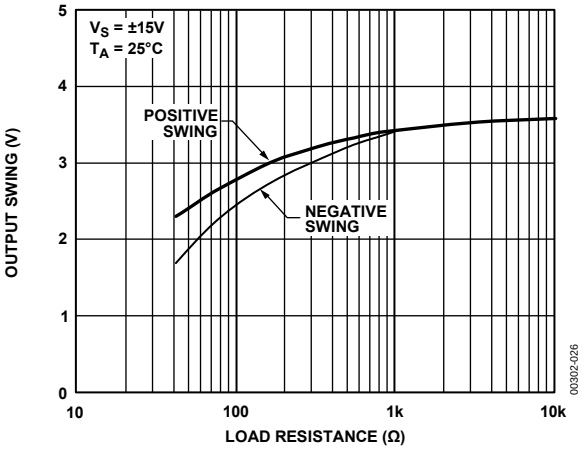


Figure 26. Output Swing vs. Load Resistance

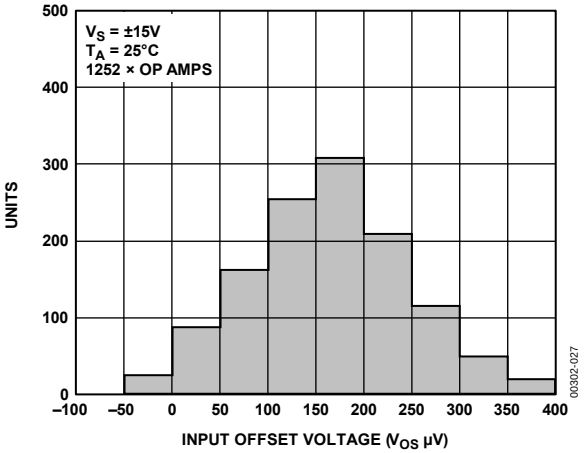


Figure 27. Input Offset Voltage Distribution

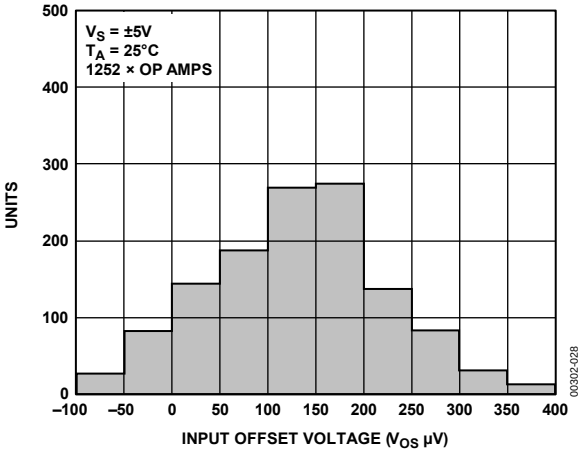


Figure 28. Input Offset Voltage Distribution

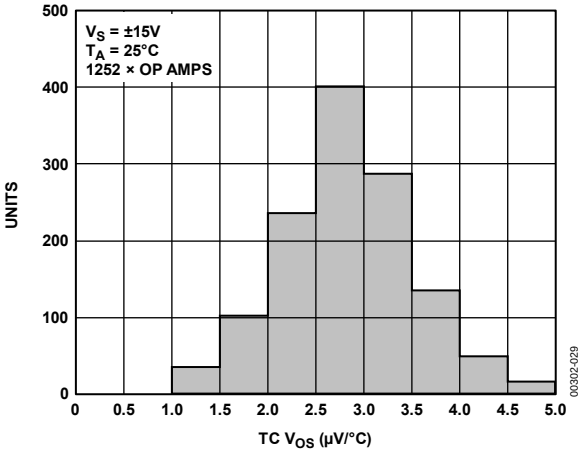


Figure 29. TC V_{OS} Distribution

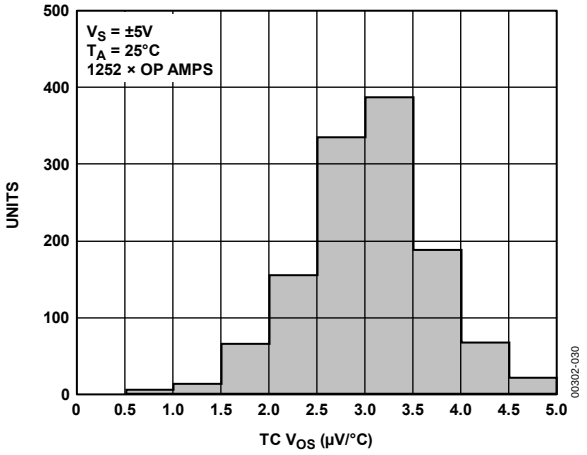


Figure 30. TC V_{OS} Distribution

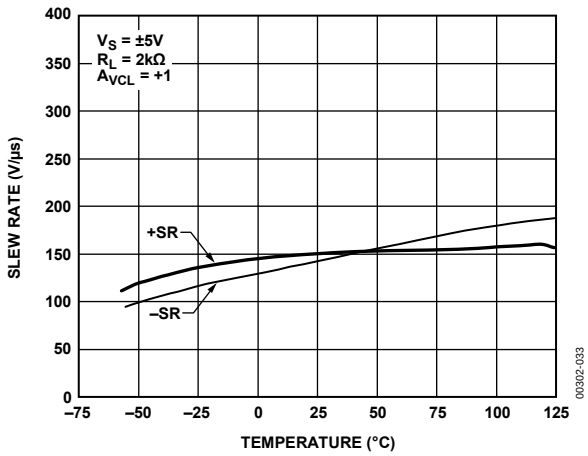


Figure 33. Slew Rate vs. Temperature

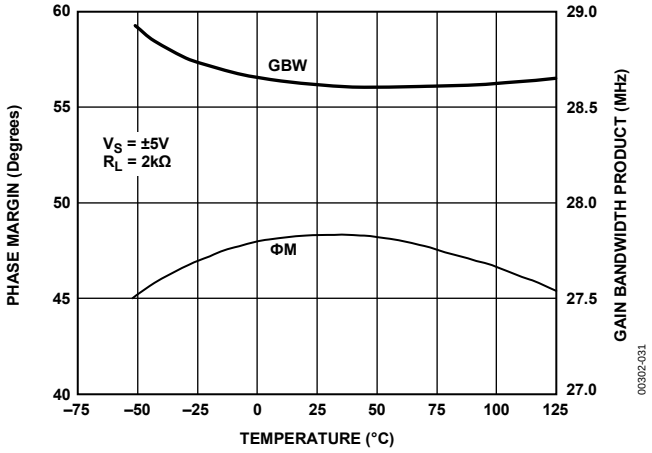


Figure 31. Phase Margin and Gain Bandwidth vs. Temperature

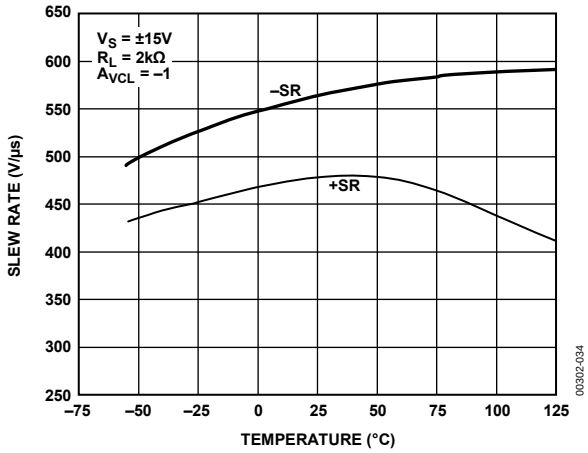


Figure 34. Slew Rate vs. Temperature

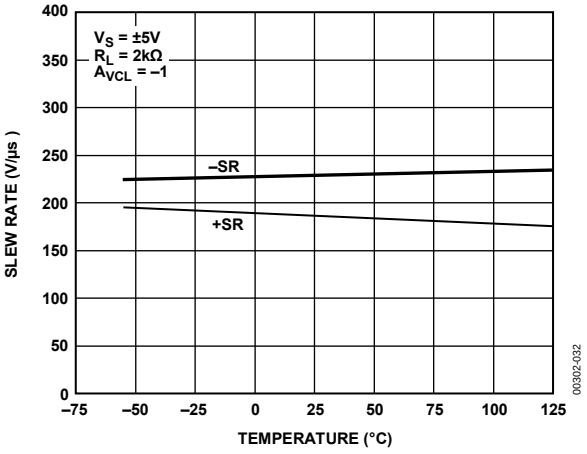


Figure 32. Slew Rate vs. Temperature

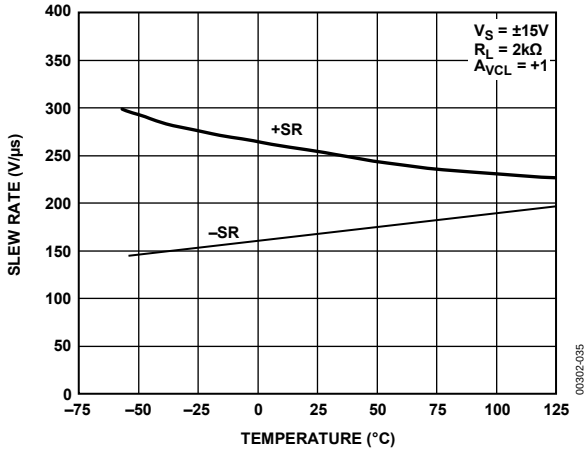


Figure 35. Slew Rate vs. Temperature

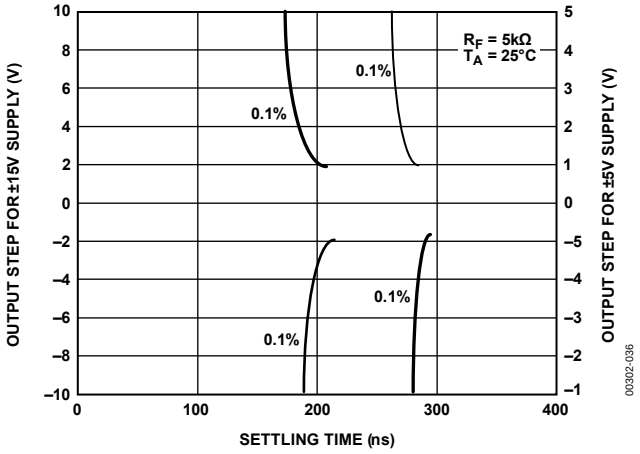


Figure 36. Output Step vs. Settling Time

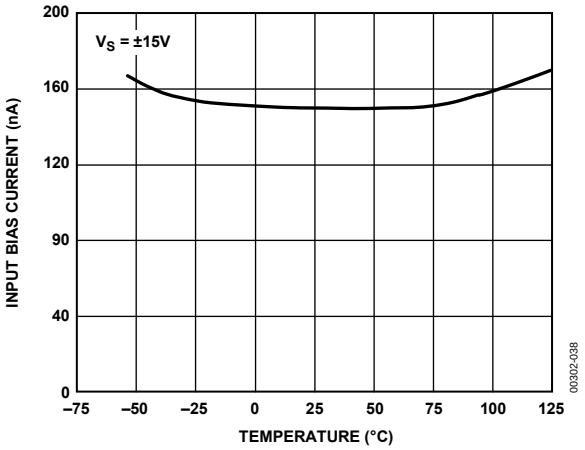


Figure 38. Input Bias Current vs. Temperature

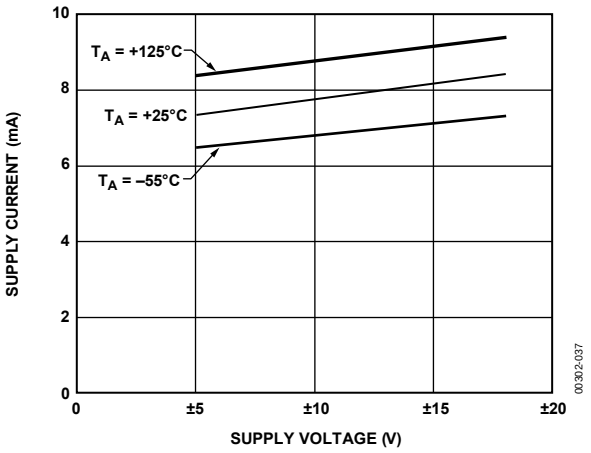


Figure 37. Supply Current vs. Supply Voltage

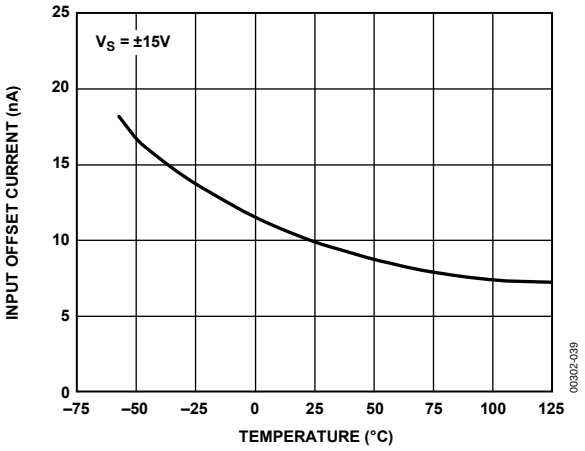


Figure 39. Input Offset Current vs. Temperature

APPLICATIONS INFORMATION

OUTPUT SHORT-CIRCUIT PERFORMANCE

To achieve a wide bandwidth and high slew rate, the OP467 output is not short-circuit protected. Shorting the output to ground or to the supplies may destroy the device.

For safe operation, the output load current should be limited so that the junction temperature does not exceed the absolute maximum junction temperature.

The maximum internal power dissipation can be calculated by

$$P_D = \frac{T_J \max - T_A}{\theta_{JA}}$$

where:
T_J and T_A are junction and ambient temperatures, respectively.
P_D is device internal power dissipation.
θ_{JA} is the packaged device thermal resistance given in the data sheet.

UNUSED AMPLIFIERS

It is recommended that any unused amplifiers in the quad package be connected as a unity-gain follower with a 1 kΩ feedback resistor with noninverting input tied to the ground plain.

PCB LAYOUT CONSIDERATIONS

Satisfactory performance of a high speed op amp largely depends on a good PCB layout. To achieve the best dynamic performance, follow the high frequency layout technique.

GROUNDING

A good ground plain is essential to achieve the optimum performance in high speed applications. It can significantly reduce the undesirable effects of ground loops and IR drops by providing a low impedance reference point. Best results are obtained with a multilayer board design with one layer assigned to the ground plain. To maintain a continuous and low impedance ground, avoid running any traces on this layer.

POWER SUPPLY CONSIDERATIONS

In high frequency circuits, device lead length introduces an inductance in series with the circuit. This inductance, combined with stray capacitance, forms a high frequency resonance circuit. Poles generated by these circuits cause gain peaking and additional phase shift, reducing the phase margin of the op amp and leading to an unstable operation.

A practical solution to this problem is to reduce the resonance frequency low enough to take advantage of the power supply rejection of the amplifier. This is easily done by placing capacitors across the supply line and the ground plane as close as possible to the device pin. Because capacitors also have internal parasitic components, such as stray inductance, selecting the right capacitor is important. To be effective, they should have low impedance over the frequency range of interest. Tantalum capacitors are an excellent choice for their high capacitance/size ratio, but their effective series resistance (ESR) increases with frequency making them less effective.

On the other hand, ceramic chip capacitors have excellent ESR and effective series inductance (ESL) performance at higher frequencies, and because of their small size, they can be placed very close to the device pin, further reducing the stray inductance. Best results are achieved by using a combination of these two capacitors. A 5 µF to 10 µF tantalum parallel capacitor with a 0.1 µF ceramic chip capacitor is recommended. If additional isolation from high frequency resonances of the power supply is needed, a ferrite bead should be placed in series with the supply lines between the bypass capacitors and the power supply. Note that addition of the ferrite bead introduces a new pole and zero to the frequency response of the circuit and could cause unstable operation if it is not selected properly.

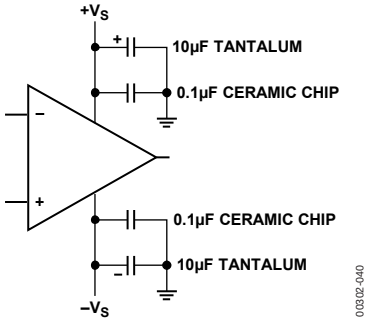


Figure 40. Recommended Power Supply Bypass

SIGNAL CONSIDERATIONS

Input and output traces need special attention to assure a minimum stray capacitance. Input nodes are very sensitive to capacitive reactance, particularly when connected to a high impedance circuit. Stray capacitance can inject undesirable signals from a noisy line into a high impedance input. Protect high impedance input traces by providing guard traces around them, which also improves the channel separation significantly.

Additionally, any stray capacitance in parallel with the input capacitance of the op amp generates a pole in the frequency response of the circuit. The additional phase shift caused by this pole reduces the gain margin of the circuit. If this pole is within the gain range of the op amp, it causes unstable performance. To reduce these undesirable effects, use the lowest impedance where possible. Lowering the impedance at this node places the poles at a higher frequency, far above the gain range of the amplifier. Stray capacitance on the PCB can be reduced by making the traces narrow and as short as possible. Further reduction can be realized by choosing a smaller pad size, increasing the spacing between the traces, and using PCB material with a low dielectric constant insulator (dielectric constant of some common insulators: air = 1, Teflon® = 2.2, and FR4 = 4.7, with air being an ideal insulator).

Removing segments of the ground plane directly under the input and output pads is recommended.

Outputs of high speed amplifiers are very sensitive to capacitive loads. A capacitive load introduces a pair of pole and zero to the frequency response of the circuit, reducing the phase margin, leading to unstable operation or oscillation.

Generally, it is good design practice to isolate the output of the amplifier from any capacitive load by placing a resistor between the output of the amplifier and the rest of the circuits. A series resistor of 10 Ω to 100 Ω is normally sufficient to isolate the output from a capacitive load.

The OP467 is internally compensated to provide stable operation and is capable of driving large capacitive loads without oscillation.

Sockets are not recommended because they increase the lead inductance/capacitance and reduce the power dissipation of the package by increasing the thermal resistance of the leads. If sockets must be used, use Teflon or pin sockets with the shortest possible leads.

PHASE REVERSAL

The OP467 is immune to phase reversal; its inputs can exceed the supply rails by a diode drop without any phase reversal.

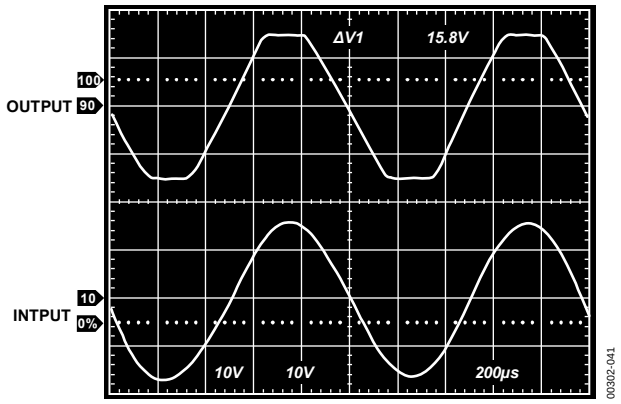


Figure 41. No Phase Reversal (A_V = +1)

SATURATION RECOVERY TIME

The OP467 has a fast and symmetrical recovery time from either rail. This feature is very useful in applications such as high speed instrumentation and measurement circuits, where the amplifier is frequently exposed to large signals that overload the amplifier.

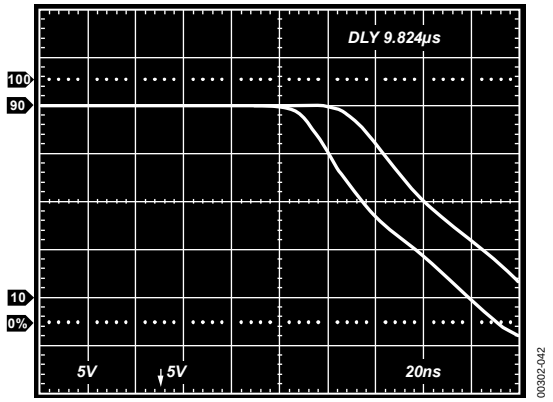


Figure 42. Saturation Recovery Time, Positive Rail

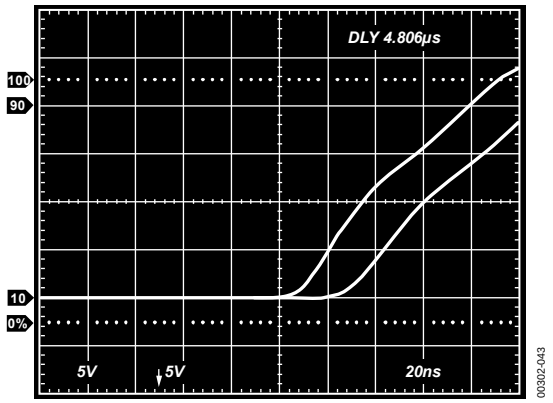


Figure 43. Saturation Recovery Time, Negative Rail

HIGH SPEED INSTRUMENTATION AMPLIFIER

The OP467 performance lends itself to a variety of high speed applications, including high speed precision instrumentation amplifiers. Figure 44 represents a circuit commonly used for data acquisition, CCD imaging, and other high speed applications.

The circuit gain is set by R_G. A 2 kΩ resistor sets the circuit gain to 2; for unity gain, remove R_G. For any other gain settings, use the following formula

$$G = 2/R_G \text{ (Resistor Value is in k}\Omega\text{)}$$

R_C is used for adjusting the dc common-mode rejection, and C_C is used for ac common-mode rejection adjustments.

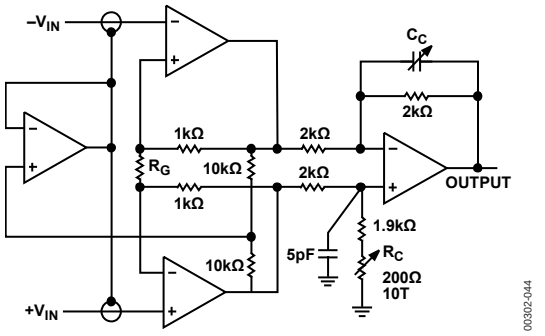


Figure 44. A High Speed Instrumentation Amplifier

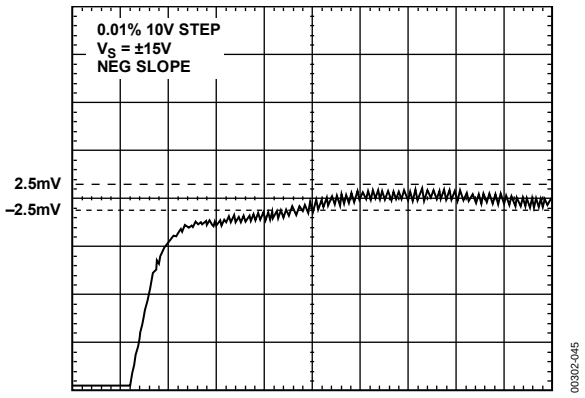


Figure 45. Instrumentation Amplifier Settling Time to 0.01% for a 10 V Step Input (Negative Slope)

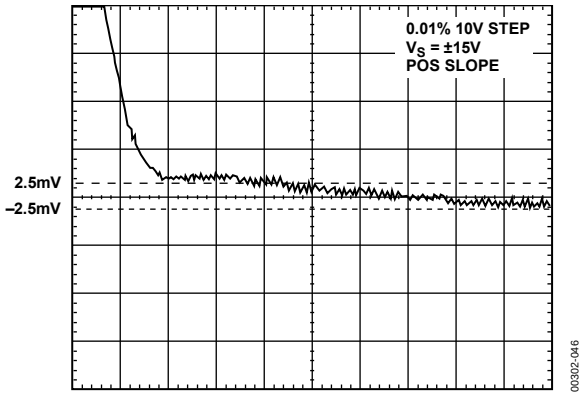


Figure 46. Instrumentation Amplifier Settling Time to 0.01% for a 10 V Step Input (Positive Slope)

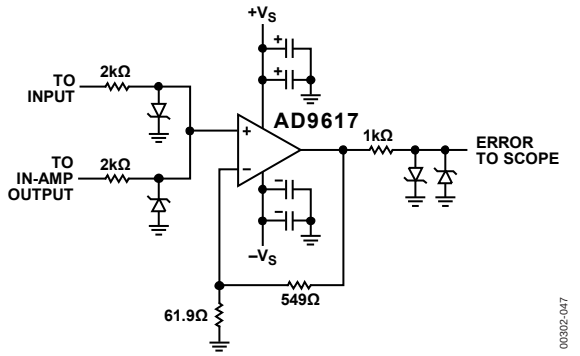


Figure 47. Settling Time Measurement Circuit

2 MHz BIQUAD BAND-PASS FILTER

The circuit in Figure 48 is commonly used in medical imaging ultrasound receivers. The 30 MHz bandwidth is sufficient to accurately produce the 2 MHz center frequency, as the measured response shows in Figure 49. When the bandwidth of the op amp is too close to the center frequency of the filter, the internal phase shift of the amplifier causes excess phase shift at 2 MHz, which alters the response of the filter. In fact, if the chosen op amp has a bandwidth close to 2 MHz, the combined phase shift of the three op amps causes the loop to oscillate.

Careful consideration must be given to the layout of this circuit as with any other high speed circuit.

If the phase shift introduced by the layout is large enough, it can alter the circuit performance, or worse, cause oscillation.

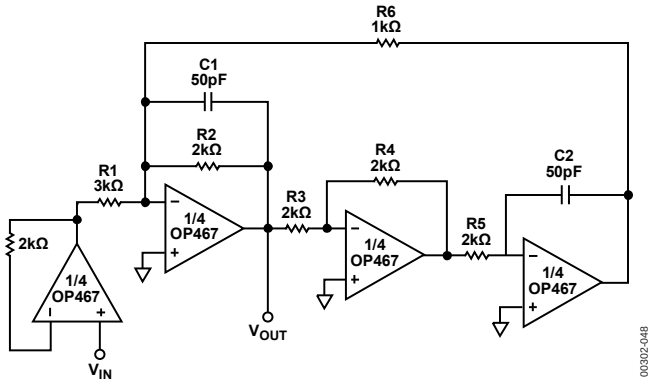


Figure 48. 2 MHz Biquad Filter

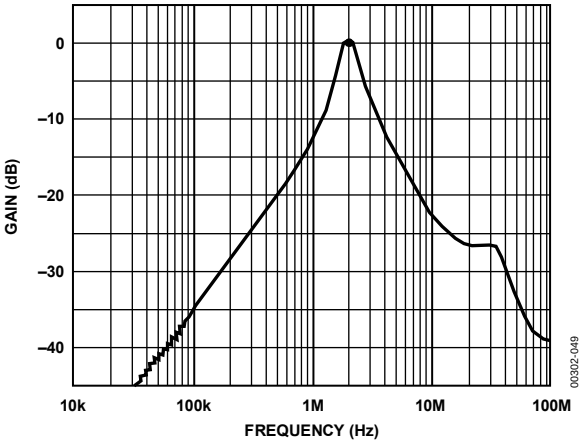


Figure 49. Biquad Filter Response

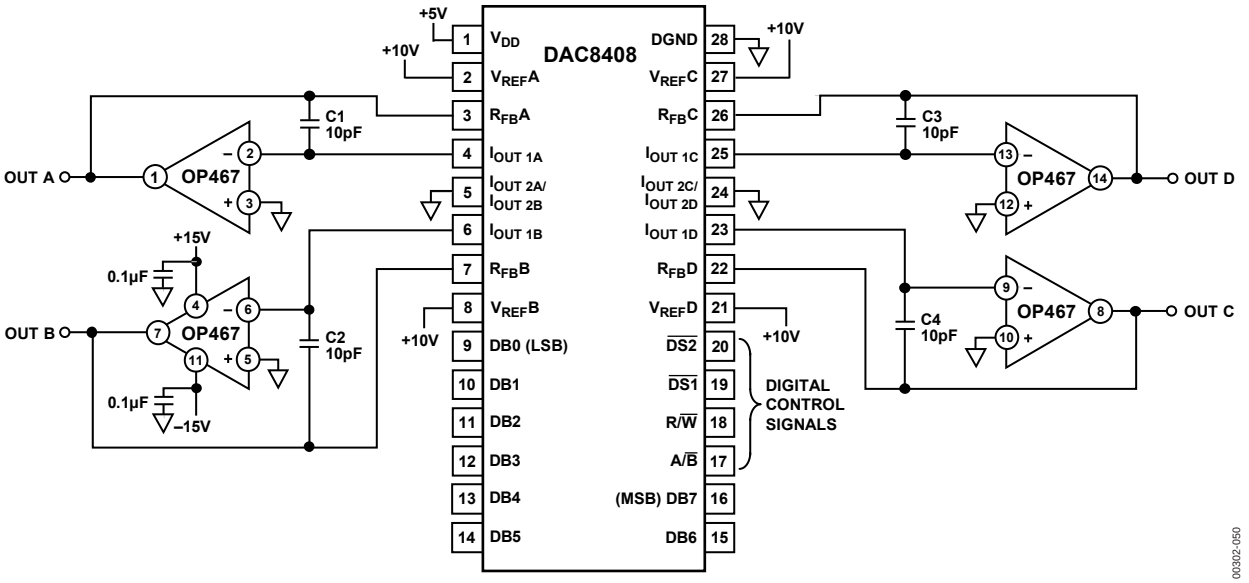


Figure 50. Quad DAC Unipolar Operation

FAST I-TO-V CONVERTER

The fast slew rate and fast settling time of the OP467 are well suited to the fast buffers and I-to-V converters used in a variety of applications. The circuit in Figure 50 is a unipolar quad DAC consisting of only two ICs. The current output of the DAC8408 is converted to a voltage by the OP467 configured as an I-to-V converter. This circuit is capable of settling to 0.1% within 200 ns. Figure 51 and Figure 52 show the full-scale settling time of the outputs. To obtain reliable circuit performance, keep the traces from the I_{OUT} of the DAC to the inverting inputs of the OP467 short to minimize parasitic capacitance.

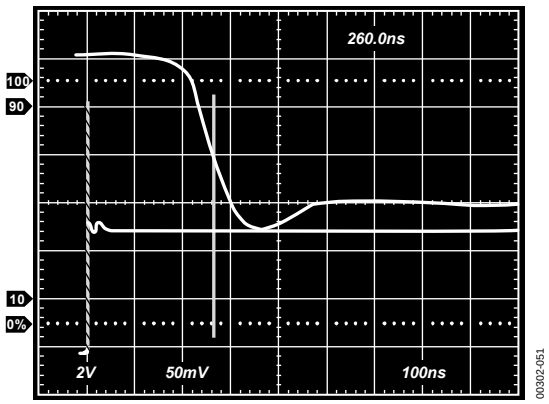


Figure 51. Falling Edge Output Settling Time

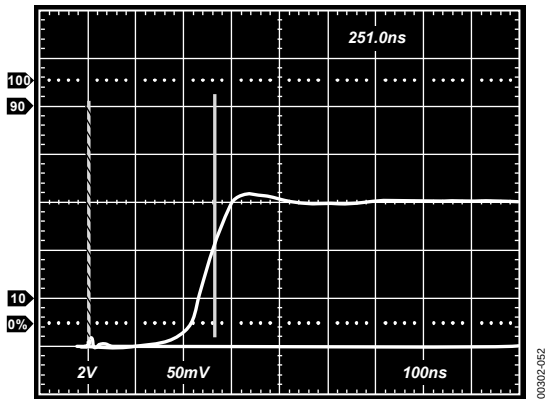


Figure 52. Rising Edge Output Settling Time

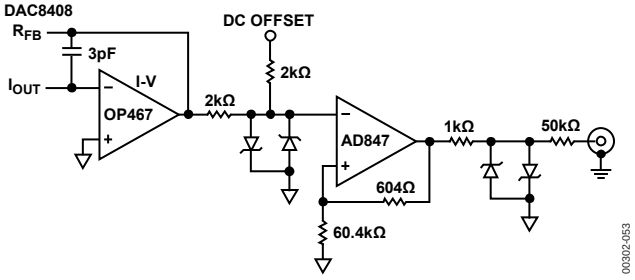


Figure 53. DAC V_{OUT} Settling Time Circuit

OP467 SPICE MARCO-MODEL

```
* Node assignments
                        noninverting input
                        |       inverting input
                        |       |       positive supply
                        |       |       |       negative supply
                        |       |       |       |       output
*                       |       |       |       |       |
. SUBCKT OP467          1       2       99      50      27
*
* INPUT STAGE
*
I1      4       5       10E–3
                0
CIN     1       2       1E–12
IOS     1       2       5E–9
Q1      5       2       8 QN
Q2      6       7       9 QN
R3      99      5       185 . 681
R4      99      6       185 . 681
R5      8       4       180 . 508
R6      9       4       180 . 508
EOS     7       1       POLY (1)        (14,20)     50E–6     1
EREF    98      0       (20,0) 1
*
* GAIN STAGE AND DOMINANT POLE AT 1.5 kHz
*
R7      10      98      3 . 714E6
C2      10      98      28 . 571E–12
G1      98      10      (5,6) 5 . 386E–3
V1      99      11      1 . 6
V2      12      50      1 . 6
D1      10      11      DX
D2      12      10      DX
RC      10      28      1 . 4E3
CC      28      27      12E–12
*
* COMMON-MODE STAGE WITH ZERO AT 1.26 kHz
*
ECM     13      98      POLY (2)    (1, 20)     (2,20) 0 0.  5 0 . 5
R8      13      14      1E6
R9      14      98      25 . 119
C3      13      14      126 . 721E–12
*
*POLE AT 400E6
*
R10     15      98      1E6
C4      15      98      0 . 398E–15
G2      98      15      (10,20) 1E–6
*
* OUTPUT STAGE
*
ISY     99      50      –8 . 183E–3
RMP1    99      20      96 . 429E3
RMP2    20      50      96 . 429E3
RO1     99      26      200
RO2     26      50      200
L1      26      27      1E–7
GO1     26      99      (99,15) 5E–3
GO2     50      26      (15,50) 5E–3
G4      23      50      (15,26) 5E–3
G5      24      50      (26,15) 5E–3
V3      21      26      50
V4      26      22      50
D3      15      21      DX
D4      22      15      DX
D5      99      23      DX
D6      99      24      DX
D7      50      23      DY
D8      50      24      DY
*
* MODELS USED
*
. MODEL QN NPN (BF=33.333E3)
. MODEL DX D
. MODEL DY D (BV=50)
. ENDS OP467
```

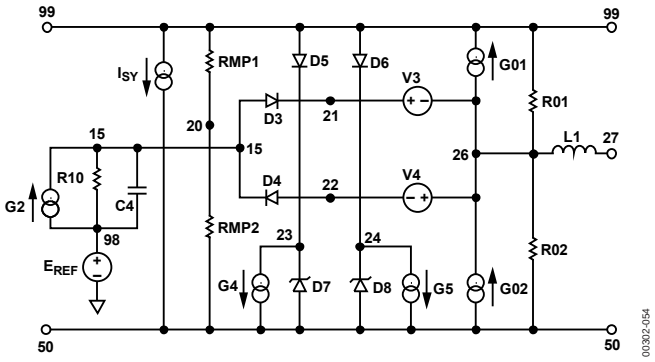


Figure 54. SPICE Macro-Model Output Stage

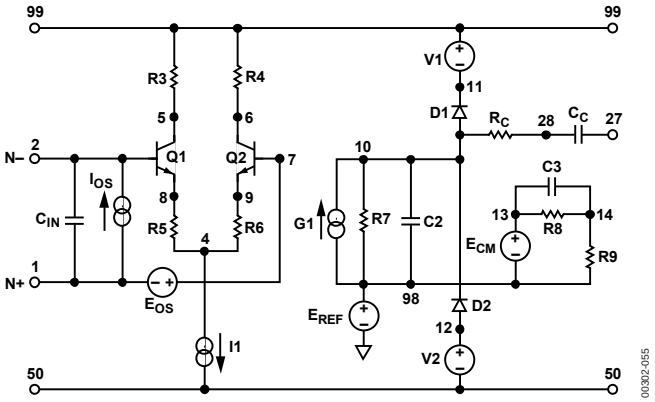
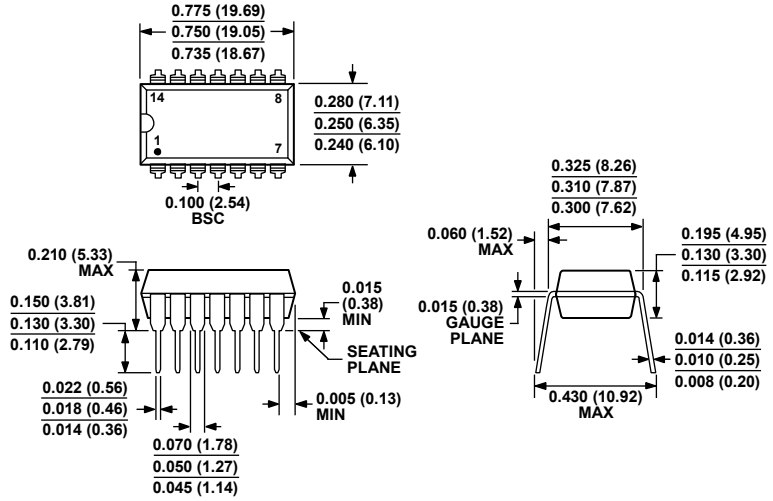


Figure 55. SPICE Macro-Model Input and Gain Stage

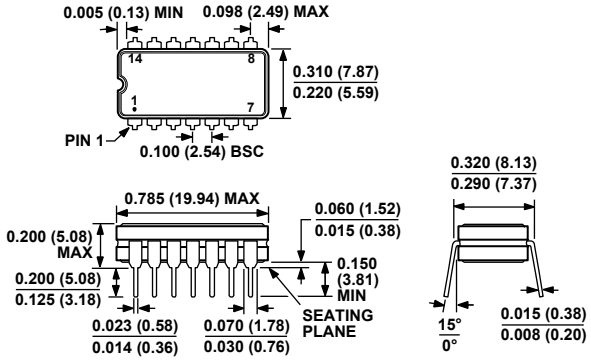
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

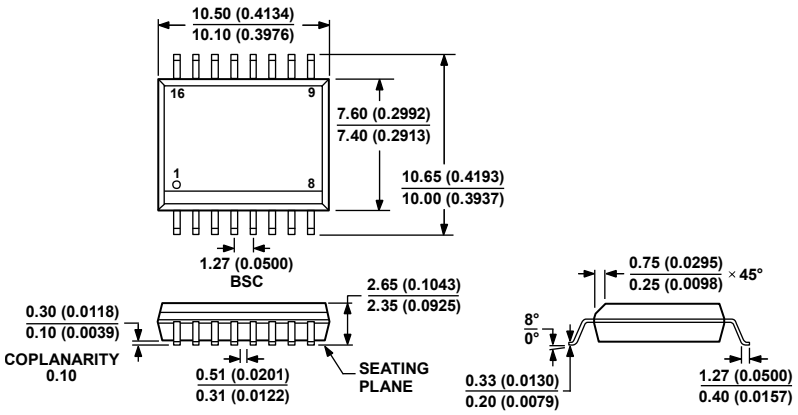
07 06 06-A

Figure 56. 14-Lead Plastic Dual In-Line Package [PDIP]
(N-14)
P-Suffix
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 57. 14-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-14)
Y-Suffix
Dimensions shown in inches and (millimeters)



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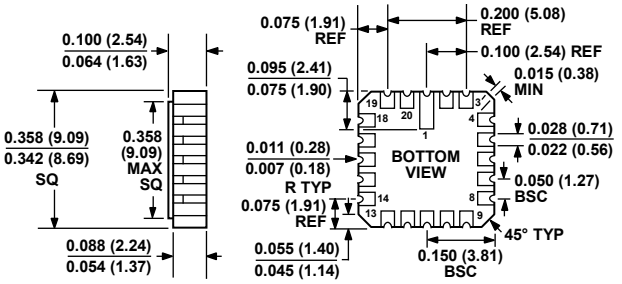
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 58. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
S-Suffix
Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

022106-A

Figure 59. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20-1) RC-Suffix
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
OP467GP	−40°C to +85°C	14-Lead PDIP	N-14
OP467GPZ	−40°C to +85°C	14-Lead PDIP	N-14
OP467GS	−40°C to +85°C	16-Lead SOIC_W	RW-16
OP467GS-REEL	−40°C to +85°C	16-Lead SOIC_W	RW-16
OP467GSZ	−40°C to +85°C	16-Lead SOIC_W	RW-16
OP467GSZ-REEL	−40°C to +85°C	16-Lead SOIC_W	RW-16
OP467ARC/883C	−55°C to +125°C	20-Terminal LCC	E-20-1
OP467AY/883C	−55°C to +125°C	14-Lead CERDIP	Q-14
OP467GBC		Die	

[1] Z = RoHS Compliant Part.

D00302-0-4/10(I)

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5962-9325801M2A OP467AY/883C OP467GS OP467GP OP467GPZ OP467GSZ 5962-9325801MCA OP467ARC/883C OP467GS-REEL OP467GSZ-REEL