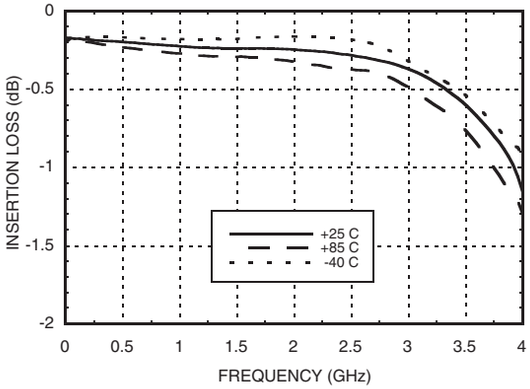
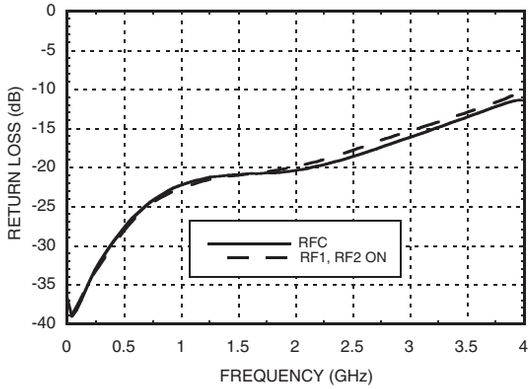
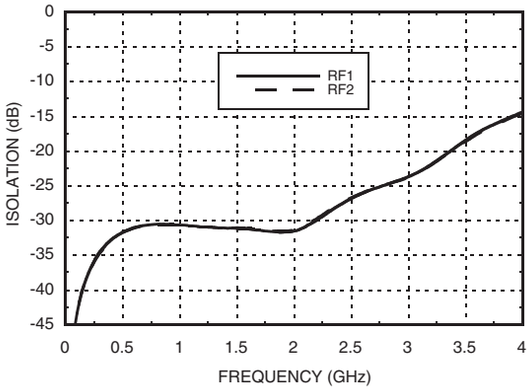
Insertion Loss



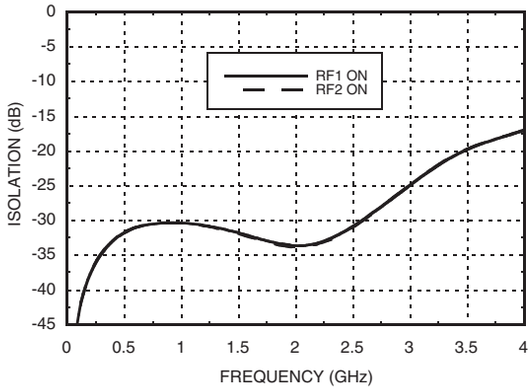
Return Loss



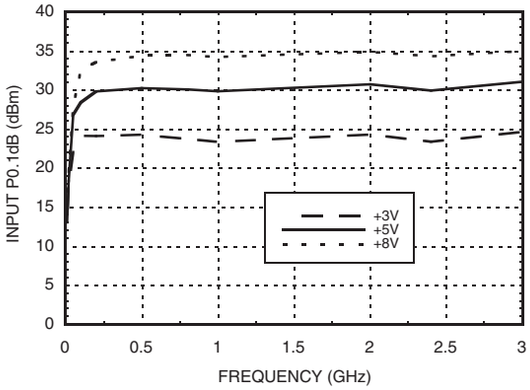
Isolation Between Ports RFC and RF1/RF2



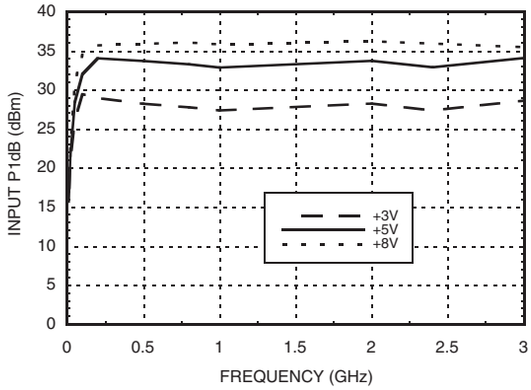
Isolation Between Ports RF1 and RF2



Input P0.1dB vs. Vctl



Input P1dB vs. Vctl



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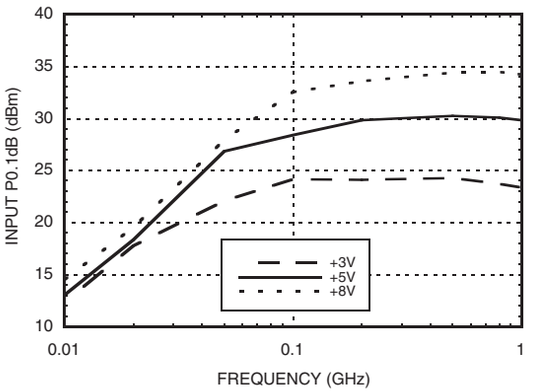
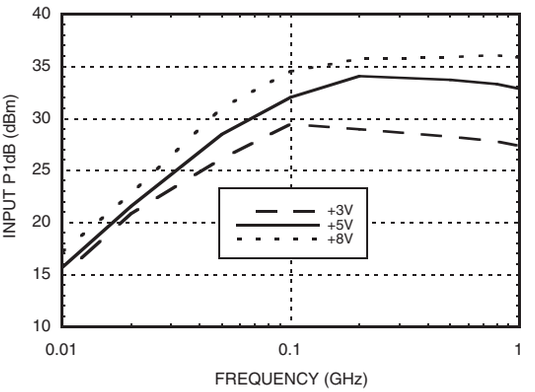
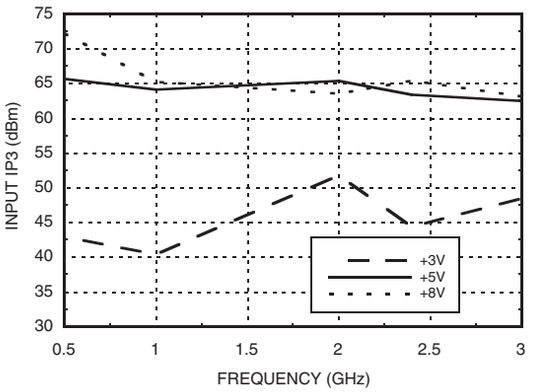
Low Frequency Input P0.1dB vs. Vctl



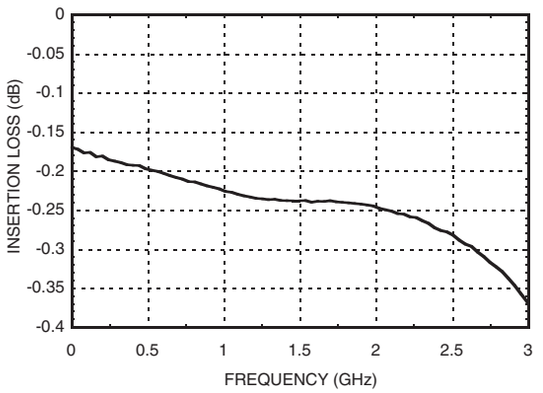
Low Frequency Input P1dB vs. Vctl



Input Third Order Intercept Point vs. Control Voltage



Insertion Loss, T = +25 °C



Absolute Maximum Ratings

RF Input Power (Vctl = 0/+8V)	+34 dBm
Control Voltage Range (A & B)	-0.2 to +12 Vdc
Hot Switch Power Level (Vctl = 0/+8V)	+32 dBm
Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 3.5 mW/ °C above 85°C)	0.23 W
Thermal Resistance	282 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

DC blocks are required at ports RFC, RF1 and RF2.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Truth Table

Control Input		Control Current	
A	B	RFC to RF1	RFC to RF2
Low	High	Off	On
High	Low	On	Off

Control Voltages

State	Bias Condition
Low	0 to 0.2 Vdc @ 1 µA Typical
High	+3 Vdc @ 0.5 µA Typical to +8 Vdc @ 3 µA Typical (±0.2 Vdc)

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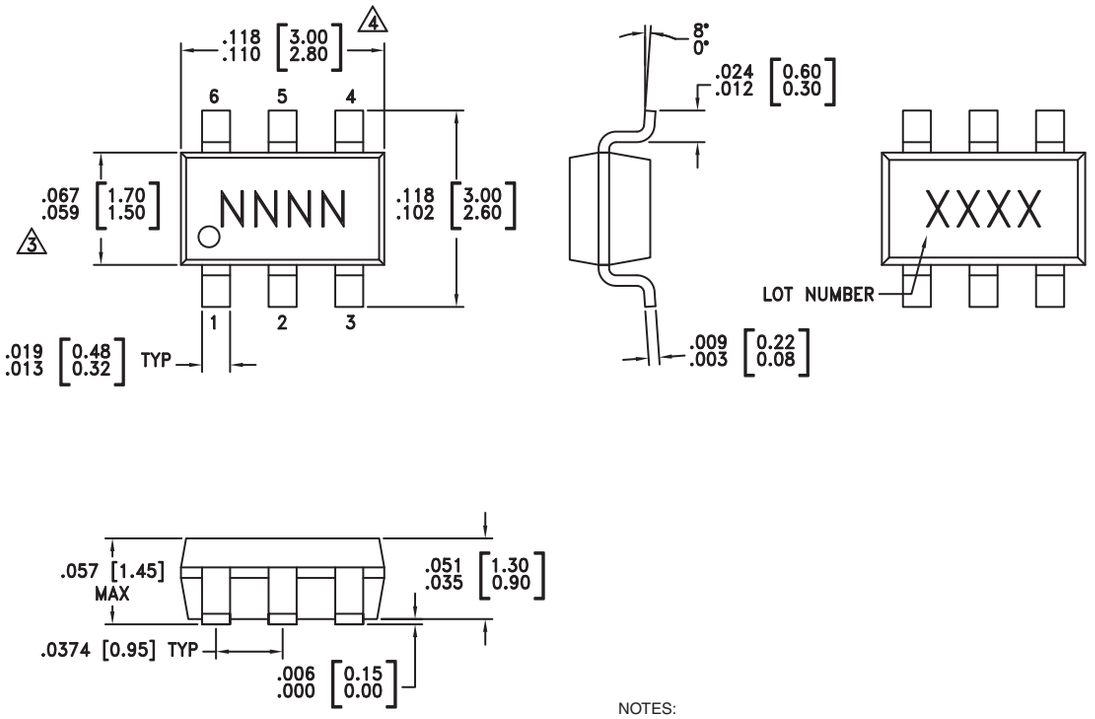
Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking
HMC545	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H545
HMC545E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	545E

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C

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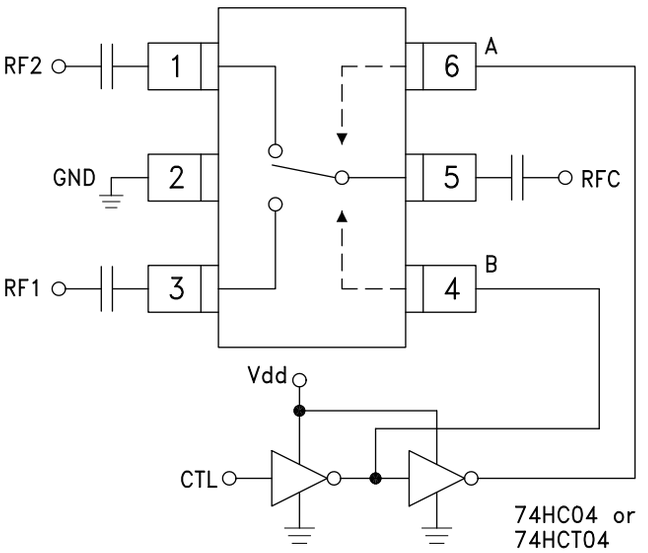
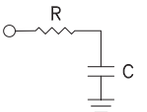
Typical Application Circuit



Notes:

1. Set logic gate Vdd = +3V to +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of +3V to +8V applied to the CMOS logic gates.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with Vdd = +8V and A/B set to 0/+8V.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 5	RF2, RF1, RFC	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required.	
2	GND	This pin must be connected to RF/DC ground.	
4	B	See truth and control voltage tables.	
6	A	See truth and control voltage tables.	

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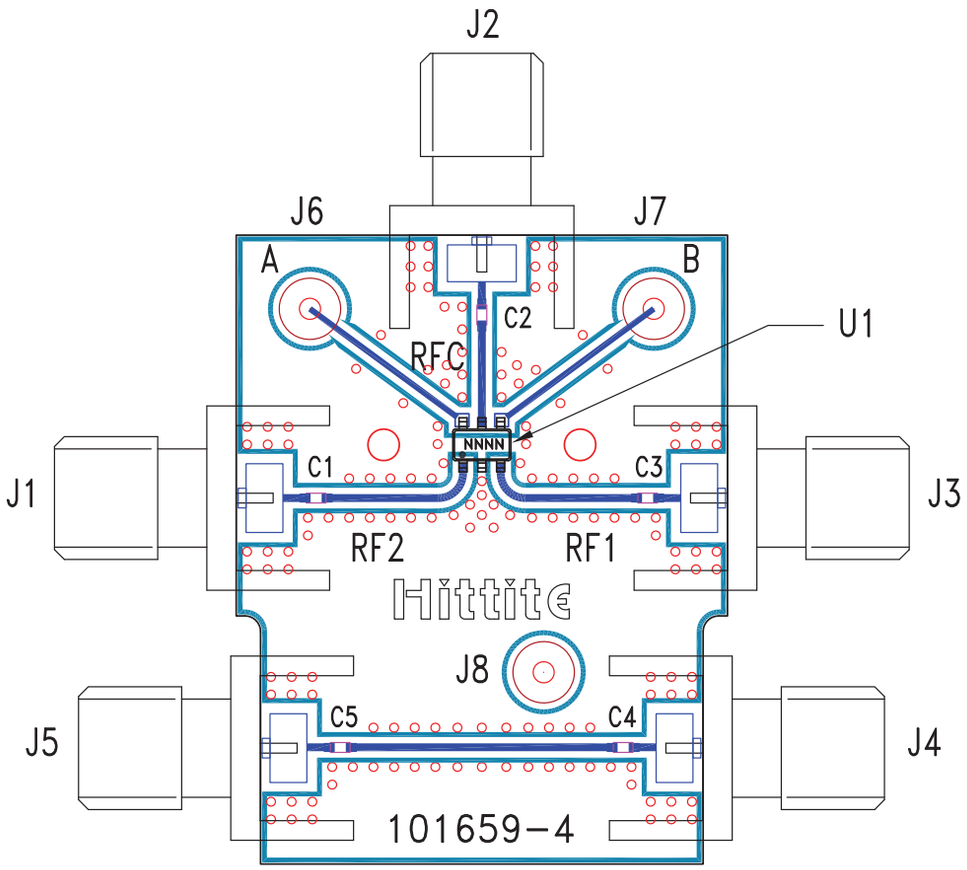
Evaluation PCB



List of Materials for Evaluation PCB 101675 [1]

Item	Description
J1 - J5	PCB Mount SMA RF Connector
J6 - J8	DC Pin
C1 - C5	330 pF capacitor, 0402 Pkg.
U1	HMC545 / HMC545E SPDT Switch
PCB [2]	101659 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 ohm impedance and the package ground leads should be connected directly to the ground plane similar to that shown above. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.

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