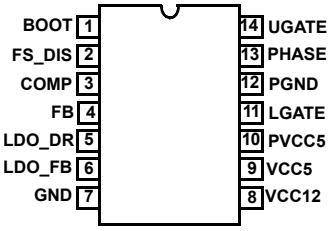
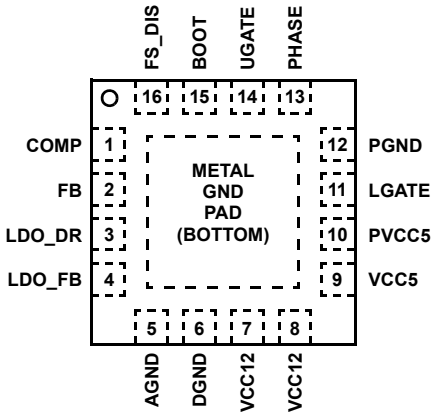
Pinouts

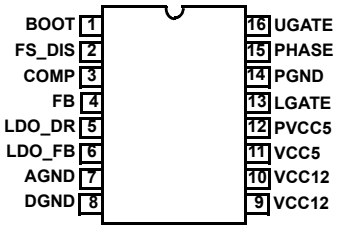
ISL6549 (SOIC)
TOP VIEW



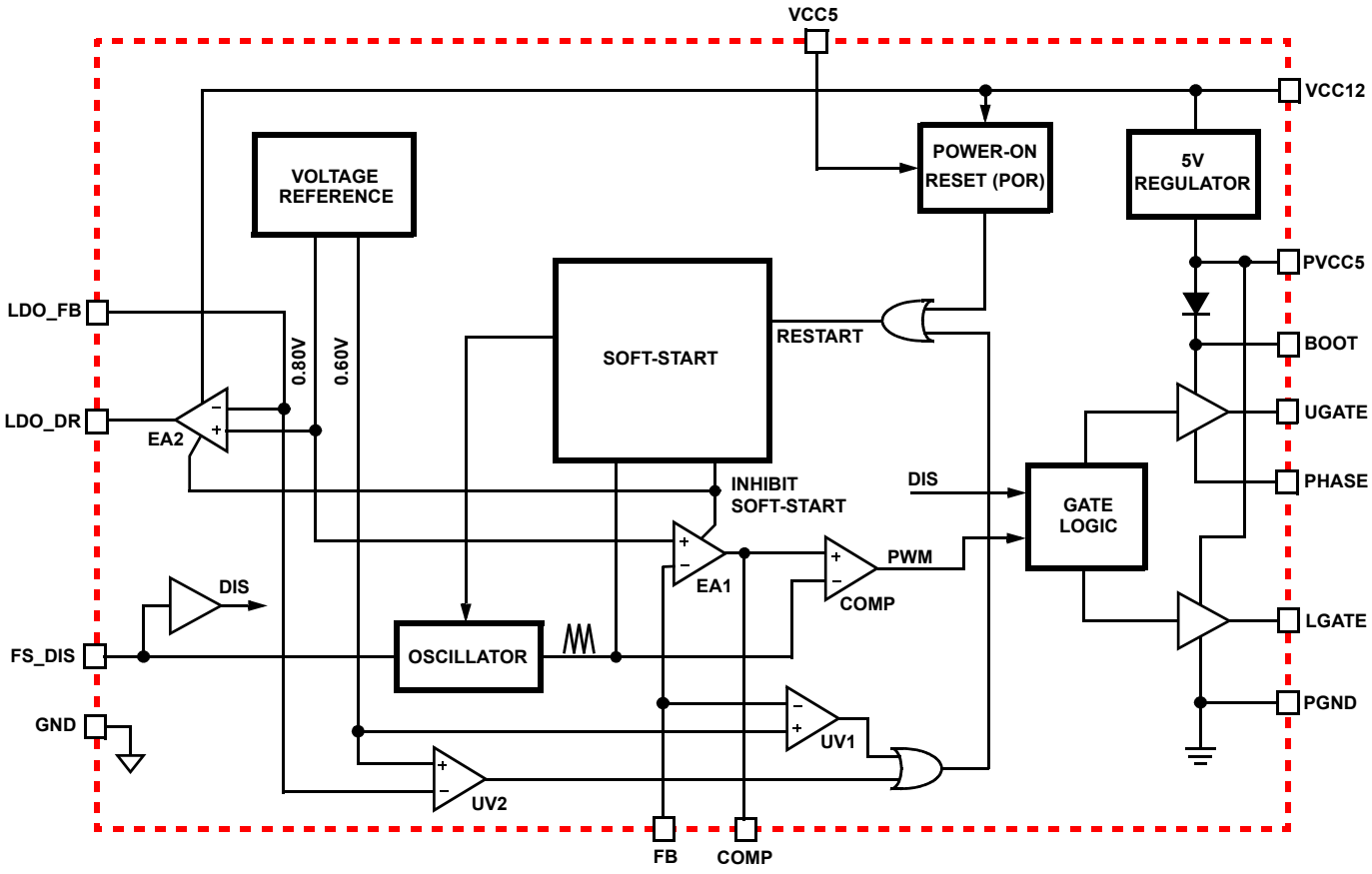
ISL6549 (QFN)
TOP VIEW



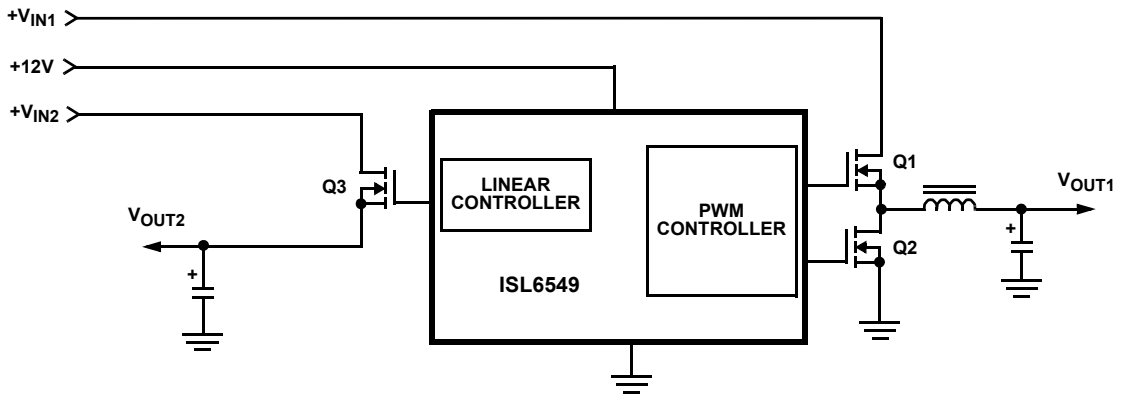
ISL6549 (QSOP)
TOP VIEW



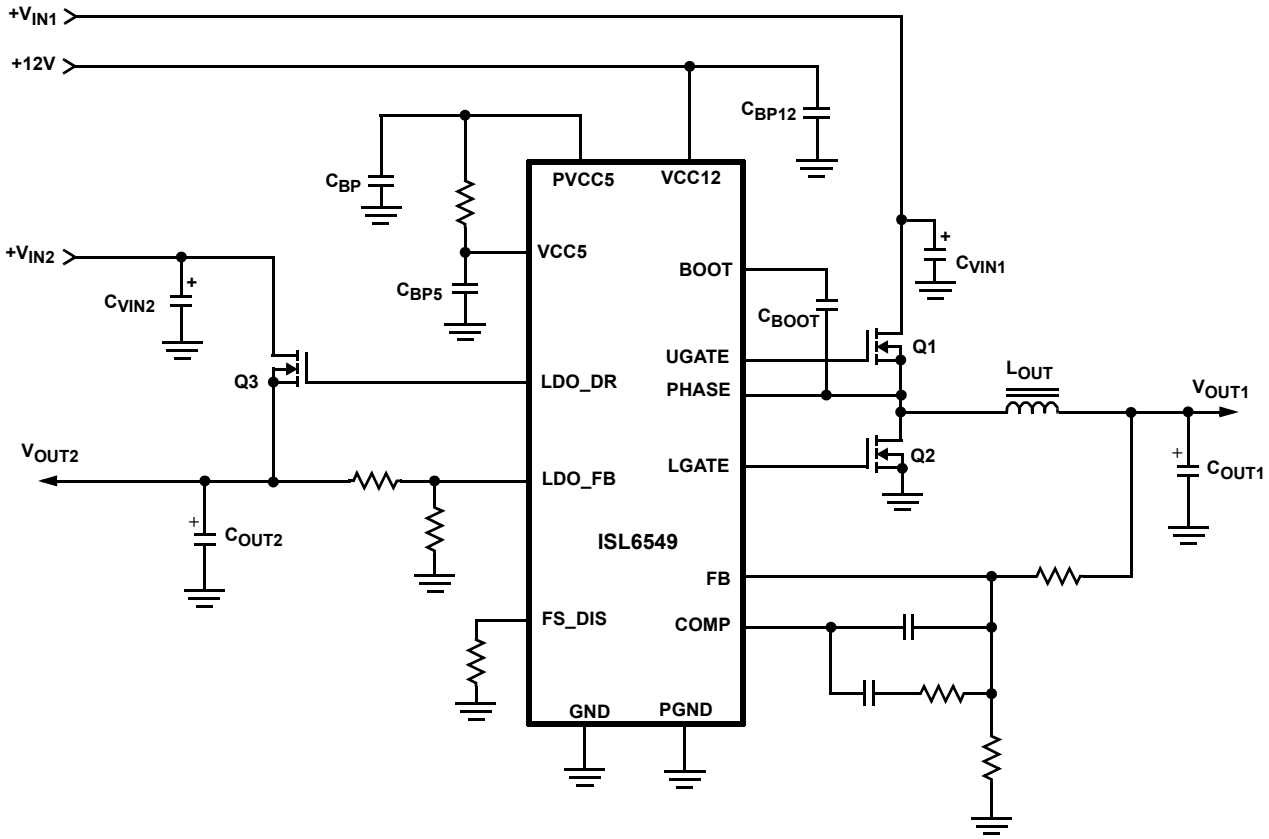
Block Diagram



Simplified Power System Diagram



Typical Application Schematic



Absolute Maximum Ratings

VCC12 . . . . . GND - 0.3V to +14V
PVCC5, VCC5 . . . . . GND - 0.3V to +7V
VCC5 (if used with external supply) . . . . . GND - 0.3V to +6V
BOOT . . . . . GND - 0.3V to +27V
PHASE . . . . . V_{BOOT} - 7V to V_{BOOT} + 0.3V
V_{BOOT} - V_{PHASE} . . . . . +7V
UGATE . . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
LGATE . . . . . GND - 0.3V to PVCC5 + 0.3V
LDO_DR . . . . . GND - 0.3V to VCC12 + 0.3V
FB, LDO_FB, COMP, FS_DIS . . . . . GND - 0.3V to VCC5 + 0.3V
ESD Classification
Human Body Model (Per JESD22-A114C) . . . . . Class 2
Machine Model (Per EIA/JESD22-A115-A) . . . . . Class B
Charge Device Model (Per JESD22-C101C) . . . . . Class IV

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	105	N/A
QFN Package (Notes 2, 3)	52	14
QSOP Package (Note 1)	110	N/A

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC - Lead Tips Only)

Recommended Operating Conditions

External Supply Voltage on VCC5 . . . . . +5.0V ±5%
Supply Voltage on VCC12 . . . . . +12V ±10%
Ambient Temperature Range (C) . . . . . 0°C to 70°C
Ambient Temperature Range (I) . . . . . -40°C to +85°
Junction Temperature Range . . . . . 0°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted. VCC12 = 12V Temperature = 0 to +70°C (typical = +25°C) for Commercial; Temperature = -40 to + 85°C (typical = +25°C) for Industrial. Refer to Block Diagram, Simplified Power System Diagram, and Typical Application Schematic.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current VCC12 (disabled)	$I_{CC12\ dis}$	UGATE, LGATE and LDO_DR open; FS_DIS = GND		2	3	mA
Nominal Supply Current VCC5 (disabled)	$I_{CC5\ dis}$	UGATE, LGATE and LDO_DR open; FS_DIS = GND (Note 4)		5	7.5	mA
Nominal Supply Current VCC12 (includes PVCC5 current)	I_{CC12}	UGATE, LGATE and LDO_DR open; F_{OSC} = 620kHz		12	18	mA
Nominal Supply Current VCC5	I_{CC5}	UGATE, LGATE and LDO_DR open; F_{OSC} = 620kHz		4	6	mA
Maximum PVCC5 Current Available (Note 5)	I_{PVCC5}			100		mA
VCC12 to PVCC5 Current Limit (Note 5)	$I_{PVCC5CL}$			150		mA
PVCC5 Voltage	V_{PVCC5}	ISL6549C; No external load	4.95	5.25	5.8	V
		ISL6549I; No external load	4.85	5.25	5.8	
POWER-ON RESET						
Rising VCC5 Threshold		VCC12 = 12V	3.7	4.2	4.5	V
Falling VCC5 Threshold		VCC12 = 12V	3.3	3.8	4.1	V
Rising VCC12 Threshold		VCC5 = 5V	8.8	9.5	10.0	V
Falling VCC12 Threshold		VCC5 = 5V	7.0	7.5	8.0	V
OSCILLATOR AND SOFT-START						
Switching Frequency	F_{OSC}	ISL6549C; R_{FS_DIS} = 45.3kΩ	540	620	700	kHz
		ISL6549I; R_{FS_DIS} = 45.3kΩ	525	620	700	kHz

Electrical Specifications Recommended Operating Conditions, unless otherwise noted. VCC12 = 12V Temperature = 0 to +70°C (typical = +25°C) for Commercial; Temperature = -40 to + 85°C (typical = +25°C) for Industrial. Refer to Block Diagram, Simplified Power System Diagram, and Typical Application Schematic. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sawtooth Amplitude (Note 6)	DV_{OSC}			1.5		V
Soft-Start Interval	T_{SS}	F_{OSC} = 620kHz		6.8		ms
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}	ISL6549C; For Error Amp 1 and 2	0.792	0.8	0.808	V
		ISL6549I; For Error Amp 1 and 2	0.788	0.8	0.812	V
PWM CONTROLLER ERROR AMPLIFIER						
DC Gain (Note 6)		R_L = 10K, C_L = 10pF		96		dB
Gain-Bandwidth Product (Note 6)	GBWP	R_L = 10K, C_L = 10pF		20		MHz
Slew Rate (Note 6)	SR	R_L = 10K, C_L = 10pF		8		V/µs
FB Input Current	$\lvert I_I \rvert$	V_{FB} = 0.8V		0.1	1.0	µA
COMP High Output Voltage	V_{OUT} High			4.8		V
COMP Low Output Voltage	V_{OUT} Low			0.6		V
COMP High Output, Source Current	I_{OUT} High			-2.8		mA
Undervoltage Level (V_{FB}/V_{REF})	V_{UV}		70	75	80	%
PWM CONTROLLER GATE DRIVERS						
UGATE Maximum Voltage	V_{HUGATE}	VCC12 = 12V; PHASE = 12V	17	17.5	18	
LGATE Maximum Voltage	V_{HLGATE}	VCC12 = 12V; based on PVCC5 voltage		5.25	6	V
UGATE and LGATE Minimum Voltage	V_{LGATE}	VCC12 = 12V; PHASE = 0V		0	0.5	V
UGATE Source Output Impedance	$R_{DS(ON)}$	VCC12 = 12V; I_{GATE} = 100mA		0.8		Ω
UGATE Sink Output Impedance	$R_{DS(ON)}$	VCC12 = 12V; I_{GATE} = 100mA		0.7		Ω
LGATE Source Output Impedance	$R_{DS(ON)}$	VCC12 = 12V; I_{GATE} = 100mA		0.8		Ω
LGATE Sink Output Impedance	$R_{DS(ON)}$	VCC12 = 12V; I_{GATE} = 100mA		0.4		Ω
LINEAR REGULATOR (LDO_DR)						
DC Gain (Note 6)	Gain	R_L = 10K, C_L = 10pF		100		dB
Gain-Bandwidth Product (Note 6)	GBWP	R_L = 10K, C_L = 10pF		2		MHz
Slew Rate (Note 6)	SR	R_L = 10K, C_L = 10pF		6		V/µs
LDO_FB Input Current	$\lvert I_I \rvert$	V_{LDO_FB} = 0.8V		0.1	1.0	µA
LDO_DR High Output Voltage	V_{OUT} High	VCC12 = 12V		11.0	11.5	V
LDO_DR Low Output Voltage	V_{OUT} Low			0.0	0.5	V
LDO_DR High Output Source Current	I_{OUT} High	V_{OUT} = 2.0V		2.0		mA
LDO_DR Low Output Sink Current	I_{OUT} Low			0.5		mA
Undervoltage Level (V_{LDO_FB}/V_{REF})	V_{UV}	Percent of Nominal	70	75	80	%

NOTES:

4. Current in VCC5 is actually higher disabled, due to extra current required to pull down against the FS_DIS pin. VCC12 current is lower disabled.
5. Guaranteed by design, not production tested. Exceeding the maximum current from PVCC5 may result in degraded performance and unsafe operation.
6. Guaranteed by design, not production tested.

Functional Pin Description

VCC12

This is the power supply pin for the IC; it sources the internal 5V regulator used for the gate drivers. Provide a local decoupling capacitor to GND. The voltage at this pin is monitored for Power-On Reset (POR) purposes. The 16 Ld QFN and 16 Ld QSOP have two VCC12 pins; tie them together on the board.

VCC5

This pin supplies the internal 5V bias for analog and logic functions. Provide a local decoupling capacitor to GND, and a resistor to PVCC. The voltage at this pin is monitored for Power-On Reset (POR) purposes. See “Internal PVCC5 Regulator” on page 7 for more details.

GND, AGND, DGND

These pins are the signal ground for the IC. All voltage levels are measured with respect to these pins. Connect all to the ground plane via the shortest available path.

PVCC5

This pin is the internal 5V linear regulator for the BOOT supply (for the UGATE driver), and the source for the LGATE. Provide a local decoupling capacitor to PGND. Do not use this pin as a voltage source for other circuits. See “Internal PVCC5 Regulator” on page 7 for more details.

PGND

This pin is the power ground return for the lower gate driver. (LGATE). Connect to the ground plane on the board via the shortest available path.

UGATE

This output pin drives the upper MOSFET gate from the internal 5V regulator. Connect it to the gate of the upper MOSFET via a short, low inductance trace.

BOOT

The BOOT pin, along with the external capacitor (from PHASE to BOOT), an internal diode, and the internal 5.5V regulator, creates the bootstrap voltage for the upper gate driver (UGATE). The maximum voltage is around 5.5V (above PHASE).

PHASE

This pin represents the return path for the upper gate drive. Connect it to the source of the upper MOSFET via a short, low inductance trace.

LGATE

This output pin drives the lower MOSFET gate from the internal 5V regulator. Connect it to the gate of the lower MOSFET via a short, low inductance trace.

FB

FB is the available external inverting input pin of the error amplifier. Connect the output of the switching regulator to this pin through a properly sized resistor divider, to set the output voltage. The voltage at this pin is regulated to the internal reference voltage. This pin is also monitored for undervoltage detection.

COMP

COMP is the available external output pin of the error amplifier. This pin is used to compensate the voltage-mode control feedback loop of the standard synchronous rectified buck converter. Connect an appropriate compensation network between this and the FB pin. See *“PWM Controller Feedback Compensation” on page 10* for more information.

FS_DIS

This input pin has two functions. A resistor to GND sets the internal oscillator frequency for the switching regulator. In addition, if the pin is pulled down towards GND with a low impedance (<1kΩ, such as an external FET), it will disable both regulator outputs until released (at which time a new soft-start cycle will begin).

LDO_DR

This output pin provides the gate voltage for the linear regulator pass transistor. Connect this pin to the gate terminal of an external N-channel MOSFET transistor. This pin (along with the LDO_FB pin) also provides a means of compensating the error amplifier, should the application require it.

LDO_FB

This input pin is the FB inverting input on the linear regulator error amplifier. Connect the output of the linear regulator to this pin through a properly sized resistor divider, to set the output voltage. The voltage at this pin is regulated to the internal reference voltage. This pin is also monitored for undervoltage detection.

Bottom Pad (QFN Package Only)

The QFN package’s metal bottom pad is resistively tied to the internal IC GND. For best thermal and electrical performance, connect this pad to the GND pins, and to the ground plane of the PCB through 4 vias equidistantly situated inside the solder landing pad.

Description

Operation Overview

The ISL6549 monitors and precisely controls two output voltage levels. Refer to the *"Block Diagram" on page 2*, *"Simplified Power System Diagram" on page 3*, and *"Typical Application Schematic" on page 3*. The controller is intended for use in applications where only a 12V bias input is available. The IC integrates both a standard buck PWM controller and a linear controller. The PWM controller regulates the output voltage (V_{OUT1}) to a level programmed by a resistor divider. The linear controller is designed to regulate the lower current local memory voltage (V_{OUT2}) through an external N-Channel MOS pass transistor.

Internal PVCC5 Regulator

The preferred and recommended configuration is as follows: +12V to VCC12 pin, a resistor (~10Ω) between PVCC5 and VCC5 pins, and decoupling caps on all three pins to ground. This creates the PVCC5 voltage for the gate drivers, and externally filters it for bias on the VCC5 pin. It also guarantees that all 3 voltages track each other during power-up and power-down.

The PVCC5 pin cannot be used as an input and it should not be used as an output for other circuits; its current capability is reserved for the gate drivers and VCC5 bias. Similarly, the VCC5 pin should not be used as an output. Although not preferred, the VCC5 pin can be used with an external 5V supply (±5%). However, proper precautions must be followed, which mainly have to do with proper sequencing, to prevent latch-up or related problems. Note in the power-up diagram (Figure 1), the 5V lags the 12V by a few msecs and a volt or so; that is expected. Both the VCC12 and VCC5 pins must exceed their rising POR trip points before the soft-start is enabled; the trip order is not important as long as both have some voltage. The 12V can be present with no 5V at all, but the 5V should not precede the 12V. Similarly, on power down, the 5V should discharge with or before the 12V.

Under normal operation, the internal regulator can supply up to 100mA (which includes the VCC5 bias current, with the resistor between the pins). The amount of current is determined primarily by the switching parameters: the oscillator frequency and the loading of the FET gates. Overloading of the internal regulator is not recommended; even if there is enough current, the gate driver waveforms may be degraded. See *"Switcher FET Considerations" on page 13* for more details.

The PVCC5 pin has a current limit that provides some protection against a shorted gate driver dragging down the 12V rail. The temperature of the IC will increase as the current and corresponding on-chip power dissipation increases. There is no thermal shutdown, so even if the current limit is effective, the IC can be subject to very high temperatures. If the current limit is exceeded, the regulator voltage will likely collapse, shutting down everything until the load current is reduced or removed.

Initialization

The ISL6549 automatically initializes upon application of input power (at the VCC12) pin. The ISL6549 creates its own PVCC5 and VCC5 supplies for internal use. The POR function continually monitors the input bias supply voltage at the VCC12 and VCC5 pins. The POR function initiates soft-start operation after both these supply voltages exceed their POR rising threshold voltages.

Soft-Start

The POR function initiates the digital soft-start sequence. Both the linear regulator error amplifier and PWM error amplifier reference inputs are forced to track a voltage level proportional to the soft-start voltage. As the soft-start voltage slews up, the PWM comparator regulates the output relative to the tracked soft-start voltage, slowly charging the output capacitor(s). Simultaneously, the linear output follows the smooth ramp of the soft-start function into normal regulation.

Figure 1 shows the soft-start sequence. Both the VCC12 and VCC5 pins must be above their respective rising POR trip points. In most cases, as shown here, the last one exceeding its threshold is the VCC12 around 9.5V. The ramp time is based on the internal oscillator period multiplied by 4096. So for a 600kHz (1.67µs) example, the soft-start ramp time would be 6.8ms.

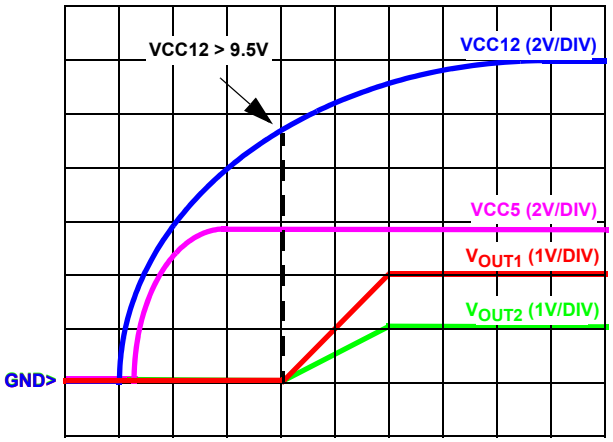


FIGURE 1. 12V POWER-UP INTO SOFT-START

Figure 2 shows more detail of the output ramps, by increasing the time and voltage resolution. The clock for the DAC producing the steps is approximately 9.4kHz (600kHz/64), so each step is just over 100µs long. The step voltage is 1/64 of the final value for each output; around 31mV for V_{OUT1} and 15.6mV for V_{OUT2} in this example. By providing many small steps of voltage (and current) that effectively charge the output capacitor, the potentially large peak current resulting from a sudden, uncontrolled voltage rise are eliminated, by spreading it out over the whole ramp time.

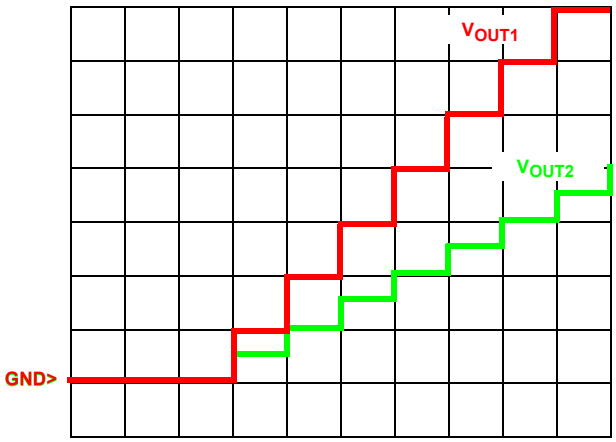


FIGURE 2. EXPANDED VIEW: VOLTAGE RAMP AND TIME

A few clock cycles are used for initialization to insure that soft-start begins near zero volts. The ramps are the same, whether triggered by releasing FS_DIS or by exceeding the POR trip levels.

Both outputs use the same soft-start ramp, and the ramp time is determined by the switching frequency. Thus, there is no simple way to disable or sequence them independently, or to change the ramp rate independently of the clock.

If the switcher output is already pre-charged to a voltage when the regulator starts up, the ISL6549 will detect this condition (see Figure 3). The red trace shows the normal ramp, when the output starts at GND. The green trace shows the case when the output is pre-charged to a voltage less than the final output. The upper or lower FET does not turn on until the soft-start ramp voltage exceeds the output; then the output starts ramping seamlessly from there. If the output voltage is pre-charged above the normal output level, as shown in the magenta trace, neither FET will turn on until the end of the soft-start ramp; then the output will be quickly pulled down to the final value.

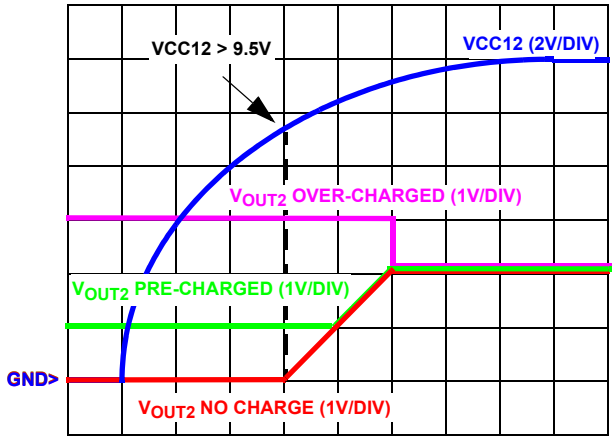


FIGURE 3. PRE-CHARGED OUTPUT

Undervoltage Protection

The FB and LDO_FB pins are each monitored during converter operation by their own Undervoltage (UV) comparator. If either FB voltage drops below 75% of the reference voltage (75% of 0.8V = 0.6V), a fault signal is internally generated, and the fault logic shuts down BOTH regulators. The UV comparators are enabled when the soft-start ramp is about one-quarter (25%) done.

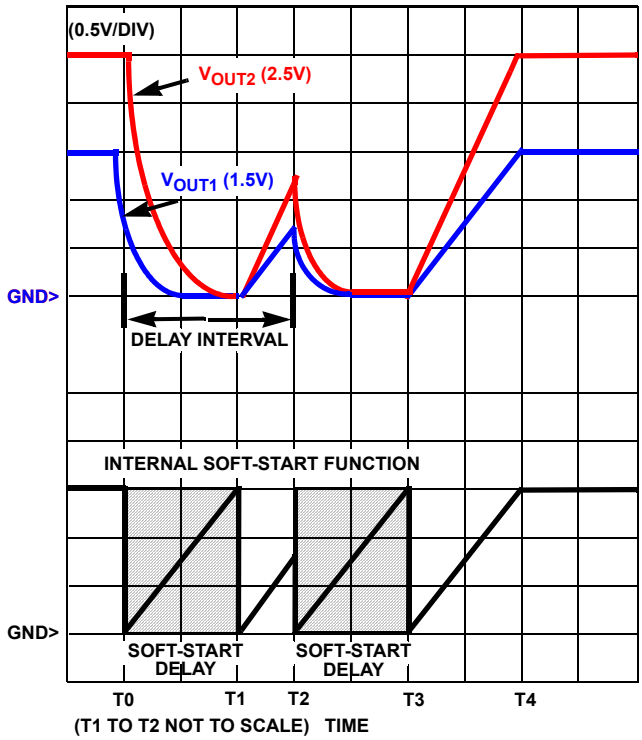


FIGURE 4. UNDERVOLTAGE PROTECTION RESPONSE

Figure 4 illustrates the protection feature responding to a UV event on V_{OUT1}. At time T0, V_{OUT1} has dropped below 75% of the nominal output voltage. Both outputs are quickly shut down and the UGATE and LGATE stop switching immediately, but the fall time of each output is determined by the load and/or short condition on each plus the output capacitance that needs to be discharged. The soft-start function begins producing an internal soft-start ramp. The delay interval, T0 to T1, seen by the output is equivalent to one soft-start cycle. Then a normal soft-start ramp of the output starts, at time T1. At the one-quarter point of the soft-start ramp (not drawn exactly to scale), the good output will have ramped one-quarter way up, while the shorted output will presumably be lower than a quarter (depending on the magnitude of the short). Once the UV comparators are enabled (at the one-quarter point) both outputs will again shut down (if the fault is still present on one of them). Time T2 starts a new internal soft-start cycle, and at T3, starts a new ramp, similar to T1. This time, if we assume the short has gone away, the outputs will ramp up to T4 as they should. If the short has not gone away, then the T0, T1, T2 hiccup mode cycle will keep repeating indefinitely; this cycle time is the equivalent of 1.25

soft-start cycles (1 internal soft-start ramp cycle, plus one-quarter on the next).

If either V_{INx} voltage is not present at startup, that will cause a UV shutdown and restart cycle; similarly, if either V_{INx} is removed after start-up, a shutdown and restart cycle will start when its output drifts down to the UV trip point. But in both cases, once the V_{INx} is restored, the V_{OUTs} will recover on the next soft-start ramp.

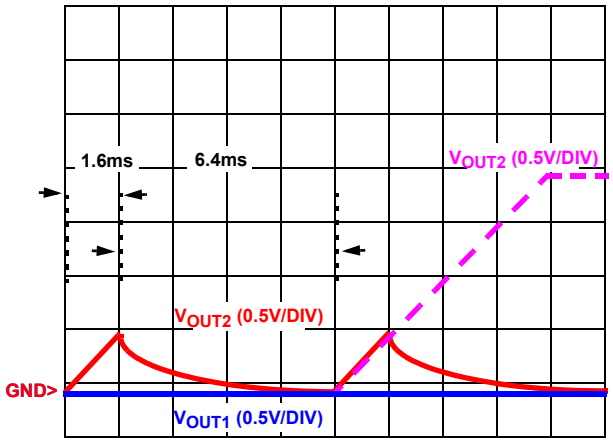


FIGURE 5. UNDERVOLTAGE PROTECTION (SIMULATED BY HAVING NO VIN1 ON POWER-UP)

Figure 5 shows an example of the start-up, with V_{IN1} not powered. V_{OUT2} ramps up one-quarter of the way, at which time the UV comparators are enabled. Since V_{IN1} is not present, V_{OUT1} will not be following the soft-start ramp up, and it will fail the test for UV, shutting down both outputs. It starts an internal delay time-out (equal to one soft-start interval), and then starts a new ramp. For this example, it shows about a 1.6ms ramp up, and 6.4ms off, before the next ramp starts. Thus, the total period of 8ms is based on 1.25 soft-start cycles (one-quarter of the first ramp, and then one full time-out, at a clock period of around 1.6µs) The dotted magenta line shows the case where V_{OUT2} is allowed to ramp all of the way up to 2V.

Switching Frequency

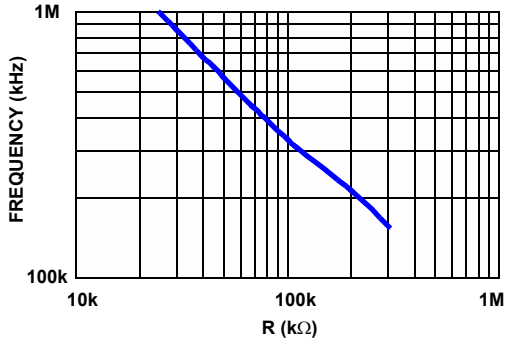


FIGURE 6. FREQUENCY vs FS RESISTOR

The switching frequency of the ISL6549 is determined by the value of the FS resistor. The graph in Figure 6 shows the dependence between the resistor chosen and the resulting switching frequency.

Output Voltage Selection

The output voltage of the PWM converter can be programmed to any level between V_{IN1} and the internal reference, 0.8V. However, even though the ISL6549 can run at near 100% duty cycle at zero load, additional voltage margin is required above V_{IN1} to allow for loading. An external resistor divider is used to scale the output voltage relative to the reference voltage and feed it back to the inverting input of the error amplifier (see Figure 7). A typical value for R1 may be 1.00kΩ (±1% for accuracy), and then R4 (also ±1%) is chosen according to Equation 1:

$$R4 = \frac{R1 \times 0.8V}{V_{OUT1} - 0.8V} \quad \text{(EQ. 1)}$$

R1 is also part of the compensation circuit (see *"PWM Controller Feedback Compensation" on page 10* for more details), so once chosen for that, it should not be changed to adjust V_{OUT1}; only change R4. If the output voltage desired is 0.8V, simply route V_{OUT1} back to the FB pin through R1, but do not populate R4. V_{OUT1} voltages less than the 0.8V reference are not available.

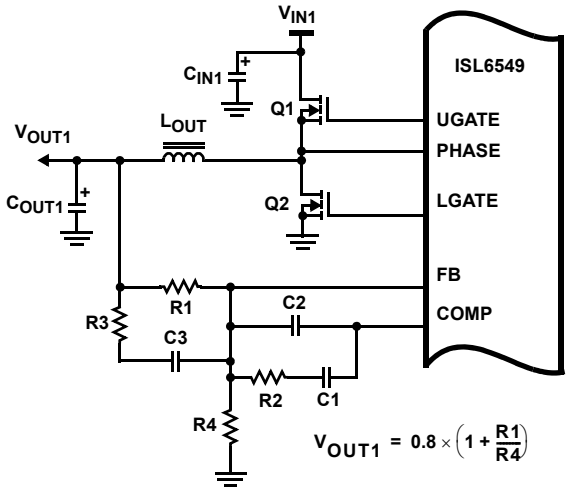


FIGURE 7. OUTPUT VOLTAGE SELECTION OF THE SWITCHER (V_{OUT1})

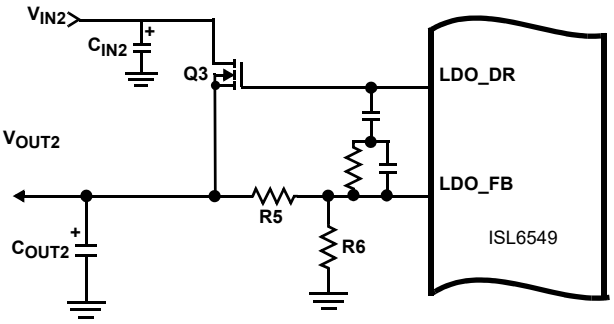
The linear regulator output voltage is also set by means of an external resistor divider as shown in Figure 8. Select a value for R5 (typical 1.00kΩ ±1% for accuracy), and use Equation 2 to calculate R6 (also ±1%), where V_{OUT2} is the desired linear regulator output voltage and V_{REF} is the internal reference voltage, 0.8V. For an output voltage of 0.8V, simply populate R5 with a value less than 5kΩ and do not populate R6. V_{OUT2} voltages less than the 0.8V reference are not available.

$$R6 = \frac{R5 \times 0.8V}{V_{OUT2} - 0.8V} \quad \text{(EQ. 2)}$$

For most situations, no external compensation is required for the linear output. See *"Linear Controller Feedback Compensation" on page 12*.

For both outputs, the selection of 1% resistors may not be able to get the exact ratio desired for any given output voltage. If the output must be defined better, then one option is to place a much bigger resistor in parallel with R4 or R6, to lower its value. For example, a 100kΩ in parallel with a 1.00kΩ yields 990Ω, 1% below 1.00kΩ, which gives finer resolution than the next lower size (976Ω 1%). The big resistor may not have to be 1% tolerance either.

If the linear output is not required, connect the LDO_DR pin directly to LDO_FB pin with no other components. This will terminate the signals and keep the linear from tripping its undervoltage, which would force both outputs into retry.



$$V_{OUT2} = 0.8 \times \left(1 + \frac{R5}{R6}\right)$$

FIGURE 8. OUTPUT VOLTAGE SELECTION OF THE LINEAR (V_{OUT2})

Converter Shutdown

Pulling and holding the FS_DIS pin near GND will shut down both regulators; almost any NFET or other pull-down device (<1kΩ impedance) should work. Upon release of the FS_DIS pin, the regulators enter into a soft-start cycle which brings both outputs back into regulation. The FS_DIS pin requires a quiet GND to minimize jitter. To accomplish this, the FS resistor and any pull-down device should be placed as close as possible to the pin, and the GND should be kept away from the noisy FET GND.

Boot Capacitor, Boot Refresh

A capacitor from the PHASE pin to the BOOT pin is required for the bootstrap circuit for the Upper Gate. The V_{IN1} voltage (and thus the PHASE node) is allowed to go as high as a nominal 12V (±10%) supply. A diode is included on the IC (anode to PVCC5 pin, cathode to BOOT pin), such that the PVCC5 (nominally around 5.25V) will be the bootstrap supply.

In the event that the UGATE is on for an extended period of time, the charge on the boot capacitor can start to sag, raising the $R_{DS(ON)}$ of the upper FET. The ISL6549 has a circuit that detects a long UGATE on-time (32 oscillator clock periods), and forces the LGATE to go high for one oscillator cycle, which allows the bootstrap capacitor time to recharge.

PWM Controller Feedback Compensation

This section highlights the design consideration for a voltage-mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended (see Figure 9).

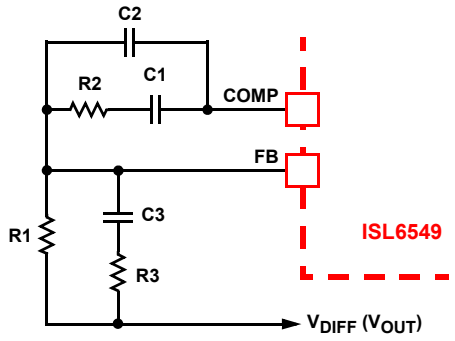


FIGURE 9. COMPENSATION CONFIGURATION FOR ISL6549 CIRCUIT

Figure 10 highlights the voltage-mode control loop for a synchronous-rectified buck converter, applicable to the ISL6549 circuit. The output voltage (V_{OUT}) is regulated to the reference voltage, VREF. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) modified saw-tooth wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor E.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $d_{MAX}V_{IN}/V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis, L and D represent the channel inductance and its DCR, while C and E represents the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2\pi \cdot C \cdot E} \qquad \text{(EQ. 3)}$$

The compensation network consists of the error amplifier (internal to the ISL6549) and the external R1-R3, C1-C3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of F_{SW}) and adequate phase margin (better than 45 degrees). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. The equations that follow relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 10.

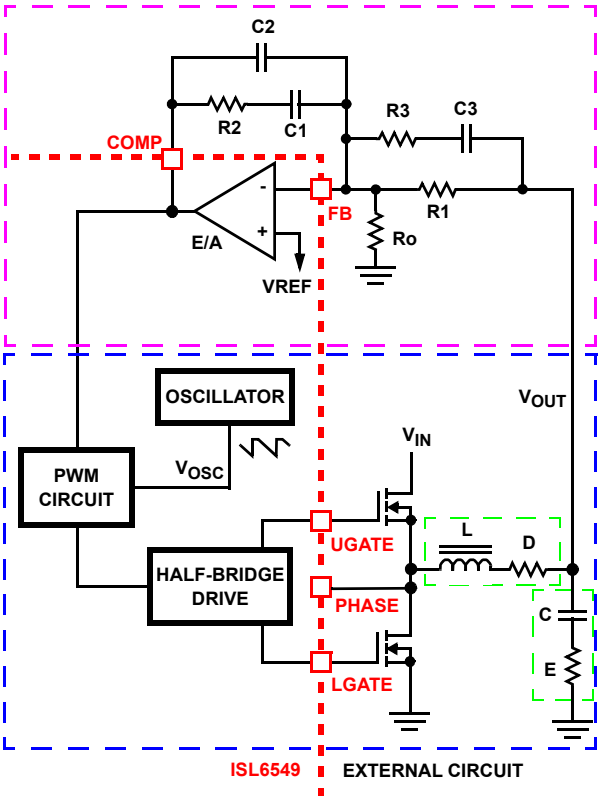


FIGURE 10. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R1 (1kΩ to 5kΩ, typically). Calculate value for R2 for desired converter bandwidth (F_0). If setting the output voltage via an offset resistor connected to the FB pin, Ro in Figure 10, the design procedure can be followed as presented.

$$R2 = \frac{V_{OSC} \cdot R1 \cdot F_0}{d_{MAX} \cdot V_{IN} \cdot F_{LC}} \quad \text{(EQ. 4)}$$

2. Calculate C1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C1 = \frac{1}{2\pi \cdot R2 \cdot 0.5 \cdot F_{LC}} \quad \text{(EQ. 5)}$$

3. Calculate C2 such that F_{P1} is placed at F_{CE}.

$$C2 = \frac{C1}{2\pi \cdot R2 \cdot C1 \cdot F_{CE} - 1} \quad \text{(EQ. 6)}$$

4. Calculate R3 such that F_{Z2} is placed at F_{LC}. Calculate C3 such that F_{P2} is placed below F_{SW} (typically, 0.5 to 1.0 times F_{SW}). F_{SW} represents the switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R3 = \frac{R1}{\frac{F_{SW}}{F_{LC}} - 1} \qquad C3 = \frac{1}{2\pi \cdot R3 \cdot 0.7 \cdot F_{SW}} \quad \text{(EQ. 7)}$$

It is recommended a mathematical model is used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. Equation 8 describes the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{d_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot E \cdot C}{1 + s(f) \cdot (E + D) \cdot C + s^2(f) \cdot L \cdot C}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R2 \cdot C1}{s(f) \cdot R1 \cdot (C1 + C2)} \cdot \frac{1 + s(f) \cdot (R1 + R3) \cdot C3}{(1 + s(f) \cdot R3 \cdot C3) \cdot \left(1 + s(f) \cdot R2 \cdot \left(\frac{C1 \cdot C2}{C1 + C2}\right)\right)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \qquad \text{where, } s(f) = 2\pi \cdot f \cdot j \quad \text{(EQ. 8)}$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R2 \cdot C1} \qquad F_{P1} = \frac{1}{2\pi \cdot R2 \cdot \frac{C1 \cdot C2}{C1 + C2}}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R1 + R3) \cdot C3} \qquad F_{P2} = \frac{1}{2\pi \cdot R3 \cdot C3} \quad \text{(EQ. 9)}$$

Figure 11 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the above guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 11 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

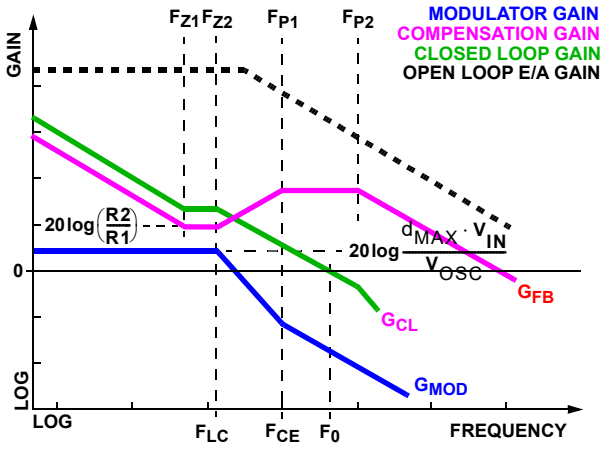


FIGURE 11. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the switching frequency, F_{SW}.

Linear Controller Feedback Compensation

For most situations, no external compensation is required for the linear output. As long as the output capacitor (C_{OUT2}) is large (>100µF) and so is its ESR (>20mW), then it should be stable for loads as low as 10mA up to at least 4A. If smaller values of capacitance and/or ESR are desired, then special considerations may be required to add external compensation (as shown in Figure 8).

Component Selection Guidelines

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equation 10.

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \qquad \text{(EQ. 10)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient (and usually increases the DCR of the inductor, which decreases the efficiency). Increasing the switching frequency (F_{SW}) for a given inductor also reduces the ripple current and voltage.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6549 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equation 11 gives the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 11)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the output voltage setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Output Capacitors Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. And keep in mind that not all applications have the same requirements; some may need many ceramic capacitors in parallel; others may need only one.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate

transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not always a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of upper FET Q1 and the source of lower FET Q2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately half the DC load current. Several electrolytic capacitors may be needed.

Bootstrap Capacitor Selection

The boot diode is internal to the ISL6549, and uses PVCC5 to charge the external boot capacitor. The size of the bootstrap capacitor can be chosen by using the equations in Equation 12.

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V} \quad \text{and} \quad Q_{GATE} = \frac{N \bullet Q_G \bullet V_{IN}}{V_{GS}}$$

where

N is the number of upper FETs

Q_G is the total gate charge per upper FET

V_{IN} is the input voltage

V_{GS} is the gate-source voltage (~5V for ISL6549)

ΔV is the change in boot voltage before and immediately after the transfer of charge; typically 0.7V to 1.0V

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V} = \frac{N \bullet Q_G \bullet V_{IN}}{V_{GS} \bullet \Delta V} = \frac{1 \bullet 33 \bullet 12}{5 \bullet 0.7} = 0.113\mu F \quad \text{(EQ. 12)}$$

The last equation plugs in some typical values: N = 1; Q_G is 33nC, V_{IN} is 12V, V_{GS} is 11V, ΔV_{max} = 1V. In this example, $C_{BOOT} \geq 0.113\mu F$. This value is often rounded to 0.1µF or 0.22µF as a starting value. The bootstrap capacitors for the ISL6549 can usually be rated for 6.3V.

Switcher FET Considerations

The IC was designed for nominal 12V supply for V_{IN1} (drain of upper FET Q1). However, it will work with most any voltage (from other supplies or other regulator outputs) down to around 1V, as long as the input is above the output by a sufficient margin (based on practical duty cycle limitations and upper FET $R_{DS(ON)}$ constraints). For example, although the IC can function at near 100% duty cycle, the voltage drop due to the $R_{DS(ON)}$ of the upper FET at full load current will limit the practical duty cycle to something less than 100%. So the V_{IN1} range is roughly 1.0V up to 12V, with the V_{OUT1} range slightly below it. Therefore, the FETs need to be rated for drain-source breakdown above the V_{IN1} voltage; 20V and 30V ratings are common.

The ISL6549 gate drivers (UGATE and LGATE) were designed to drive up to 2 upper and 2 lower 8 Ld SOIC FETs; when the FETs are properly sized, the output currents can range from under 1A to over 20A. Driving more or bigger FETs is not recommended; even if there is enough current (from the internal PVCC5 regulator), the gate driver waveforms may be degraded. DPAK FET packages can be used, but D^2PAK FETs are not recommended, due to the higher inductance of the package leads. For example, the inductance in the source of the lower FET can create large negative spikes on the PHASE node when the UGATE turns off.

Both the UGATE and LGATE voltages are derived from the internal PVCC5 internal regulator, typically 5.25V. UGATE is only about 5.0V above PHASE, due to the drop in the internal BOOT diode charging the BOOT capacitor; LGATE sees the full 5.25V. So both are considered "5V" drivers; this affects the FET selection in two ways. First, the FET gate-source voltage rating can be as low as 12V (this rating is usually consistent with the 20V or 30V breakdown chosen above). Second, the FETs must have a low threshold voltage (around 1V), in order to have its $R_{DS(ON)}$ rating at V_{GS} = 4.5V in the 10mΩ-20mΩ range. While some FETs are also rated with gate voltages as low as 2.7V, with typical thresholds under 1V, these can cause application problems. As LGATE shuts off the lower FET, it does not take much ringing in the LGATE signal to turn the lower FET back on, while the Upper FET is also turning on, causing some shoot-through current. So avoid FETs with thresholds below 1V.

Another set of important parameters are the turn-on and turn-off times (internal propagation delays, how long before the output starts to switch) and the rise and fall times (external delay to complete the switching). The UGATE and LGATE drivers use an adaptive technique to determine the dead time (when both gate drivers signals are low). Comparators sense when each driver is getting close to GND (such that its FET is close to being off), before turning on the other. This technique minimizes the dead time to the 10ns-20ns range. So if either

FET is particularly slow in these parameters, there is a greater chance that shoot-through current will occur.

As referenced in the “Block Diagram” on page 2, the UGATE signal is referenced to PHASE signal. The deadtime comparator also looks at the difference (UGATE - PHASE). This is significant when viewing the gate driver waveforms on an oscilloscope. One simple indication of shoot-through (or insufficient deadtime) is when the UGATE and LGATE signals overlap. But in this case, one should look at UGATE-PHASE (either by a math function of the two signals, or by using a differential probe measurement) compared to LGATE. Figure 12 shows an example of this. It looks as if the UGATE and LGATE signals have crossed, but the UGATE-PHASE signal does not cross the LGATE.

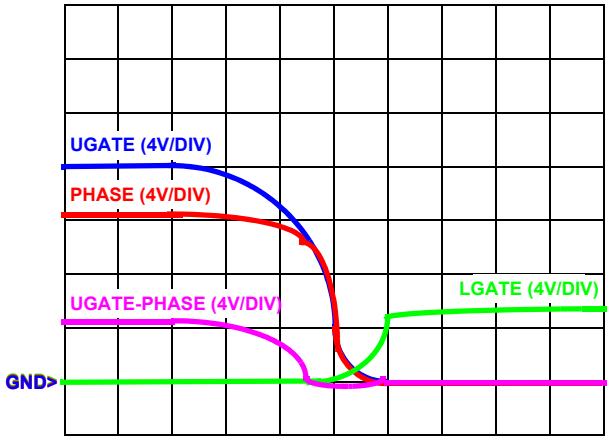


FIGURE 12. GATE DRIVER WAVEFORMS

One important consideration is negative spikes on the PHASE node as it goes low. The upper FET is turning off, but before the lower FET can take over, stray inductance in the layout (on the board, or even the inductance of some components, such as D^2PAK FETs) can contribute to the PHASE going negative.

There is no maximum spec for PHASE spike below GND, however, there is an absolute maximum rating for (BOOT - PHASE) of 7V; exceeding this limit can cause damage to the IC, and possibly to the system. Since the BOOT signal is typically 5V above the PHASE node most of the time, it only takes a few volts of a spike on either signal to exceed the limit. A good design should be characterized by using the math function or differential probe, and monitoring these signals for compliance, especially during full loads, where the signals are usually the noisiest. Slowing down the turn-off of the upper FET may help, while at other times, sometimes the problem may just be the choice of FETs.

If the power efficiency of the system is important, then other FET parameters are also considered. Efficiency is a measure of power losses from input to output, and it contains two major components: losses in the IC (mostly in the gate drivers) and losses in the FETs. Optimizing the sum involves many trade-offs (for example, raising the voltage of the gate drivers typically adds power to the IC side, but may reduce some power on the FET side). For low duty cycle applications (such as 12V in to 1.5V out), the upper FET is usually chosen for low gate charge, since switching losses are key, while the lower FET is chosen for low $R_{DS(ON)}$, since it is on most of the time. For high duty cycles (such as 3.3V in to 2.5V out), the opposite is true.

In summary, the following parameters may need to be considered in choosing the right FETs for an application: drain-source breakdown voltage rating, gate-source rating, maximum current, thermal and package considerations, low gate threshold voltage, gate charge, $R_{DS(ON)}$ at 4.5V, and switching speed. And, of course, the board layout constraints and cost also are factored into the decision.

Linear FET Considerations

The linear FET is chosen primarily for thermal performance. The current for the linear output is generally limited by the power dissipation ($P = (V_{IN2} - V_{OUT2}) * I$), and the FET thermal rating for getting the heat out of the package, and spreading it out on the board, especially when no heatsinks or airflow is available. It is generally not recommended to parallel two FETs in order to get higher current or to spread out the heat, as the FETs would need to be very well-matched in order to share the current properly. Should this approach be desired, and as perfectly matched FETs are seldom available, a small resistor, or PCB trace of suitable resistance placed in the source of each of the FETs can be used to improve the current balance.

The maximum V_{OUT2} voltage allowed is determined by several factors:

- Power dissipation, as described earlier
- Input voltage available
- LDO_DR voltage
- FET chosen

The voltage cannot be any higher than the input voltage available, and the max V_{IN2} is 12V (13.2V for a ±10% supply). The LDO_DR voltage is driven from the VCC12 rail; allowing for headroom, the typical maximum voltage is 11V (lower as VCC12 goes to its minimum of 10.8V). So the maximum output voltage will be at least a V_{GS} drop (which includes the FET threshold voltage) below the 11V, at the maximum load current; some additional headroom is usually needed to handle transient conditions. So a practical typical value around 8V may be possible, but remember to also factor in the variations for worst case conditions on V_{IN2} and the FET parameters. As long as the V_{IN2} is low enough such that headroom versus VCC12 is not a problem, then the maximum output voltage is just below V_{IN2}, based on the $R_{DS(ON)}$ drop at maximum current.

The input supply for V_{IN2} can also be any available supply less than 12V, subject to the considerations above. The drain-source breakdown voltage of the FET should be greater

than the V_{IN2} voltage. The FET's gate-source rating should be greater than 12V (even though the output voltage may not require such a high gate voltage, load transients or other disturbances might force LDO_DR to momentarily approach 12V). The FET threshold is not critical, except for the cases where the LDO_DR headroom is diminished. And finally, the package (and board area allowed) must be able to handle the maximum power dissipation expected.

Application Guidelines

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently at 600kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes the voltage spikes in the converters.

As an example, consider the turn-off transition of the PWM upper MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET and parasitic diode. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimizes the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using the ISL6549. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. Next are the small signal components which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multilayer printed circuit board is recommended. Figure 13 shows the connections of the critical components in the converter. Capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections through vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to the output inductor short. The power plane should support the input and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase node. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the LGATE and UGATE pins to the MOSFET gates should be kept short and wide enough to easily handle the several Amps of drive current.

The critical small signal components include any bypass capacitors, feedback components, and compensation components. Position the bypass capacitors, C_4, C_5, and C_6 close to their pins with a local GND connection, or via directly to the ground plane. R12 should be placed near VCC5 and PVCC5 pins. FS_DIS resistor R7 should be near the FS-DIS pin, and its GND return should be short, and kept away from the noisy FET GND. Place the PWM converter compensation components close to the FB and COMP pins. The feedback resistors for both regulators should also be located as close as possible to the relevant FB pin with vias tied straight to the ground plane as required.

Then the switching components should be placed close to the ISL6549. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible, and make the GND returns (from lower FET source to VIN cap GND) short. Position the output inductor and output capacitors between the upper MOSFET and lower MOSFET and the load.

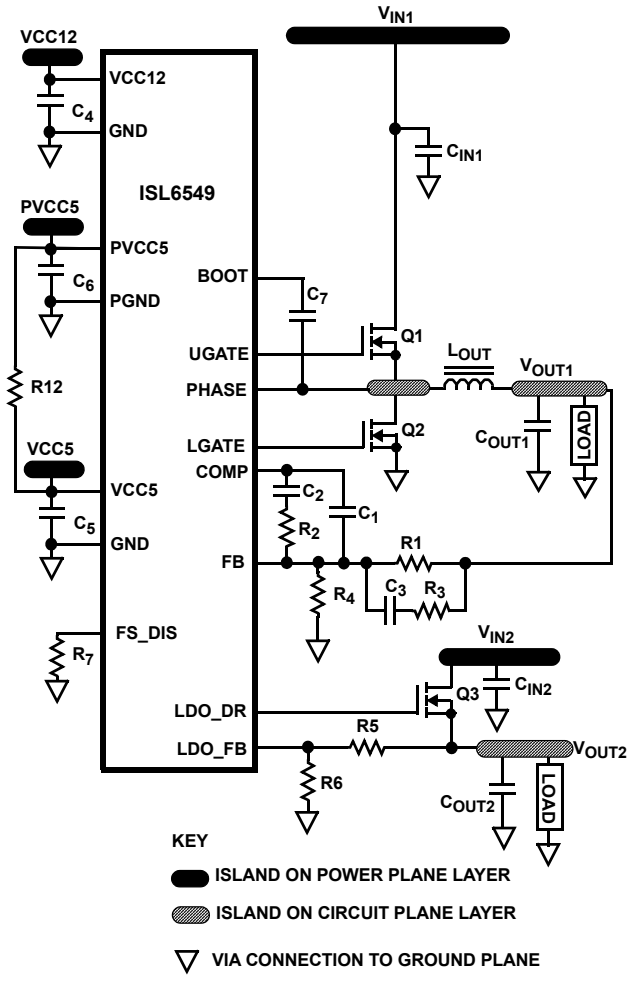
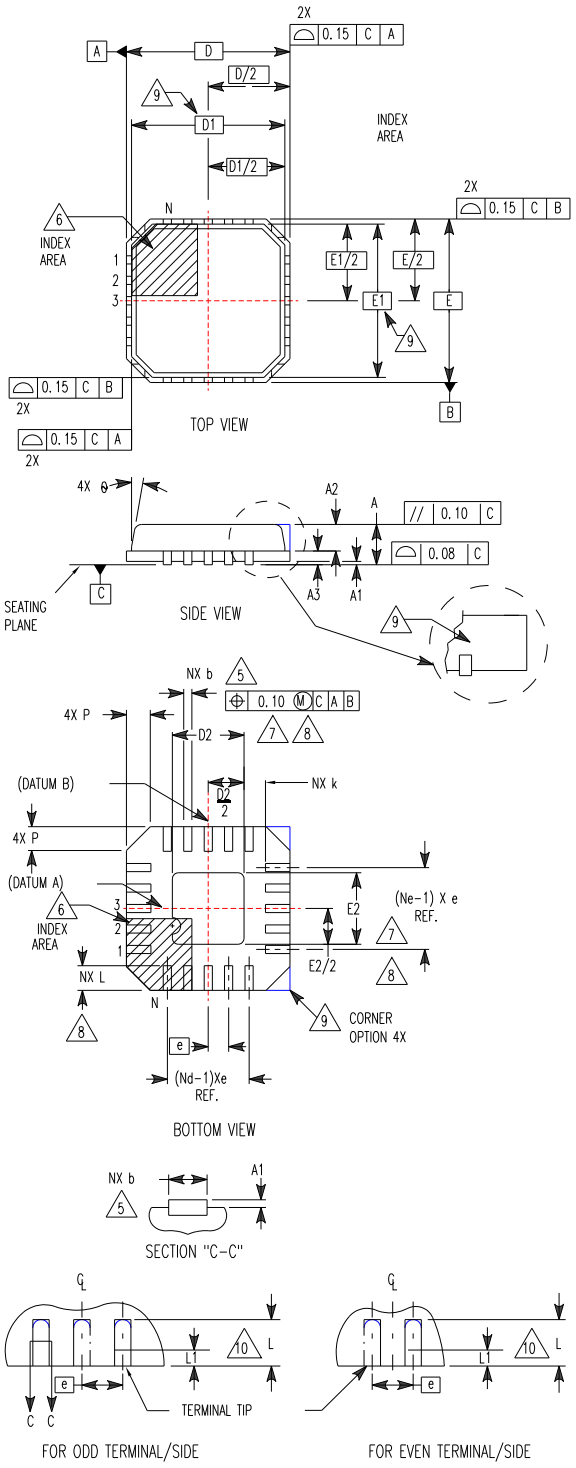


FIGURE 13. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

References

Applications Note: AN1201
Visit us on the internet: www.intersil.com

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

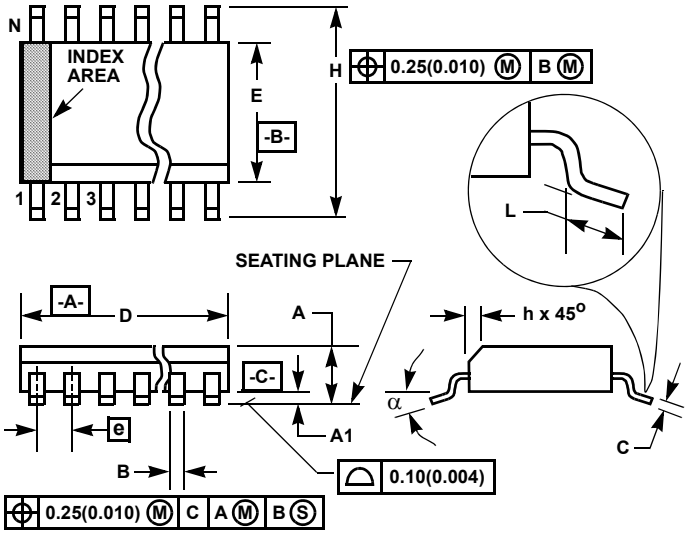
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

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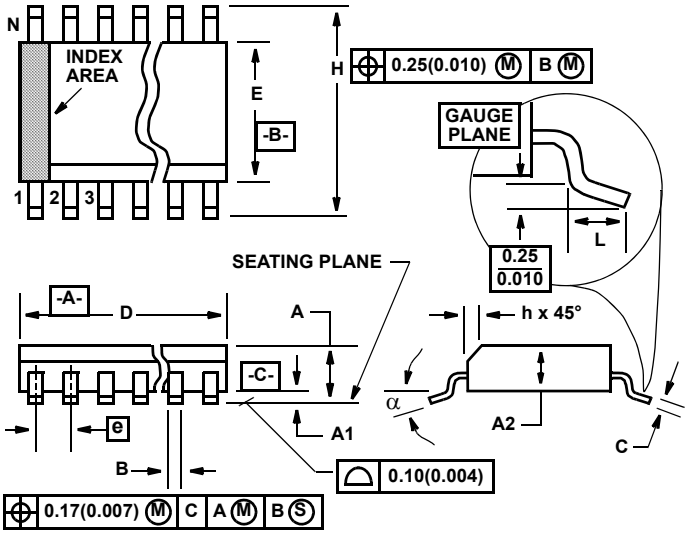
Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



M16.15A

16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150" WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.061	0.068	1.55	1.73	-
A1	0.004	0.0098	0.102	0.249	-
A2	0.055	0.061	1.40	1.55	-
B	0.008	0.012	0.20	0.31	9
C	0.0075	0.0098	0.191	0.249	-
D	0.189	0.196	4.80	4.98	3
E	0.150	0.157	3.81	3.99	4
e	0.025 BSC		0.635 BSC		-
H	0.230	0.244	5.84	6.20	-
h	0.010	0.016	0.25	0.41	5
L	0.016	0.035	0.41	0.89	6
N	16		16		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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