Absolute Maximum Ratings

(Voltages relative to ground.)
Voltage Range on V_{DD} ..... -0.3V to +7.0V
Voltage Range on Any Other Pin ..... -0.3V to +7.0V
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(2.7V ≤ V_{DD} ≤ 5.5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	2.7		5.5	V
Input Logic-High	V_{IH}	(Note 1)	0.7 x V_{DD}		V_{DD}+ 0.5	V
Input Logic-Low	V_{IL}	(Note 1)	-0.5		0.3 x V_{DD}	V
SDA Output Logic-Low Voltage	V_{OL1}	3mA sink current (Note 1)	0		0.4	V
	V_{OL2}	6mA sink current (Note 1)	0		0.6	
O.S. Saturation Voltage	V_{OL}	4mA sink current (Notes 1, 9)			0.8	V
Input Current Each I/O Pin		0.4 < $V_{I/O}$ < 0.9 x V_{DD} (Note 2)	-10		+10	µA
I/O Capacitance	$C_{I/O}$				10	pF
Standby Current	I_{DD1}	(Notes 3, 4)			1	µA
Active Current	I_{DD}	Active temp conversions (Notes 3, 4)			1000	µA
		Communication only (Notes 3, 4)			100	
DIGITAL THERMOMETER						
Thermometer Error	T_{ERR}	-10°C to +85°C (Notes 9, 10)		±0.5	±2.0	°C
		-55°C to +125°C (Notes 9, 10)		±1.0	±3.0	
Resolution			9		12	Bits
Conversion Time	t_{CONVT}	9-bit conversion		125	187.5	ms
		10-bit conversion		250	375	
		11-bit conversion		500	750	
		12-bit conversion		1000	1500	

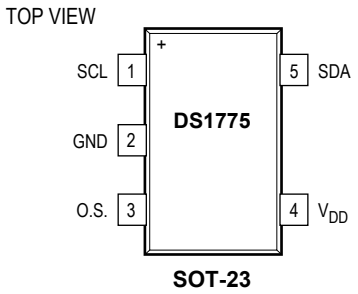
AC Electrical Characteristics-2 Wire Interface

(V_{DD} = 2.7V to 5.5V, T_A = -55°C to +125°C, unless otherwise noted.) (Figure 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode			400	kHz
		Standard mode			100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast mode (Note 5)	0.6			µs
		Standard mode (Note 5)	4.0			
Low Period of SCL	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
High Period of SCL	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Setup Time for a Repeated START	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Data Hold Time	$t_{HD:DAT}$	Fast mode (Note 6)	0		0.9	µs
		Standard mode (Note 6)	0		0.9	
Data Setup Time	$t_{SU:DAT}$	Fast mode (Note 7)	100			ns
		Standard mode (Note 7)	250			
Rise Time of Both SDA and SCL Signals	t_R	Fast mode (Note 8)	20 + 0.1C_B		300	ns
		Standard mode (Note 8)	20 + 0.1C_B		1000	
Fall Time of Both SDA and SCL Signals	t_F	Fast mode (Note 8)	20 + 0.1C_B		300	ns
		Standard mode (Note 8)	20 + 0.1C_B		300	
Setup Time for STOP	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line	C_B	(Note 8)			400	pF
Input Capacitance	C_I			5		pF

Note 1: All voltages are referenced to ground.
Note 2: I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
Note 3: I_{DD} specified with O.S. pin open.
Note 4: I_{DD} specified with V_{DD} at 5.0V and V_{SDA}, V_{SCL} = 5.0V, 0°C to +70°C.
Note 5: After this period, the first clock pulse is generated.
Note 6: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 7: A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.
Note 8: C_B = Total capacitance of one bus line in pF.
Note 9: Internal heating caused by O.S. loading causes the DS1775 to read approximately 0.5°C higher if O.S. is sinking the max rated current.
Note 10: Contact the factory for operation requiring temperature readings greater than +120°C.

Pin Configuration



GND	GROUND
SCL	2-WIRE SERIAL CLOCK
SDA	2-WIRE SERIAL DATA INPUT/OUTPUT
V_{DD}	POWER-SUPPLY VOLTAGE
O.S.	THERMOSTAT OUTPUT SIGNAL

Pin Description

PIN	NAME	FUNCTION
1	SCL	Clock Input/Output for 2-Wire Serial Communication Port. This input should be tied to GND for stand-alone thermostat operation.
2	GND	Ground
3	O.S.	Thermostat Output. Open-drain output becomes active when temperature exceeds T_{OS}. Device configuration defines means to clear overtemperature state.
4	V_{DD}	Supply Voltage 2.7V to 5.5V Input Power Pin
5	SDA	Data Input/Output for 2-Wire Serial Communication Port. In the stand-alone thermostat mode, this input selects hysteresis.

Detailed Description

Figure 1 shows a block diagram of the DS1775. The DS1775 consists of five major components:

1) Precision temperature sensor
2) Analog-to-digital converter
3) 2-wire interface electronics
4) Data registers
5) Thermostat comparator

The factory-calibrated temperature sensor requires no external components. Upon power-up, the DS1775 begins temperature conversions with the default resolution of 9 bits (0.5°C resolution). The host can periodically read the value in the temperature register, which contains the last completed conversion. As conversions are performed in the background, reading the temperature register does not affect the conversion in progress.

In power-sensitive applications, the user can put the DS1775 into a shutdown mode, under which the sensor complete and store the conversion in progress and revert to a low-power standby state. In applications where small incremental temperature changes are critical, the user can change the conversion resolution from 9 bits to 10, 11, or 12. Each additional bit of resolution approximately doubles the conversion time. This is accomplished by programming the configuration register. The configuration register defines the conversion state, thermometer resolution/conversion time, active state of the thermostat output, number of consecutive faults to trigger an alarm condition, and the method to terminate an alarm condition.

The user can also program overtemperature (T_{OS}) and undertemperature (T_{HYST}) setpoints for thermostatic operation. The power-up state of T_{OS} is +80°C and that for T_{HYST} is +75°C. The result of each temperature conversion is compared with the T_{OS} and T_{HYST} setpoints. The DS1775 offers two modes for temperature control, the comparator mode and the interrupt mode. This allows the user the flexibility to customize the condition that would generate and clear a fault condition. Regardless of the mode chosen, the O.S. output becomes active only after the measured temperature exceeds the respective trip-point a consecutive number of times; the number of consecutive conversions beyond the limit to generate an O.S. is programmable. The power-up state of the DS1775 is in the comparator mode with a single fault generating an active O.S.

Digital data is written to/read from the DS1775 via a 2-wire interface, and all communication is MSb first.

Block Diagram

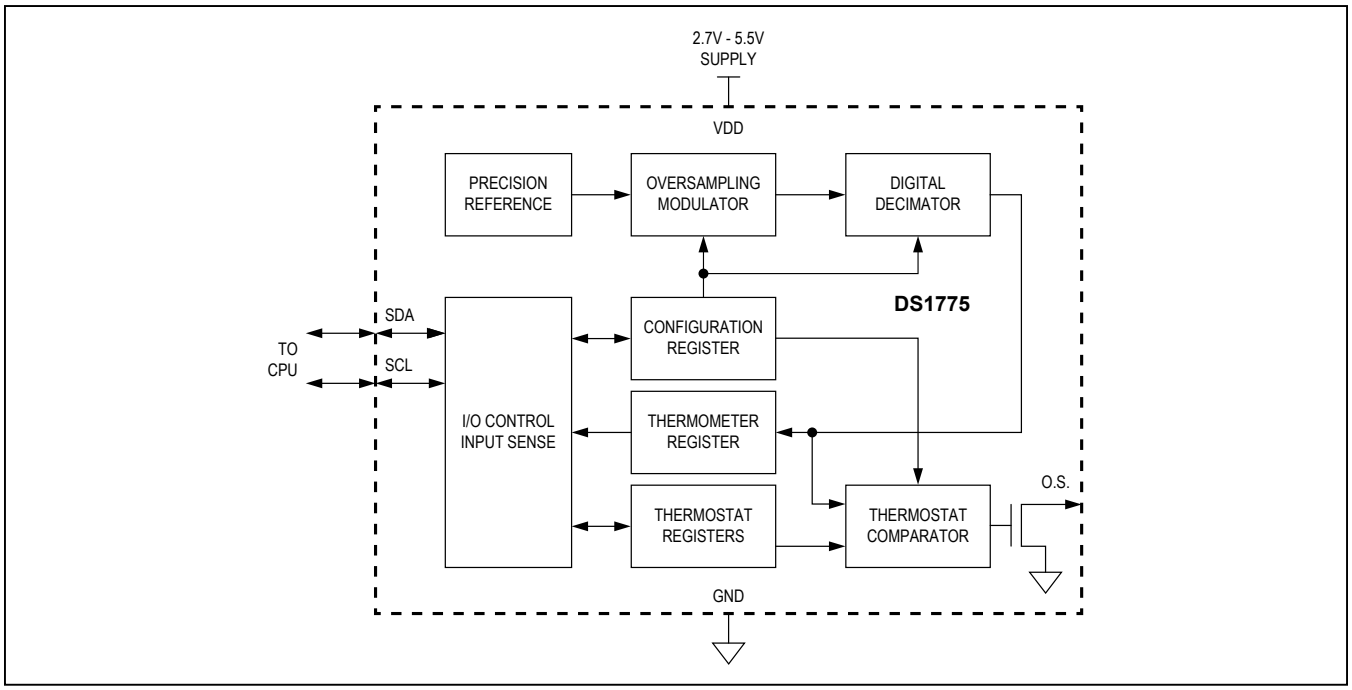


Figure 1. Block Diagram

Operation

Measuring Temperature

The core of DS1775 functionality is its direct-to-digital temperature sensor. The DS1775 measures temperature through the use of an on-chip temperature measurement technique with an operating range from -55°C to +125°C. Temperature conversions are initiated upon power-up, and the most recent result is stored in the thermometer register. Conversions are performed continuously unless the user intervenes by altering the configuration register to put the DS1775 into a shutdown mode. Regardless of the mode used, the digital temperature can be retrieved from the temperature register by setting the pointer to that location (00h, power-up default). The DS1775 power-up default has the sensor automatically performing 9-bit conversions continuously. Details on how to change the settings after power-up are contained in the *Programming* section.

The resolution of the temperature conversion is configurable (9, 10, 11, or 12 bits), with 9-bit readings the default state. This equates to a temperature resolution of 0.5°C, 0.25°C, 0.125°C, or 0.0625°C. Following each conversion, thermal data is stored in the thermometer register in two's complement format; the information can be retrieved over the 2-wire interface with the device pointer set to the temperature register. Table 1 describes the exact relationship of output data to measured temperature. The table assumes the DS1775 is configured for 12-bit resolution; if the device is configured in a lower resolution mode, those bits contain zeros. The data is transmitted serially over the 2-wire serial interface, MSb first. The MSb of the temperature register contains the sign (S) bit, denoting whether the temperature is positive or negative. For Fahrenheit usage, a lookup table or conversion routine must be used.

Thermostat Control

In its comparator operating mode, the DS1775 functions as a thermostat with programmable hysteresis, as shown in Figure 2. When the DS1775's temperature meets or exceeds the value stored in the high temperature trip register (T_{OS}) a consecutive number of times, as defined by the configuration register, the output becomes active and stays active until the first time that the temperature falls below the temperature stored in the low temperature trigger register (T_{HYST}). In this way, any amount of hysteresis may be obtained. The DS1775 powers up in the comparator mode with T_{OS} = +80°C and T_{HYST} = +75°C and can be used as a stand-alone thermostat (no 2-wire interface required) with those setpoints.

In the interrupt mode, the O.S. output first becomes active following the programmed number of consecutive conversions above T_{OS}. The fault can only be cleared by either setting the DS1775 in a shutdown mode or by reading any register (temperature, configuration, T_{OS}, or T_{HYST}) on

Table 1. Temperature/Data Relationships

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	MSB
MSb				(UNIT = °C)			LSb	
2^{-1}	2^{-2}	2^{-3}	2^{-4}	0	0	0	0	LSB

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEX)
+125	0111 1101 0000 0000	7D00h
+25.0625	0000 1010 0010 0000	1910h
+10.125	0000 1010 0010 0000	0A20h
+0.5	0000 0000 1000 0000	0080h
0	0000 0000 0000 0000	0000h
-0.5	1111 1111 1000 0000	FF80h
-10.125	1111 0101 1110 0000	F5E0h
-25.0625	1110 0110 1111 0000	E6F0h
-55	1100 1001 0000 0000	C900h

the device. Following a clear, a subsequent fault can only occur if consecutive conversions fall below T_{HYST}. This interrupt/clear process is thus cyclical (T_{OS}, clear, T_{HYST}, clear, T_{OS}, clear, T_{HYST}, clear, etc.). Only the first of multiple consecutive T_{OS} violations activates O.S., even if each fault is separated by a clearing function. The same situation applies to multiple consecutive T_{HYST} events.

Regardless of the mode chosen, the O.S. output is open-drain and the active state is set in the configuration register. The power-up default is active low. See the *Programming* section for instructions in adjusting the thermostat setpoints, thermostat mode, and O.S. active state.

Programming

There are three areas of interest in programming the DS1775: the configuration register, the T_{OS} register, and the T_{HYST} register. All programming is done via the 2-wire interface by setting the pointer to the appropriate location. Table 2 illustrates the pointer settings for the four registers of the DS1775.

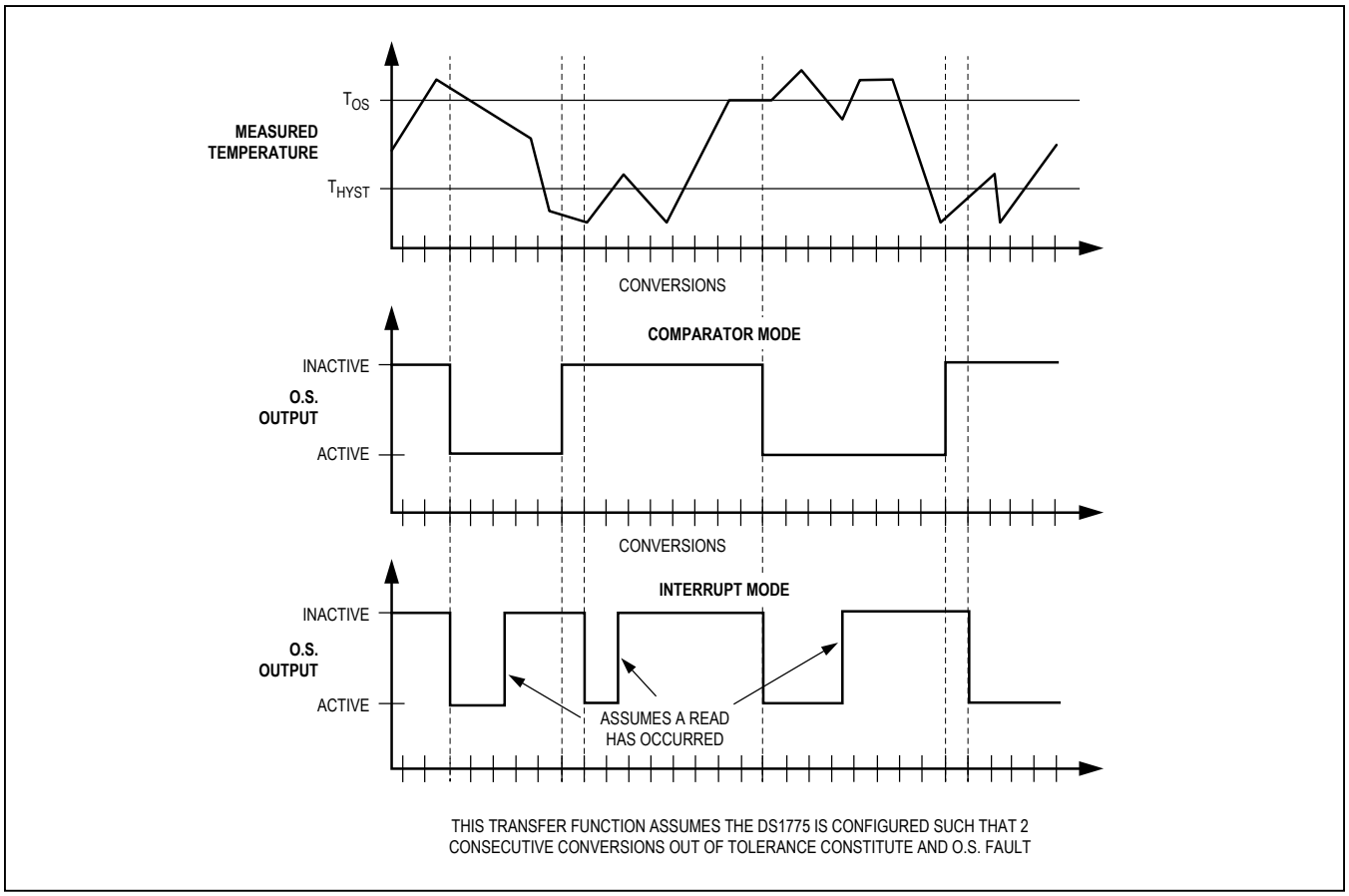


Figure 2. O.S. Output Transfer Function

Table 2. Pointer Register Structure

POINTER	ACTIVE REGISTER
00h	Temperature (default)
01h	Configuration
02h	T_{HYST}
03h	T_{OS}

The DS1775 powers up with the temperature register selected. If the host wishes to change the data pointer, it simply addresses the DS1775 in the write mode (R/$\overline{W}$= 0), receives an acknowledge, and writes the 8 bits that correspond to the new desired location. The last pointer location is always maintained so that consecutive reads from the same register do not require the host to always provide a pointer address. The only exception is at power-up, in which case the pointer is always set to 00h, the temperature register. The pointer address must always precede data in writing to a register, regardless of which address is currently selected. See the *2-Wire Serial Data Bus* section for details of the 2-wire bus protocol.

Configuration Register Programming

The configuration register is accessed if the DS1775 pointer is currently set to the 01h location. Writing to or reading from the register is determined by the R/$\overline{W}$ bit of the 2-wire control byte (see the *2-Wire Serial Data Bus* section). Data is read from or written to the configuration register MSb first. The format of the register is illustrated in Table 3. The effect each bit has on DS1775 functionality is described below along with the power-up state of the bit. The user has read/write access to all bits in the configuration register. The entire register is volatile, and thus it powers up in the default state.

SD = Shutdown bit. If SD is 0, the DS1775 continuously performs temperature conversions and stores the last completed result in the thermometer register. If SD is changed to 1, the conversion in progress is completed and stored; then the device reverts to a low-power standby mode. The O.S. output is cleared if the device is in the interrupt mode and remains unchanged in the comparator mode. The 2-wire port remains active. The power-up default state is 0 (continuous conversion mode).

TM = Thermostat mode. If TM = 0, the DS1775 is in the comparator mode. TM = 1 sets the device to the interrupt mode. See the *Thermostat Control* section for a description of the difference between the two modes. The power-up default state of the TM bit is 0 (comparator mode).

POL = O.S. Polarity Bit. If POL = 1, the active state of the O.S. output is high. A 0 stored in this location sets the thermostat output to an active-low state. The user has read/write access to the POL bit, and the power-up default state is 0 (active low).

F0, F1 = O.S. Fault Tolerance bits. The fault tolerance defines the number of consecutive conversions returning a temperature beyond limits is required to set the O.S. output in an active state. This may be necessary to add margin in noisy environments. Table 4 defines the four settings. The DS1775 powers up with F0 = F1 = 0, such that a single occurrence triggers a fault.

R0, R1 = Thermometer resolution bits. Table 5 defines the resolution of the digital thermometer, based on the settings of these two bits. There is a direct trade-off between resolution and conversion time, as shown in the *AC Electrical Characteristics*. The default state is R0 = 0 and R1 = 0 (9-bit conversions).

Table 3. Configuration/Status Register

0	R1	R0	F1	F0	POL	TM	SD
MSb							LSb

Table 4. Fault Tolerance Configuration

F1	F0	CONSECUTIVE CONVERSIONS BEYOND LIMITS TO GENERATE FAULT
0	0	1
0	1	2
1	0	4
1	1	6

Table 5. Thermometer Resolution Configuration

R1	R0	THERMOMETER RESOLUTION (BITS)	MAX CONVERSION TIME (SECONDS)
0	0	9	0.1875
0	1	10	0.375
1	0	11	0.75
1	1	12	1.5

Thermostat Setpoints Programming

The thermostat registers (T_{OS} and T_{HYST}) can be programmed or read via the 2-wire interface. T_{OS} is accessed by setting the DS1775 data pointer to the 03h location, and to the 02h location for T_{HYST}.

The format of the T_{OS} and T_{HYST} registers is identical to that of the Thermometer register; that is, 12-bit 2's complement representation of the temperature in °C. The user can program the number of bits (9, 10, 11, or 12) for each T_{OS} and T_{HYST} that corresponds to the thermometer resolution mode chosen. For example, if the 9-bit mode is chosen the three least significant bits of T_{OS} and T_{HYST} are ignored by the thermostat comparator. Table 6 shows the format for both T_{OS} and T_{HYST}. The power-up default for T_{OS} is +80°C and for T_{HYST} is +75°C.

If the user does not wish to take advantage of the thermostat capabilities of the DS1775, the 24 bits can be used for general storage of system data that need not be maintained following a power loss.

2-WIRE Serial Data Bus

The DS1775 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1775 operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see Figure 3):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Table 6. Thermostat Setpoint (T_{OS}/T_{HYST}) Format

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	MSB
MSb				(UNIT = °C)			LSb	
2^{-1}	2^{-2}	2^{-3}	2^{-4}	0	0	0	0	LSB

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEX)
+80	0101 0000 0000 0000	5000h
+75	0100 1011 0000 0000	4B00h
+10.125	0000 1010 0010 0000	0A20h
+0.5	0000 0000 1000 0000	0080h
0	0000 0000 0000 0000	0000h
-0.5	1111 1111 1000 0000	FF80h
-10.125	1111 0101 1110 0000	F5E0h
-25.0625	1110 0110 1111 0000	E6F0h
-55	1100 1001 0000 0000	C900h

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1775 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

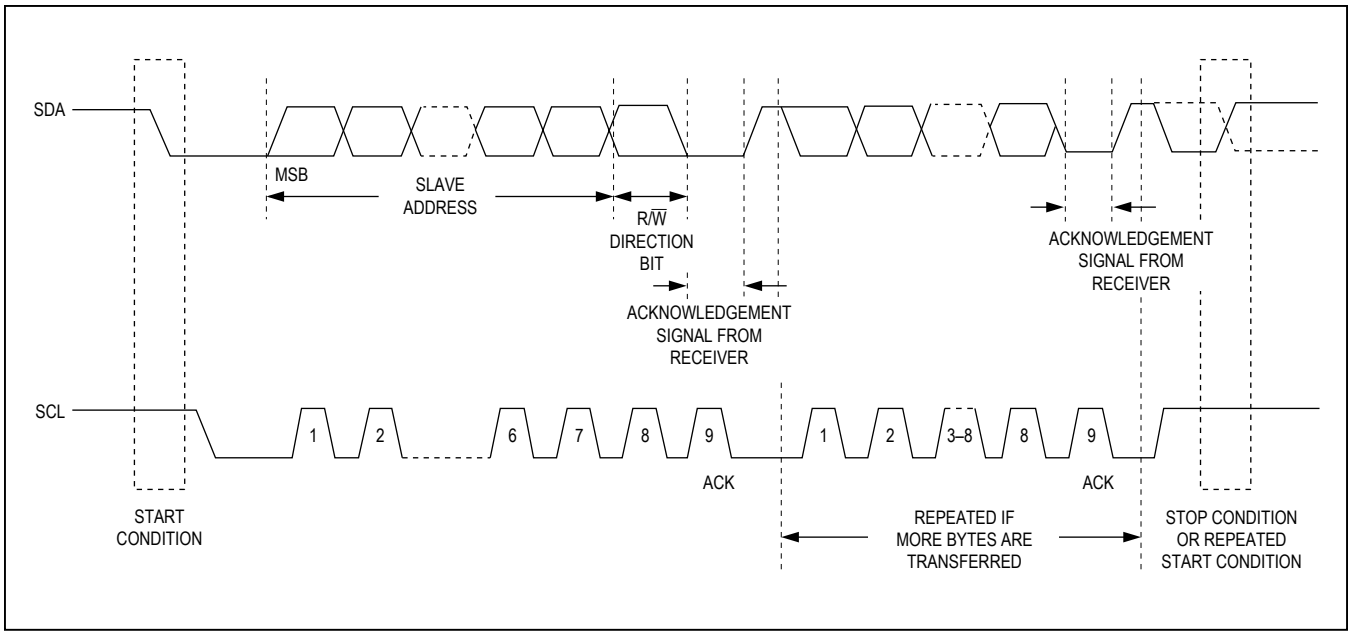


Figure 3. Data Transfer on 2-Wire Serial Bus

Figure 3 details how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The DS1775 can operate in the following two modes:

1) **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2) **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1775 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Slave Address

A control byte is the first byte received following the START condition from the master device. The control byte consists of a 4-bit control code; for the DS1775, this is set as 1001 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). These bits are set to 000 (A2 = 0, A1 = 0, A0 = 0) for the DS1775R and vary according to the device's part number as specified in the *Ordering Information* table. They are used by the master device to select which of eight devices are to be accessed. The set bits are in effect the three least significant bits of the slave address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a 1 a read operation is selected; when set to a 0 a write operation is selected. Following the START condition, the DS1775 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1001 code and appropriate device select bits of 000, the DS1775 outputs an acknowledge signal on the SDA line. See Figure 4.

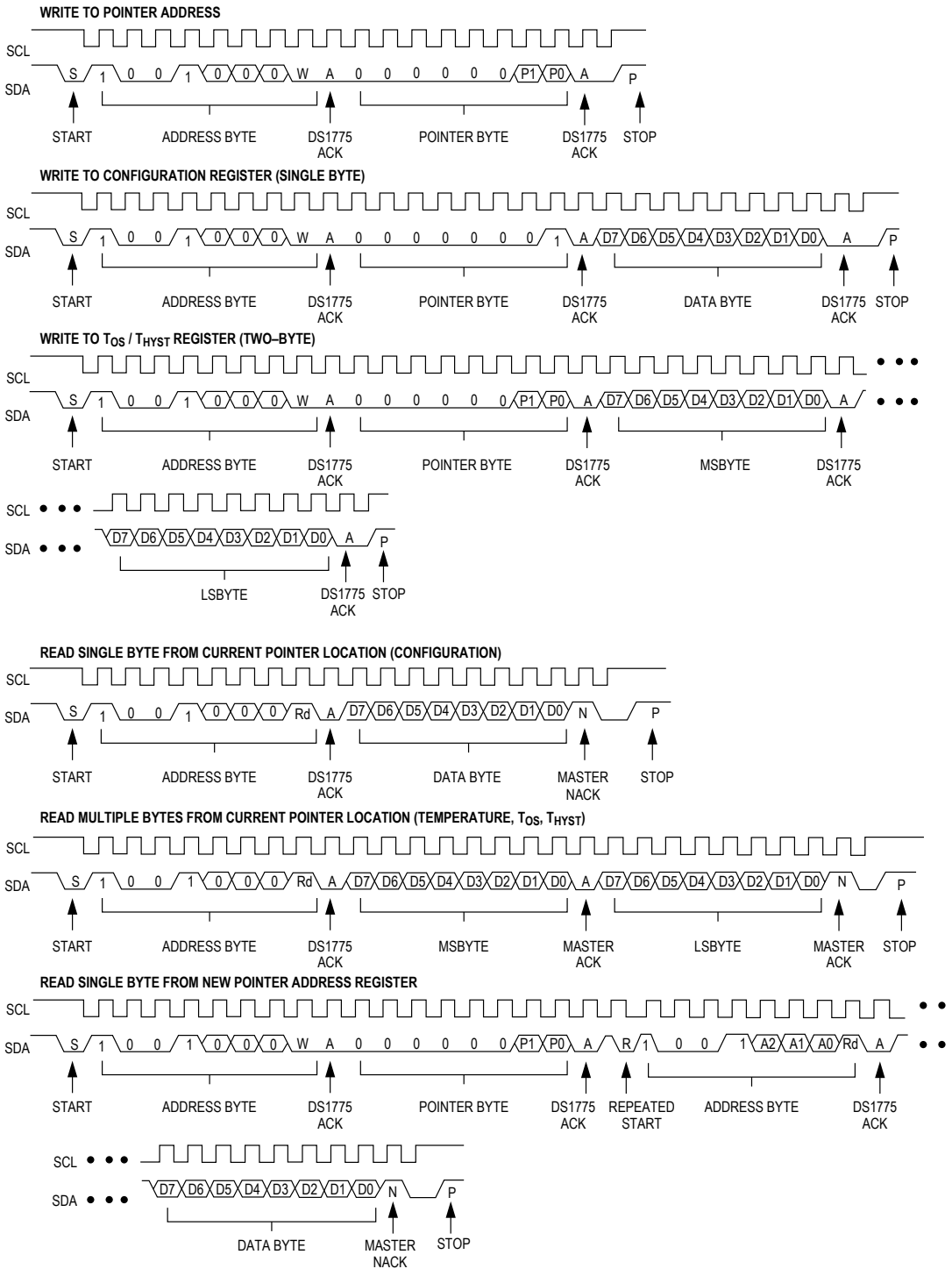


Figure 4. 2-Wire Serial Communication with DS1775

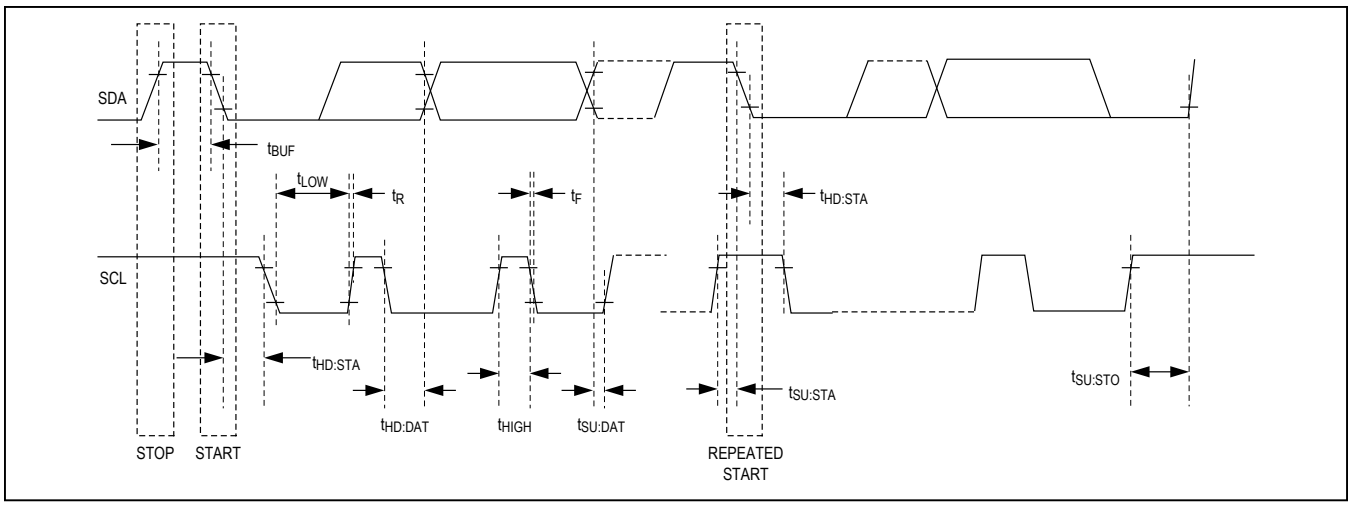


Figure 5. Timing Diagram

Ordering Information

PART	ADDRESS	TOP MARK	TEMP RANGE	PIN-PACKAGE
DS1775R+U	000	7750	-55°C to +125°C	5 SOT23
DS1775R+T&R				
DS1775R1+U	001	7751	-55°C to +125°C	5 SOT23
DS1775R1+T&R				
DS1775R2+U	010	7752	-55°C to +125°C	5 SOT23
DS1775R2+T&R				
DS1775R3+U	011	7753	-55°C to +125°C	5 SOT23
DS1775R3+T&R				
DS1775R4+U	100	7754	-55°C to +125°C	5 SOT23
DS1775R4+T&R				
DS1775R5+U	101	7755	-55°C to +125°C	5 SOT23
DS1775R5+T&R				
DS1775R6+U	110	7756	-55°C to +125°C	5 SOT23
DS1775R6+T&R				
DS1775R7+U	111	7757	-55°C to +125°C	5 SOT23
DS1775R7+T&R				

+Denotes a lead(Pb)-free/RoHS-compliant package.
U = Cut tape.
T&R = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SOT23	U5+1	21-0057	90-0174

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	5/13	Updated the *Absolute Maximum Ratings*, *Ordering Information*, *Package Information* sections	12, 13
2	11/16	Added typical specification to the *Thermometer Error* parameter in the *Electrical Characteristics* table and added *Thermometer Error (TERR)* typical spec in the *Electrical Characteristics* table.	2

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