Low-Power, Serial, 14-Bit DACs with Voltage Output

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND .....-0.3V to +6.0V
AGND to DGND.....-0.3V to +0.3V
Digital Inputs to DGND.....-0.3V to +6.0V
DOUT, UPO to DGND .....-0.3V to (V_{DD} + 0.3V)
OUT, REF to AGND .....-0.3V to (V_{DD} + 0.3V)
OS to AGND .....(AGND - 4.0V) to (V_{DD} + 0.3V)
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5170

(V_{DD} = +5V ±10%, V_{REF} = 2.5V, OS = AGND = DGND, R_L = 5kΩ, C_L = 100pF referenced to ground, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			14			Bits
Integral Nonlinearity (Note 1)	INL	MAX5170A			±1	LSB
		MAX5170B			±2	
Differential Nonlinearity	DNL				±1	LSB
Offset Error (Note 2)	V_{OS}				±10	mV
Gain Error	GE	R_L = ∞		-0.6	±4	LSB
		R_L = 5kΩ		-1.6	±8	
Power-Supply Rejection Ratio	PSRR			10	120	µV/V
Output Noise Voltage		f = 100kHz		1		LSBp-p
Output Thermal Noise Density				80		nV/√Hz
REFERENCE						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}		18			kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.5Vp-p + 1.5V_{DC}, slew-rate limited		350		kHz
Reference Feedthrough		V_{REF} = 3.6Vp-p + 1.8V_{DC}, f = 1kHz, code = all 0s		-80		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1.5 Vp-p + 1.5V_{DC}, f = 10kHz, code = 3FFF hex		82		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		3			V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{DD}		0.001	±1	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V

ELECTRICAL CHARACTERISTICS—MAX5170 (continued)

(V_{DD} = +5V ±10%, V_{REF} = 2.5V, OS = AGND = DGND, R_L = 5kΩ, C_L = 100pF referenced to ground, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±0.5LSB, from 10mV to full-scale		18		µs
Output Voltage Swing (Note 3)			0		V_{DD}	V
OS Pin Input Resistance			80	120		kΩ
Time Required to Exit Shutdown				40		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{SCLK} = 100kHz, V_{SCLK} = 5Vp-p		1		nV-s
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		4.5		5.5	V
Power-Supply Current (Note 4)	I_{DD}			0.28	0.4	mA
Shutdown Current (Note 4)				1	10	µA
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{DO1}	C_{LOAD} = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO2}	C_{LOAD} = 200pF			80	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Low-Power, Serial, 14-Bit DACs with Voltage Output

ELECTRICAL CHARACTERISTICS—MAX5172

(V_{DD} = +2.7V to +3.6V, V_{REF} = 1.25V, OS = AGND = DGND, R_L = 5kΩ, C_L = 100pF referenced to ground, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			14			Bits
Integral Nonlinearity (Note 5)	INL	MAX5172A			±2	LSB
		MAX5172B			±4	
Differential Nonlinearity	DNL				±1	LSB
Offset Error (Note 2)	V_{OS}				±10	mV
Gain Error	GE	R_L = ∞		-0.6	±4	LSB
		R_L = 5kΩ		-1.6	±8	
Power-Supply Rejection Ratio	PSRR			10	120	µV/V
Output Noise Voltage		f = 100kHz		2		LSBp-p
Output Thermal Noise Density				80		nV/√Hz
REFERENCE						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}		18			kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.5Vp-p + 0.75V_{DC}, slew-rate limited		350		kHz
Reference Feedthrough		V_{REF} = 1.6Vp-p + 0.8V_{DC}, f = 1kHz, code = all 0s		-80		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 0.6Vp-p + 0.9V_{DC}, f = 10kHz, code = 3FFF hex		78		dB
DIGITAL INPUT						
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{DD}		0.001	±1	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUT						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V

ELECTRICAL CHARACTERISTICS—MAX5172 (continued)

(V_{DD} = 2.7V to 3.6V, V_{REF} = 1.25V, OS = AGND = DGND, R_L = 5kΩ, C_L = 100pF referenced to ground, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±0.5LSB from 10mV to full-scale		18		µs
Output Voltage Swing (Note 3)			0		V_{DD}	V
OS Pin Input Resistance			80	120		kΩ
Time Required to Exit Shutdown				40		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{SCLK} = 100kHz, V_{SCLK} = 3Vp-p		1		nV-s
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		2.7		3.6	V
Power-Supply Current (Note 4)	I_{DD}			0.28	0.4	mA
Shutdown Current (Note 4)				1	10	µA
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}		150			ns
SCLK Pulse Width High	t_{CH}		75			ns
SCLK Pulse Width Low	t_{CL}		75			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS}		60			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		60			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{DO1}	C_{LOAD} = 200pF			200	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO2}	C_{LOAD} = 200pF			200	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		75			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		150			ns

Note 1: INL guaranteed between codes 40 and 16383.
Note 2: Offset is measured at the code that comes closest to 10mV.
Note 3: Accuracy is better than 1.0 LSB for V_{OUT} = 10mV to V_{DD} - 180mV. Guaranteed by PSR test on end points.
Note 4: R_L = open and digital inputs are either V_{DD} or DGND.
Note 5: INL guaranteed between codes 80 and 16383.

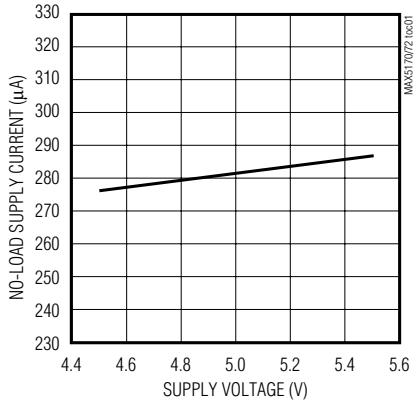
Low-Power, Serial, 14-Bit DACs with Voltage Output

Typical Operating Characteristics

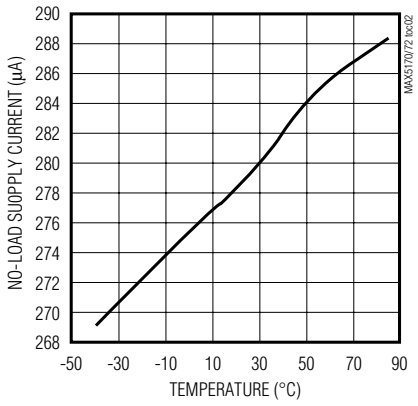
(MAX5170: V_{DD} = +5V, V_{REF} = 2.5V; MAX5172: V_{DD} = +3V, V_{REF} = 1.25V; C_L = 100pF, OS = AGND, code = 3FFF hex, T_A = +25°C, unless otherwise noted.)

MAX5170

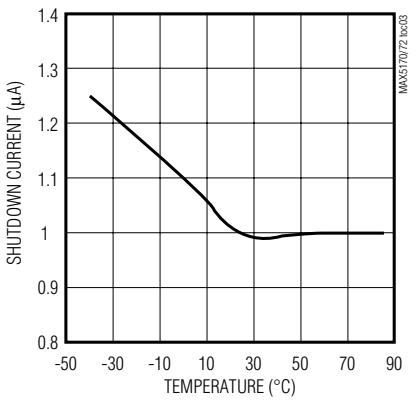
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



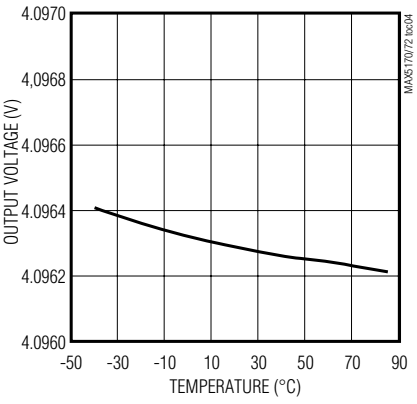
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



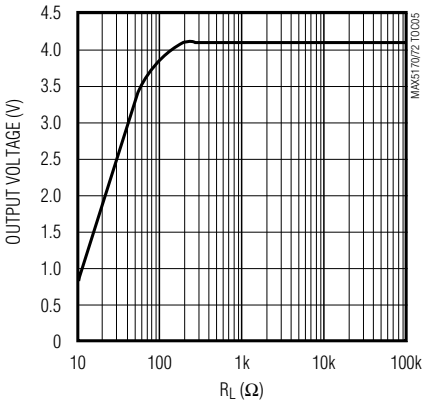
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



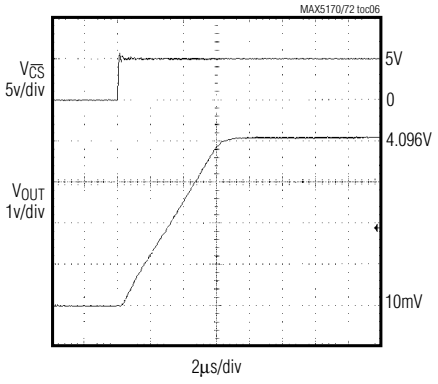
OUTPUT VOLTAGE vs. TEMPERATURE



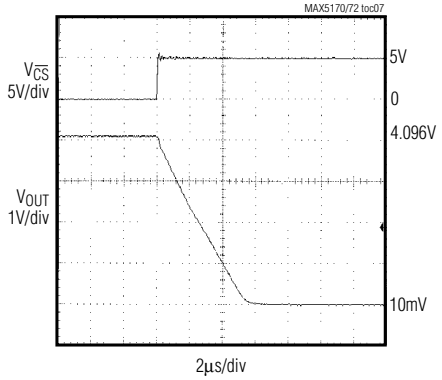
OUTPUT VOLTAGE vs. LOAD RESISTANCE



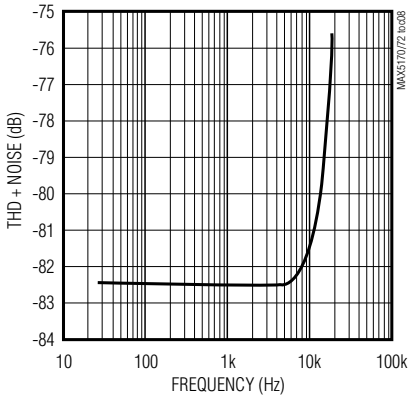
DYNAMIC RESPONSE



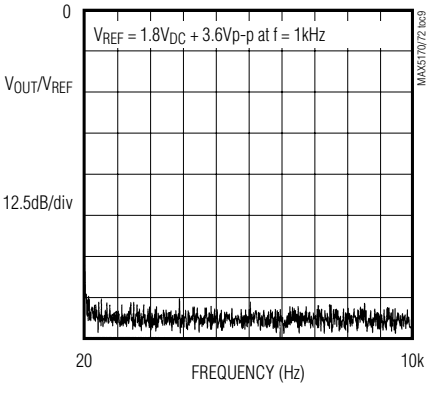
DYNAMIC RESPONSE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



REFERENCE FEEDTHROUGH

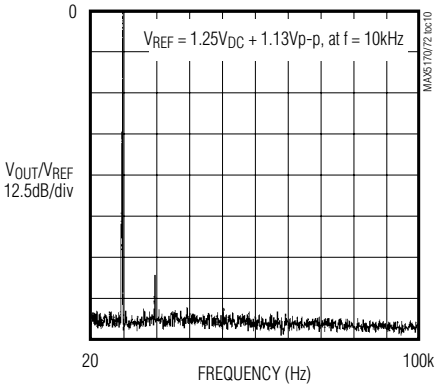


Typical Operating Characteristics (continued)

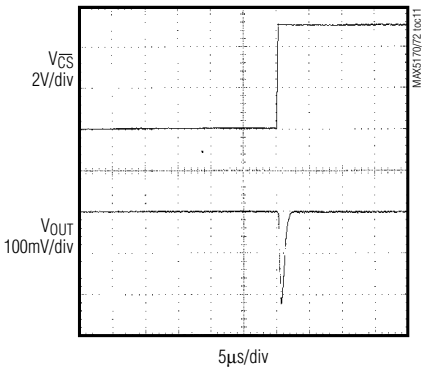
(MAX5170: V_{DD} = +5V, V_{REF} = 2.5V; MAX5172: V_{DD} = +3V, V_{REF} = 1.25V; C_L = 100pF, OS = AGND, code = 3FFF hex, T_A = +25°C, unless otherwise noted.)

MAX5170

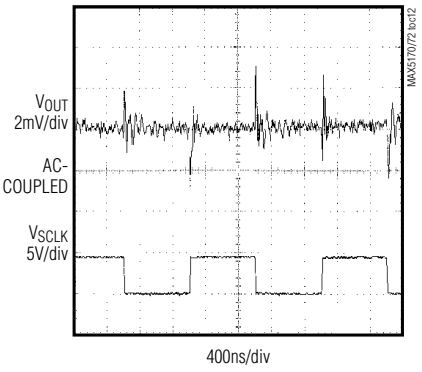
FFT PLOT



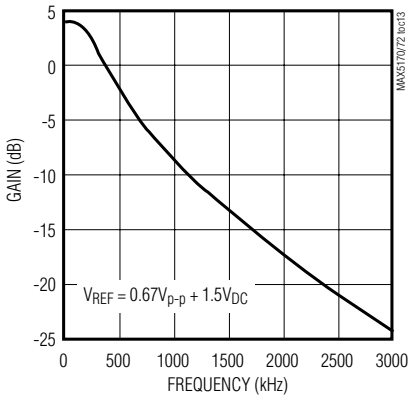
MAJOR-CARRY TRANSITION



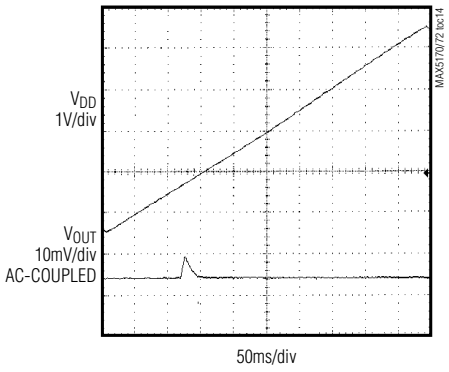
DIGITAL FEEDTHROUGH



REFERENCE INPUT FREQUENCY RESPONSE

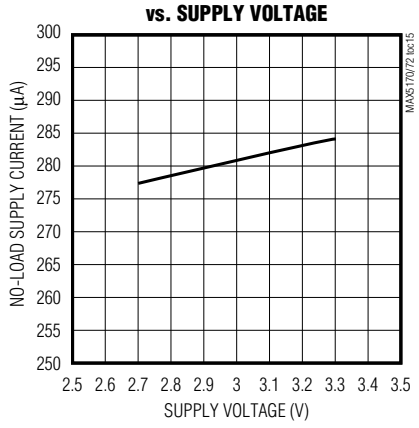


START-UP GLITCH

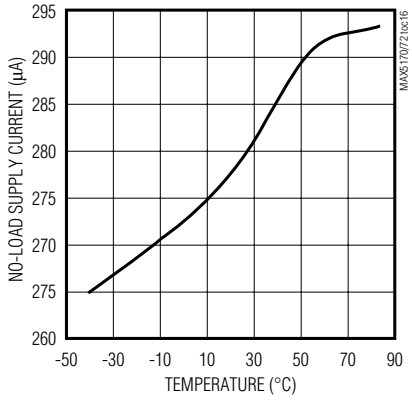


MAX5172

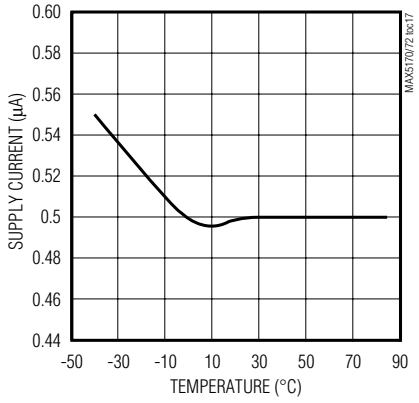
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



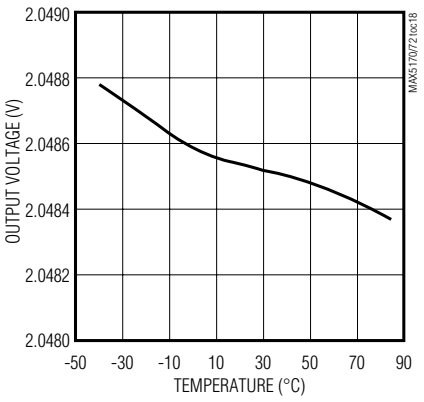
Low-Power, Serial, 14-Bit DACs with Voltage Output

Typical Operating Characteristics (continued)

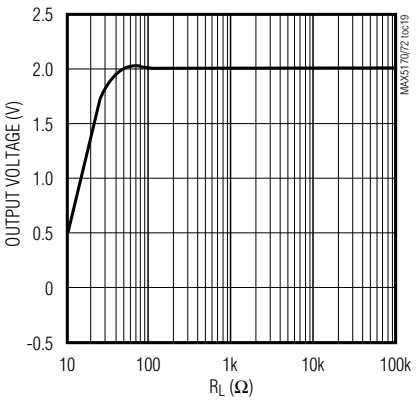
(MAX5170: V_{DD} = +5V, V_{REF} = 2.5V; MAX5172: V_{DD} = +3V, V_{REF} = 1.25V; C_L = 100pF, OS = AGND, code = 3FFF hex, T_A = +25°C, unless otherwise noted.)

MAX5172

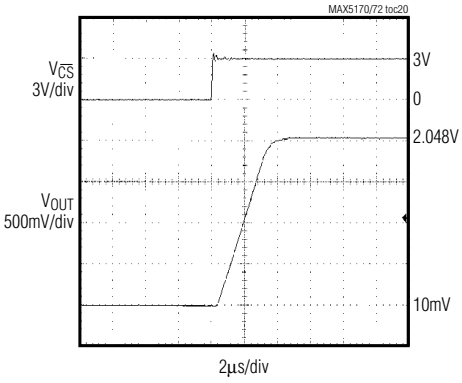
OUTPUT VOLTAGE vs. TEMPERATURE



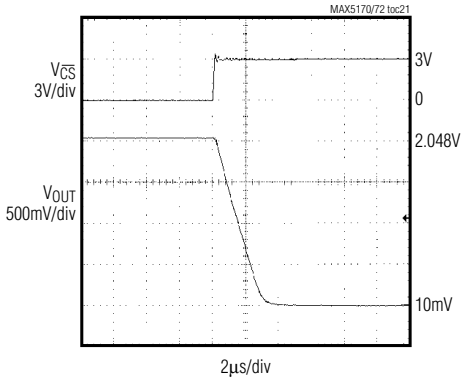
OUTPUT VOLTAGE vs. LOAD RESISTANCE



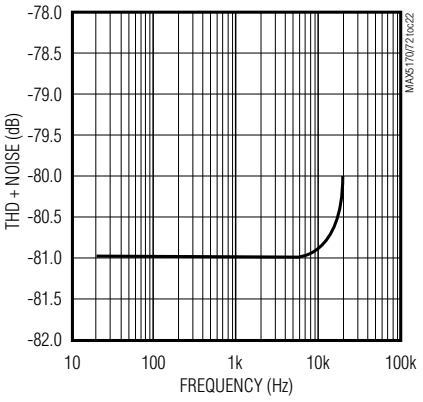
DYNAMIC RESPONSE



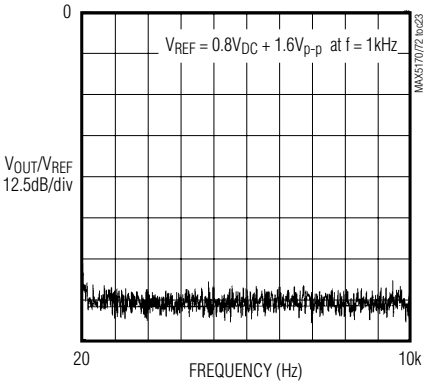
DYNAMIC RESPONSE



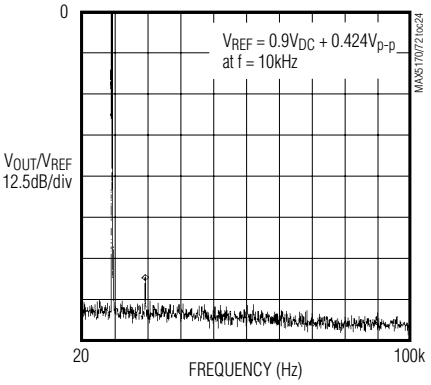
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



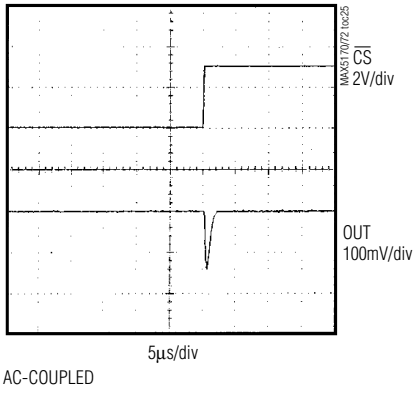
REFERENCE FEEDTHROUGH



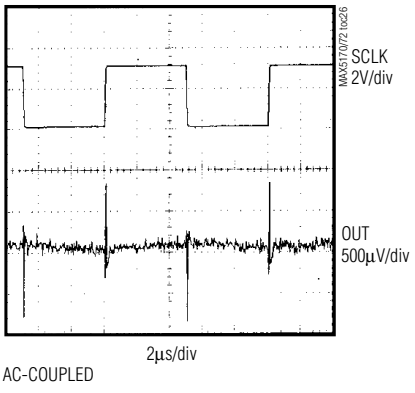
FFT PLOT



MAJOR-CARRY TRANSITION



DIGITAL FEEDTHROUGH (SCLK, OUT)

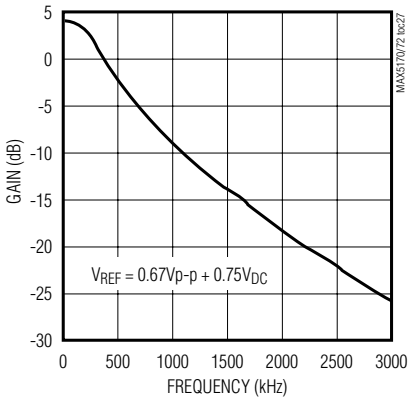


Typical Operating Characteristics (continued)

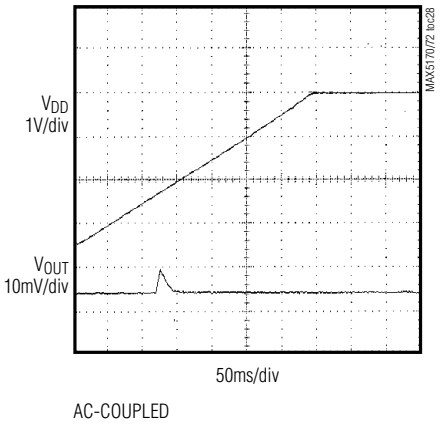
(MAX5170: V_{DD} = +5V, V_{REF} = 2.5V; MAX5172: V_{DD} = +3V, V_{REF} = 1.25V; C_L = 100pF, OS = GND, code = 3FFF hex, T_A = +25°C, unless otherwise noted.)

MAX5172

REFERENCE INPUT FREQUENCY RESPONSE



START-UP GLITCH



Pin Description

PIN	NAME	FUNCTION
1	OS	Offset Adjustment. Connect to AGND for no offset.
2	OUT	Voltage Output. High impedance when in shutdown. The output voltage is limited to V_{DD}.
3	RS	Reset Mode Select (digital input). Connect to V_{DD} to select midscale reset output voltage. Connect to DGND to select 0 reset output voltage.
4	$\overline{PDL}$	Power-Down Lockout (digital input). Connect to V_{DD} to allow shutdown. Connect to DGND to disable software and hardware shutdown.
5	$\overline{CLR}$	Clear DAC (digital input). Clears the DAC to either zero or midscale as determined by RS.
6	$\overline{CS}$	Chip Select Input (digital input). DIN ignored when $\overline{CS}$ is high.
7	DIN	Serial-Data Input (digital input). Data is clocked in on the rising edge of SCLK.
8	SCLK	Serial Clock Input (digital input)
9	DGND	Digital Ground
10	DOUT	Serial-Data Output
11	UPO	User-Programmable Output. State is set by the serial input.
12	SHDN	Shutdown (digital input). Pulling SHDN high when $\overline{PDL}$ = V_{DD} places the chip in shutdown with a maximum shutdown current of 10µA.
13	AGND	Analog Ground
14	REF	Reference Input. Maximum V_{REF} is V_{DD} - 1.4V.
15	N.C.	No Connection
16	V_{DD}	Positive Supply. Bypass to AGND with a 4.7µF capacitor in parallel with a 0.1µF capacitor.

Low-Power, Serial, 14-Bit DACs with Voltage Output

Detailed Description

The MAX5170/MAX5172 14-bit, serial, voltage-output DACs operate with a 3-wire serial interface. These devices include a 16-bit shift register and a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition, these devices employ a rail-to-rail output amplifier and internally trimmed resistors to provide a gain of +1.638V/V, maximizing the output voltage swing. The MAX5170/MAX5172's offset adjust pin allows for a DC shift in the DAC output. The DACs are designed with an inverted R-2R ladder network (Figure 1) which produces a weighted voltage proportional to the reference voltage.

Reference Inputs

The reference input accepts both AC and DC values with a voltage range extending from 0 to V_{DD} - 1.4V. The following equation represents the resulting output voltage:

$$V_{OUT} = \frac{V_{REF} \times N \times Gain}{16384}$$

where N is the numeric value of the DAC's binary input code (0 to 16383), V_{REF} is the reference voltage, and Gain is the internal set voltage gain (+1.638V/V if OS = AGND). The maximum output voltage is V_{DD}. The reference pin has a minimum impedance of 18kΩ and is code dependent.

Output Amplifier

With OS connected to AGND, the output amplifier employs an internal, trimmed resistor-divider setting the gain to +1.638V/V and minimizing gain error. The output amplifier has a typical slew rate of 0.6V/µs and settles to ±0.5LSB from a full-scale transition within 18µs, when loaded with 5kΩ in parallel with 100pF. Loads less than 2kΩ degrade performance.

For alternative output amplifier setups, refer to the *Applications Information* section.

Shutdown Mode

The MAX5170/MAX5172 feature a software- and hardware-programmable shutdown mode that reduces the typical supply current to 1µA. Enter shutdown by writing the appropriate input-control word as shown in Table 1 or by using the hardware shutdown. In shutdown mode, the reference input and the amplifier output become high-impedance and the serial interface remains active. Data in the input register is saved, allowing the MAX5170/MAX5172 to recall the prior output state when returning to normal operation. Exit shutdown by reloading the DAC register from the shift register, by simultaneously loading the input and DAC registers, or by toggling $\overline{PDL}$. When returning from shutdown, wait 40µs for the output to settle.

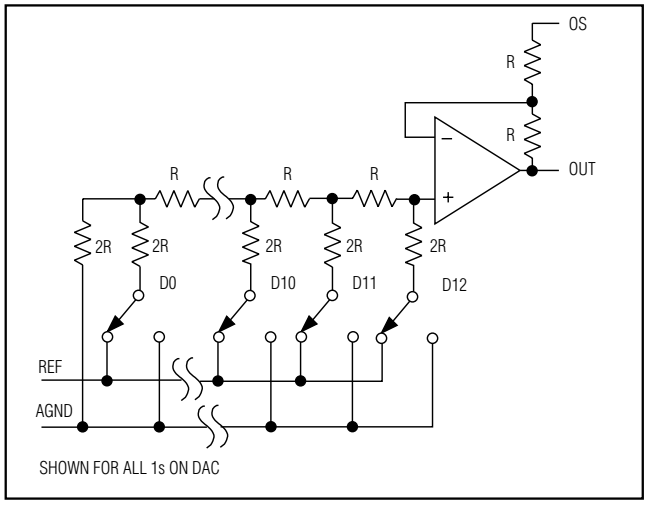


Figure 1. Simplified DAC Circuit Diagram

Power-Down Lockout

Power-Down Lockout disables the software/hardware shutdown mode. A high-to-low transition brings the device out of shutdown and returns the output to its previous state.

Shutdown

Pulling SHDN high while $\overline{PDL}$ is high places the MAX5170/MAX5172 in shutdown. Pulling SHDN low will not return the device to normal operation. A high-to-low transition on $\overline{PDL}$ or an appropriate command from the serial data line (see Table 1 for commands) is required to exit shutdown.

Serial-Interface

The MAX5170/MAX5172 3-wire serial interface is compatible with SPI, QSPI (Figure 2) and MICROWIRE (Figure 3) interface standards. The 16-bit serial input word consists of two control bits and 14 bits of data (MSB to LSB).

The control bits determine the MAX5170/MAX5172's operation as outlined in Table 1. The MAX5170/MAX5172's digital inputs are double buffered, which allows any of the following:

- Loading the input register without updating the DAC register
- Updating the DAC register from the input register
- Updating the input and DAC registers simultaneously.

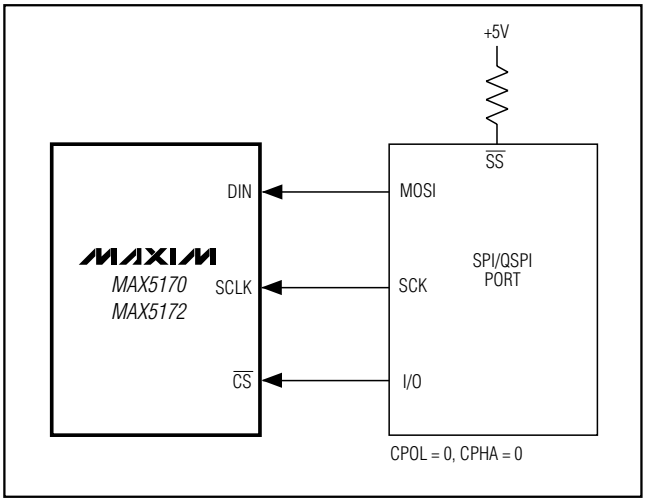


Figure 2. Connections for SPI and QSPI Interface

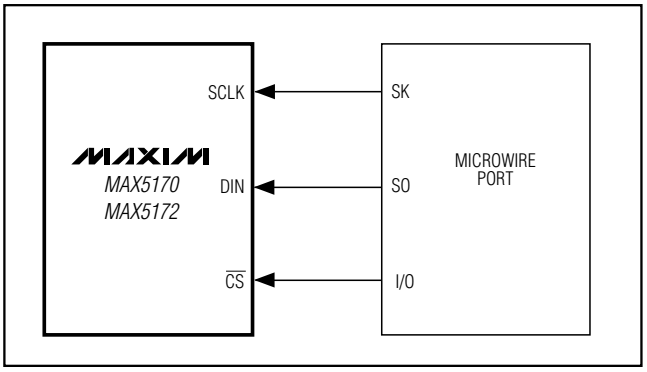


Figure 3. Connections for MICROWIRE Interface Standards

The MAX5170/MAX5172 accepts one 16-bit packet or two 8-bit packets sent while $\overline{CS}$ remains low. The MAX5170/MAX5172 allow the following to be configured:

- Clock edge on which serial data output (DOUT) is clocked out
- State of the user-programmable logic output
- Configuration of the reset state.

Specific commands for setting these are shown in Table 1.

The general timing diagram in Figure 4 illustrates how the MAX5170/MAX5172 acquire data. $\overline{CS}$ must go low at least t_{CSS} before the rising edge of the serial clock (SCLK). With $\overline{CS}$ low, data is clocked into the register on the rising edge of SCLK. The maximum serial clock frequency guaranteed for proper operation is 10MHz for MAX5170 and 6MHz for MAX5172. See Figure 5 for a detailed timing diagram of the serial interface.

Serial Data Output (DOUT)

The serial-data output, DOUT, is the internal shift register's output and allows for daisy-chaining of multiple devices as well as data readback (see *Applications Information*). By default upon start-up, data shifts out of DOUT on the serial clock's rising edge (Mode 0) and provides a lag of 16 clock cycles, thus maintaining SPI, QSPI, and MICROWIRE compatibility. However, if the device is programmed for Mode 1, the output data lags DIN by 16.5 clock cycles and is clocked out on the serial clock's rising edge. During shutdown, DOUT retains its last digital state prior to shutdown.

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD			FUNCTION
C1	C0	D13.....D0	
0	0	14-bit DAC data	Load input register; DAC registers are unchanged.
0	1	14-bit DAC data	Load input register; DAC registers are updated (start-up DAC with new data).
1	0	x x x xxx xxxx xxxx	Update DAC register from input register (start-up DAC with data previously stored in the input registers).
1	1	0 0 x xxx xxxx xxxx	No operation (NOP).
1	1	0 1 x xxx xxxx xxxx	Shut down DAC (provided $\overline{PDL}$ = 1).
1	1	1 0 0 xxx xxxx xxxx	UPO goes low (default).
1	1	1 0 1 xxx xxxx xxxx	UPO goes high.
1	1	1 1 0 xxx xxxx xxxx	Mode 1, DOUT clocked out on SCLK's rising edge.
1	1	1 1 1 xxx xxxx xxxx	Mode 0, DOUT clocked out on SCLK's falling edge (default).

Low-Power, Serial, 14-Bit DACs with Voltage Output

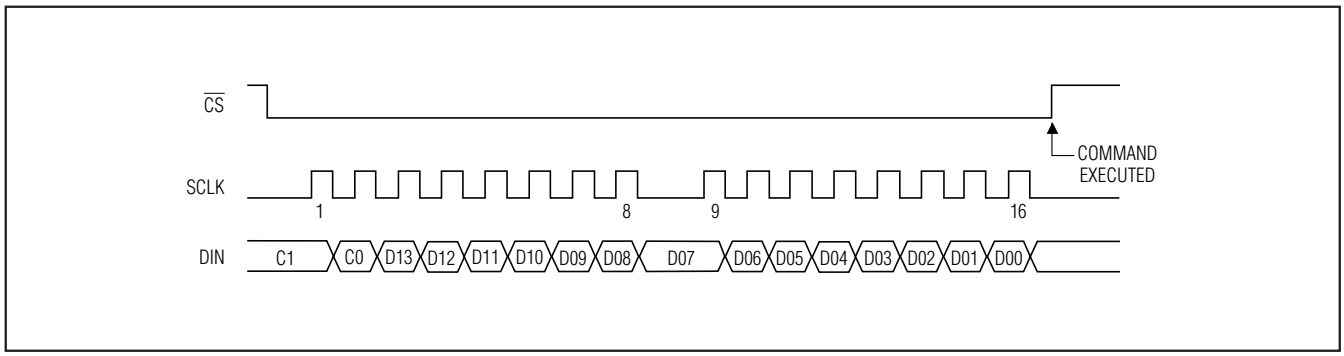


Figure 4. Serial-Interface Timing Diagram

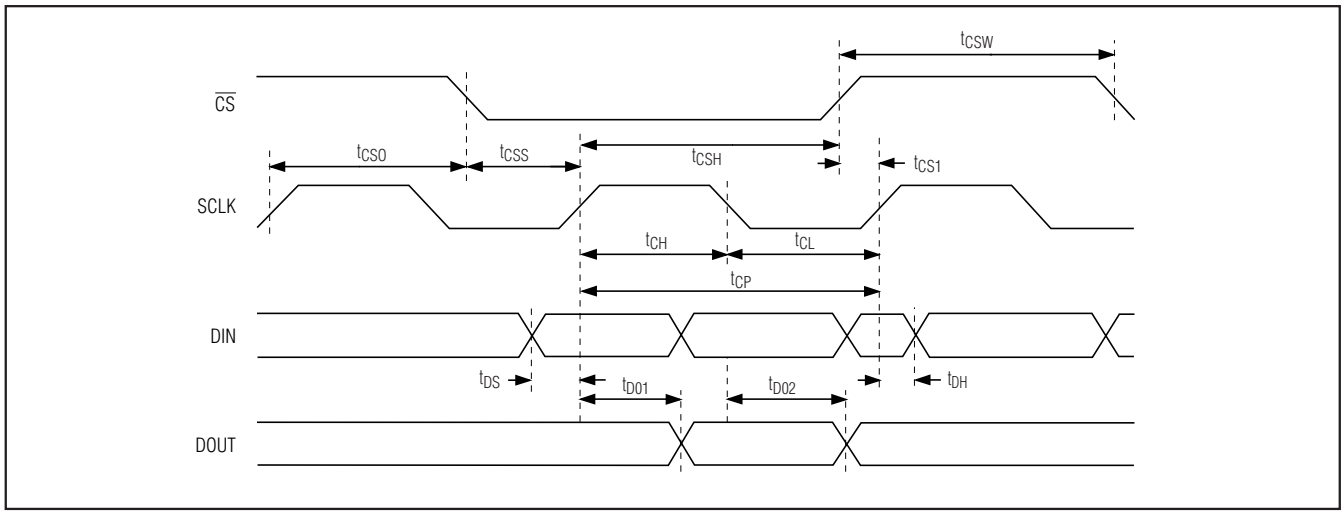


Figure 5. Detailed Serial-Interface Timing Diagram

User-Programmable Logic Output (UPO)

The UPO allows control of an external device through the serial interface, thereby reducing the number of microcontroller I/O pins required. During power-down, this output retains its digital state prior to shutdown. When $\overline{CLR}$ is pulled low, UPO resets to its programmed default state. See Table 1 for specific commands to control the UPO.

Reset (RS) and Clear ($\overline{CLR}$)

The MAX5170/MAX5172 offers a clear pin which resets the output voltage. If RS = DGND, then $\overline{CLR}$ resets the output voltage to the minimum voltage (0 if OS = AGND). If RS = V_{DD}, then $\overline{CLR}$ resets the output voltage to midscale. In either case, $\overline{CLR}$ resets UPO to its programmed default state.

Applications Information

Unipolar Output

Figure 6 shows the MAX5170/MAX5172 configured for unipolar, rail-to-rail operation with a gain of +1.638V/V. Table 2 lists the codes for unipolar output voltages. The maximum output voltage is limited to V_{DD}. Use the OS pin to introduce an offset voltage as shown in Figure 7 and described in the *Offset and Buffer Configurations* section.

Bipolar Output

Figure 8 shows the MAX5170/MAX5172 configured for bipolar output operation. The output voltage is given by the following equation (OS = AGND):

$$V_{OUT} = V_{REF}\left(\frac{2 \times N}{16{,}384} - 1\right)$$

where N represents the numeric value of the DAC's binary input code, V_{REF} is the voltage of the external reference. Table 3 shows digital codes and the corresponding output voltage for Figure 8's circuit.

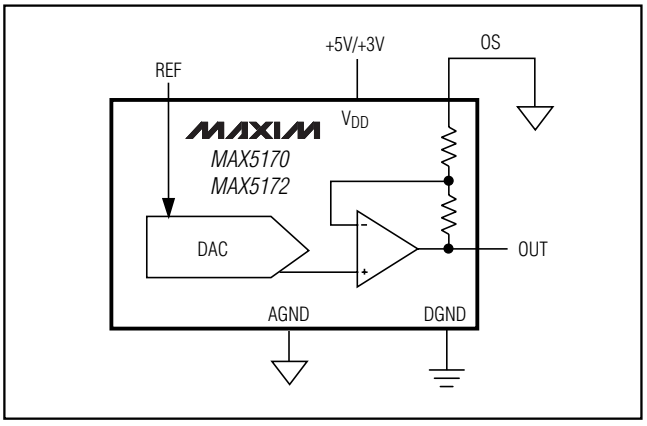


Figure 6. Unipolar Output Circuit (Rail-to-Rail)

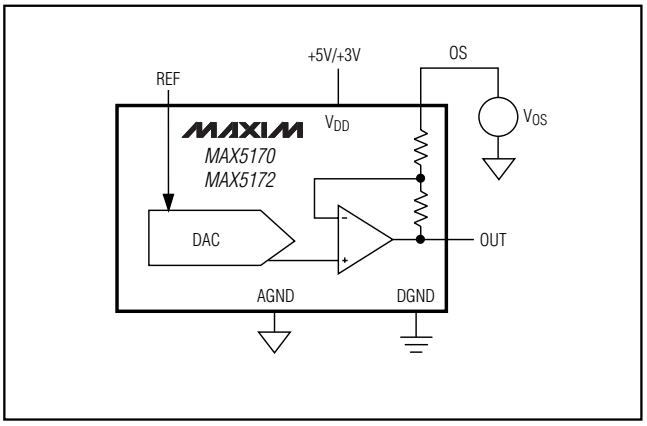


Figure 7. Setting OS for Output Offset

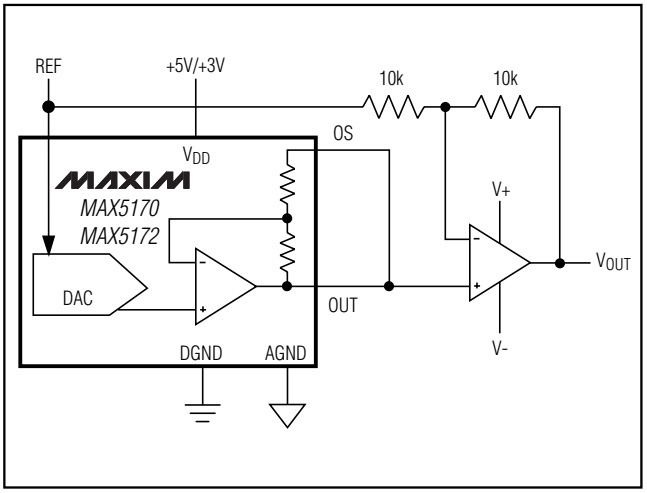


Figure 8. Bipolar Output Circuit

Table 2. Unipolar Code Table (Circuit of Figure 6)

DAC CONTENTS MSB LSB	ANALOG OUTPUT
11 1111 1111 1111	$+V_{REF}$ (16383/16384) • 1.638
10 0000 0000 0001	$+V_{REF}$ (8193/16384) • 1.638
10 0000 0000 0000	$+V_{REF}$ (8192/16384) • 1.638
01 1111 1111 1111	$+V_{REF}$ (8191/16384) • 1.638
00 0000 0000 0001	$+V_{REF}$ (1/16384) • 1.638
00 0000 0000 0000	0

Table 3. Bipolar Code Table (Circuit of Figure 8)

DAC CONTENTS MSB LSB	ANALOG OUTPUT
11 1111 1111 1111	$+V_{REF}$ [(2 · 16383/16384) - 1]
10 0000 0000 0001	$+V_{REF}$ [(2 · 8193/16384) - 1]
10 0000 0000 0000	$+V_{REF}$ [(2 · 8192/16384) - 1]
01 1111 1111 1111	$+V_{REF}$ [(2 · 8191/16384) - 1]
00 0000 0000 0001	$+V_{REF}$ [(2 · 1/16384) - 1]
00 0000 0000 0000	$-V_{REF}$

Low-Power, Serial, 14-Bit DACs with Voltage Output

Offset and Buffer Configurations

The simple circuit of Figure 7 illustrates how to introduce an offset to the output voltage. The amount of offset introduced by a voltage at the OS pin is shown in the following equation:

$$V_{OFFSET} = V_{OS} \times (1 - Gain)$$

where Gain = 1.638. However, the total output voltage of the device cannot exceed V_{DD} regardless of the voltage on the OS pin.

To set the gain of the output amplifier to 1, connect OS to OUT.

Daisy-Chaining Devices

The serial data output pin (DOUT) allows multiple MAX5170/MAX5172s to be daisy-chained together, as shown in Figure 9. The advantage of this is that only two lines are needed to control all the DACs on the line. The disadvantage is that it takes *n* commands to program the DACs. Figure 10 shows several MAX5170/MAX5172s sharing one common DIN signal line. In this configuration, the data bus is common to all devices. However, more I/O lines are required for this configuration because each device requires a dedicated $\overline{CS}$ line. The advantage of this configuration is that only one command is needed to program any DAC.

Using an AC Reference

The MAX5170/MAX5172 accepts reference voltages with AC components as long as the reference voltage remains between 0 and V_{DD} - 1.4V. Figure 11 shows a technique for applying an offset sine wave signal to REF. The reference voltage must remain above AGND.

Power-Supply and Layout Considerations

Wire-wrap boards are not recommended. For optimum system performance, use printed circuit boards with separate analog and digital ground planes. Connect the two ground planes together at the low-impedance power-supply source. Connect DGND and AGND pins together at the IC. The best ground connection is achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. This is useful because if the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass the power supply with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Minimize their lead lengths to reduce inductance. If noise becomes an issue, use shielding and/or ferrite beads to increase isolation.

To maintain INL and DNL performance as well as gain drift, it is extremely important to provide the lowest possible reference output impedance at the DAC reference input pin. INL degrades if the series resistance on REF pin exceeds 0.1Ω. The same consideration must be made for the AGND pin.

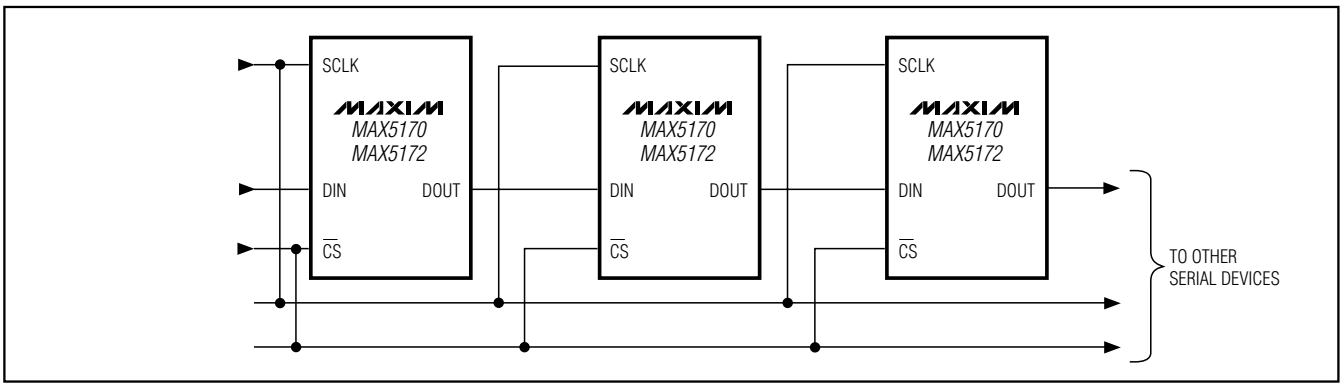


Figure 9. Daisy-Chaining MAX5170/MAX5172 Devices

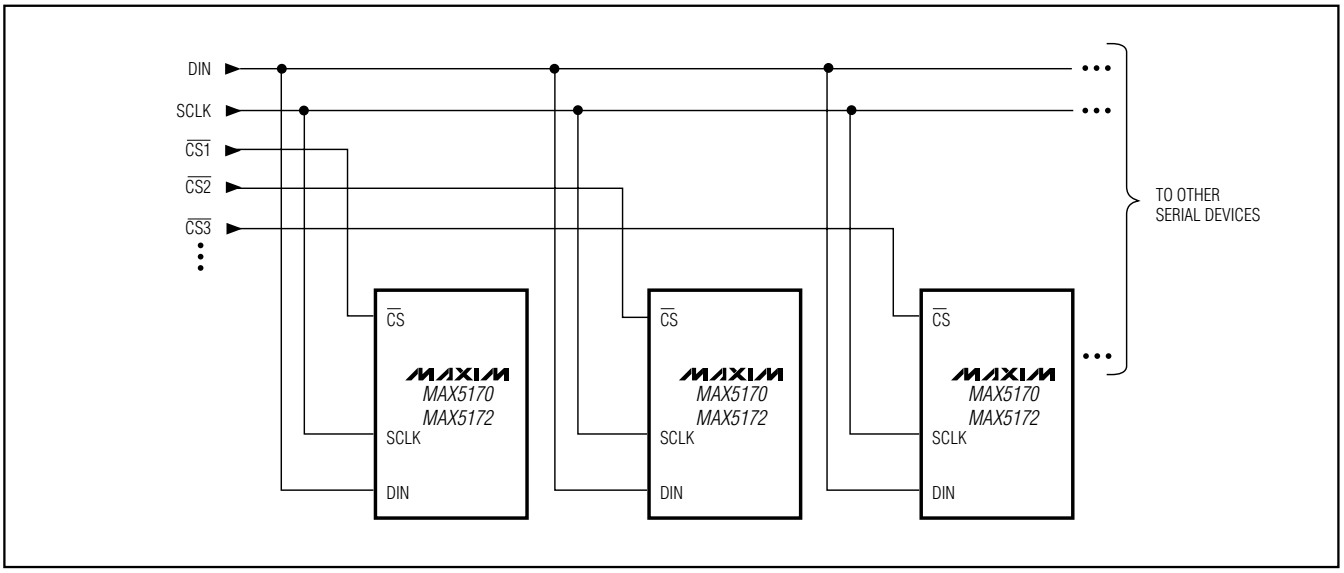


Figure 10. Multiple MAX5170/MAX5172s Sharing Common DIN and SCLK Lines

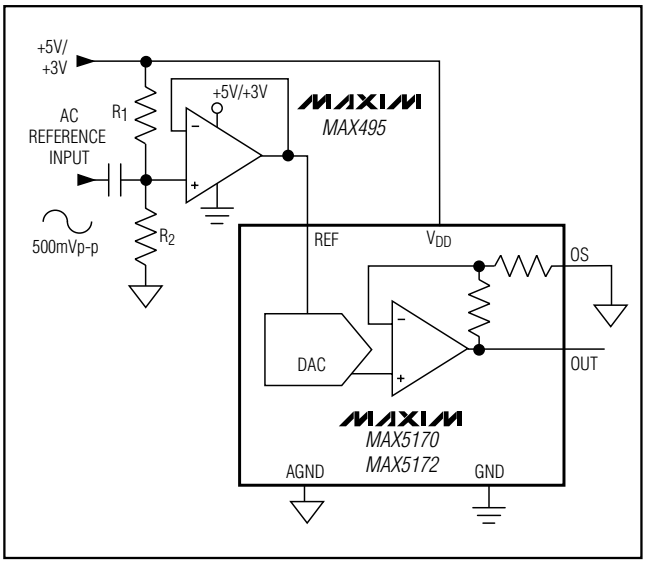


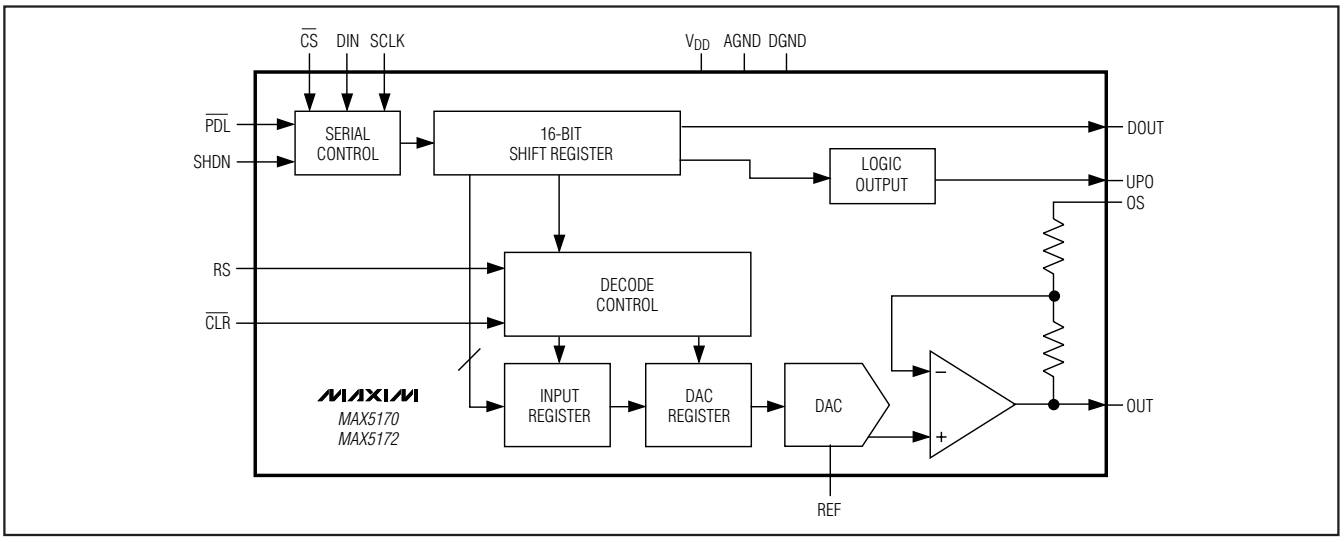
Figure 11. AC Reference Input Circuit

Chip Information

TRANSISTOR COUNT: 3457

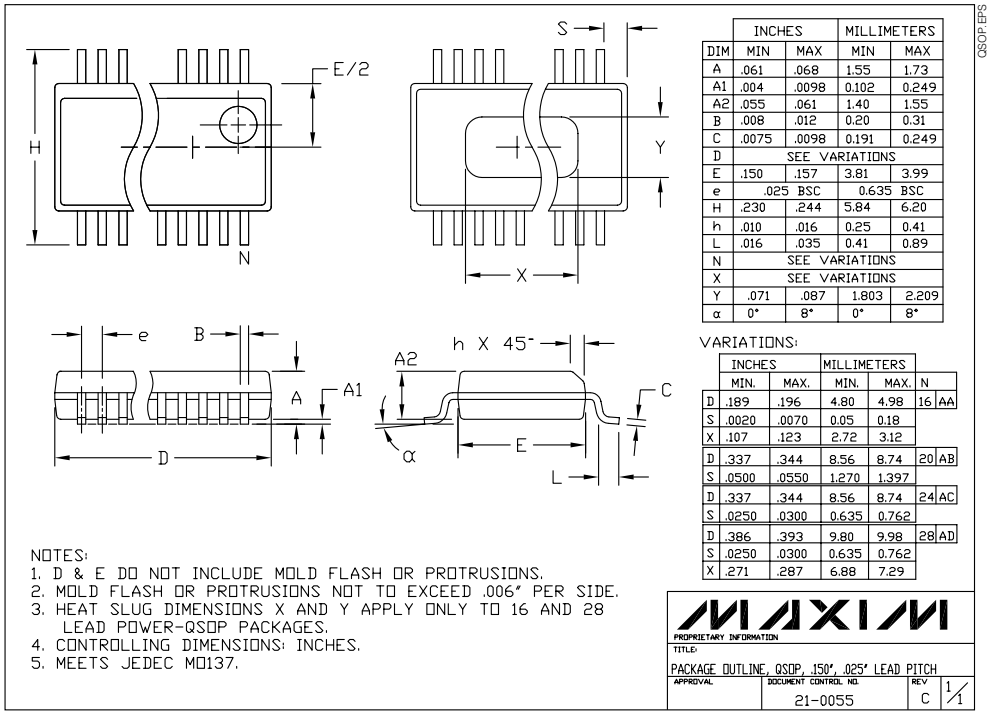
Low-Power, Serial, 14-Bit DACs with Voltage Output

Functional Diagram



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX5170AEEE+ MAX5170BEEE+ MAX5170AEEE+T MAX5170BEEE+T MAX5172AEEE+ MAX5172AEEE+T MAX5172BEEE+ MAX5172BEEE+T