Absolute Maximum Ratings

Any Pin to GND.....-0.3V to +3.9V
AVDD to GND.....-0.3V to +3.9V
DVDD to GND.....-0.3V to +3.9V
Analog Inputs (AINP, AINN, REFP, REFN) to GND .....-0.3V to (V_{AVDD} + 0.3V)
Digital Inputs and Digital Outputs to GND.....-0.3V to (V_{DVDD} + 0.3V)
ESD_{HB} (AVDD, AINP, AINN, REFP, REFN, DVDD, CLK, $\overline{CS}$, SCLK, $\overline{RDY}$/DOUT, GND).....±2kV (Note 1)

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C).....444mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -55°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Human Body Model to specification MIL-STD-883 Method 3015.7.

Electrical Characteristics

(V_{AVDD} = +3.6V, V_{DVDD} = +1.8V, V_{REFP} - V_{REFN} = V_{AVDD}; internal clock, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC PERFORMANCE						
Noise-Free Resolution (Notes 2, 3)	NFR	MAX11208A		19		Bits
		MAX11208B		20		
Thermal Noise (Notes 2, 3)	V_N	MAX11208A		2.1		μV_{RMS}
		MAX11208B		0.72		
Integral Nonlinearity	INL	(Note 4)	-10		+10	ppmFSR
Zero Error	V_{OFF}	After calibration, V_{REFP} - V_{REFN} = 2.5V	-13	1	+13	ppmFSR
Zero Drift				50		nV/°C
Full-Scale Error		After calibration, V_{REFP} - V_{REFN} = 2.5V (Note 5)	-30	3	+30	ppmFSR
Full-Scale Error Drift				0.05		ppmFSR/°C
Power-Supply Rejection		AVDD DC rejection	70	80		dB
		DVDD DC Rejection	90	100		
ANALOG INPUTS/REFERENCE INPUTS						
Common-Mode Rejection	CMR	DC rejection	90	123		dB
		50Hz/60Hz rejection, MAX11208A	90			
		50Hz/60Hz rejection, MAX11208B	144			
Normal-Mode 50Hz Rejection	NMR_{50}	MAX11208B (Note 6)	65	80.5		dB
Normal-Mode 60Hz Rejection	NMR_{60}	MAX11208B (Note 6)	73	87		dB
Common-Mode Voltage Range			GND		V_{AVDD}	V
Absolute Input Voltage		Low input voltage		GND - 30mV		V
		High input voltage		V_{AVDD} + 30mV		
DC Input Leakage		Sleep mode (Note 2)		±1		µA
AIN Dynamic Input Current				5		µA

Electrical Characteristics (continued)

(V_{AVDD} = +3.6V, V_{DVDD} = +1.8V, V_{REFP} - V_{REFN} = V_{AVDD}; internal clock, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REF Dynamic Input Current				7.5		µA
AIN Input Capacitance				10		pF
REF Input Capacitance				15		pF
AIN Voltage Range		V_{AINP} - V_{AINN}	$-V_{REF}$		$+V_{REF}$	V
REF Voltage Range					V_{AVDD}	V
Input Sampling Rate	f_S	MAX11208A		246		kHz
		MAX11208B		225		
REF Sampling Rate		MAX11208A		246		kHz
		MAX11208B		225		
LOGIC INPUTS (SCLK, CLK)						
Input Current		Input leakage current		±1		µA
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Hysteresis	V_{HYS}			200		mV
External Clock		MAX11208A		2.4576		MHz
		MAX11208B		2.2528		
LOGIC OUTPUTS ($\overline{RDY}$/DOUT)						
Output Low Level	V_{OL}	I_{OL} = 1mA, also tested for V_{DVDD} = 3.6V			0.4	V
Output High Level	V_{OH}	I_{OH} = 1mA, also tested for V_{DVDD} = 3.6V	0.9 x V_{DVDD}			V
Floating State Leakage Current		Output leakage current		±10		µA
Floating State Output Capacitance				9		pF
POWER REQUIREMENTS						
Analog Supply Voltage	AVDD		2.7		3.6	V
Digital Supply Voltage	DVDD		1.7		3.6	V
Total Operating Current		(AVDD + DVDD)		230	300	µA
DVDD Operating Current				45	60	µA
AVDD Operating Current				185	245	µA
AVDD Sleep Current				0.4	2	µA
DVDD Sleep Current				0.35	2	µA
2-WIRE SERIAL-INTERFACE TIMING CHARACTERISTICS						
SCLK Frequency	f_{SCLK}				5	MHz
SCLK Pulse Width Low	t_1	60/40 duty cycle 5MHz clock	80			ns
SCLK Pulse Width High	t_2	40/60 duty cycle 5MHz clock	80			ns
SCLK Rising Edge to Data Valid Transition Time	t_3				40	ns

Electrical Characteristics (continued)

(V_{AVDD} = +3.6V, V_{DVDD} = +1.8V, V_{REFP} - V_{REFN} = V_{AVDD}; internal clock, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

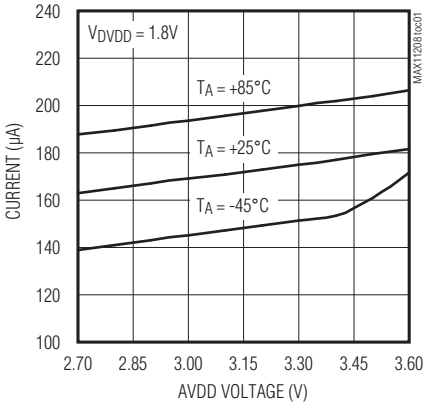
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Rising Edge Data Hold Time	t_4	Allows for positive edge data read	3			ns
$\overline{RDY}$/DOUT Fall to SCLK Rising Edge	t_5		0			ns
Next Data Update Time; No Read Allowed	t_6	MAX11208A		155		µs
		MAX11208B		169		
Data Conversion Time	t_7	MAX11208A		8.6		ms
		MAX11208B		73		
Data Ready Time After Calibration Starts (CAL + CNV)	t_8	MAX11208A		208.3		ms
		MAX11208B		256.1		
SCLK High After $\overline{RDY}$/DOUT Goes Low to Activate Sleep Mode	t_9	MAX11208A	0		8.6	ms
		MAX11208B	0		73	
Time from $\overline{RDY}$/DOUT Low to SCLK High for Sleep-Mode Activation	t_{10}	MAX11208A	0		8.6	ms
		MAX11208B	0		73	
Data Ready Time After Wake-Up from Sleep Mode	t_{11}	MAX11208A		8.6		ms
		MAX11208B		73		
Data Ready Time After Calibration from Sleep-Mode Wake-Up (CAL + CNV)	t_{12}	MAX11208A		208.4		ms
		MAX11208B		256.2		

Note 2: These specifications are not fully tested and are guaranteed by design and/or characterization.
Note 3: V_{AINP} = V_{AINN}.
Note 4: ppmFSR is parts per million of full-scale range.
Note 5: Positive full-scale error includes zero-scale errors.
Note 6: The MAX11208A has no normal-mode rejection at 50Hz or 60Hz.

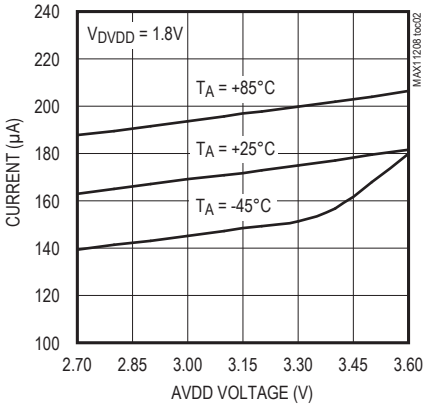
Typical Operating Characteristics

(V_{AVDD} = 3.6V, V_{DVDD} = 1.8V, V_{REFP} - V_{REFN} = AVDD; internal clock; T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

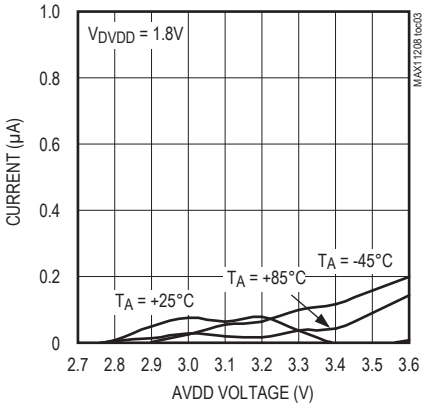
ANALOG ACTIVE CURRENT vs. AVDD VOLTAGE (MAX11208A)



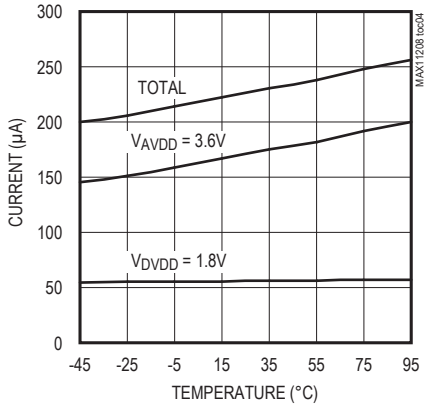
ANALOG ACTIVE CURRENT vs. AVDD VOLTAGE (MAX11208B)



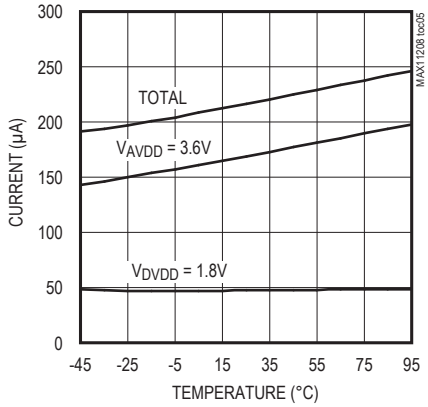
ANALOG SLEEP CURRENT vs. AVDD VOLTAGE (MAX11208A/MAX11208B)



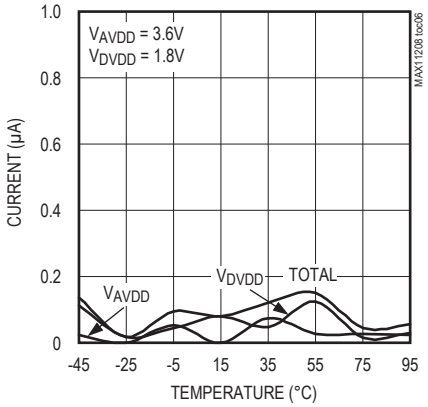
ACTIVE SUPPLY CURRENT vs. TEMPERATURE (MAX11208A)



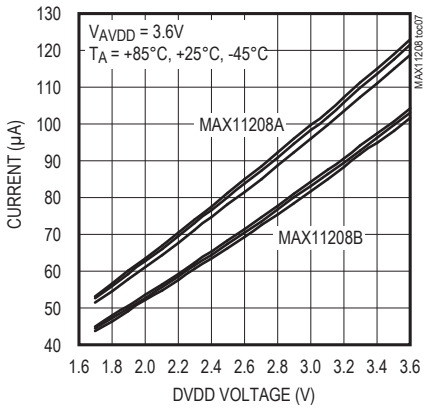
ACTIVE SUPPLY CURRENT vs. TEMPERATURE (MAX11208B)



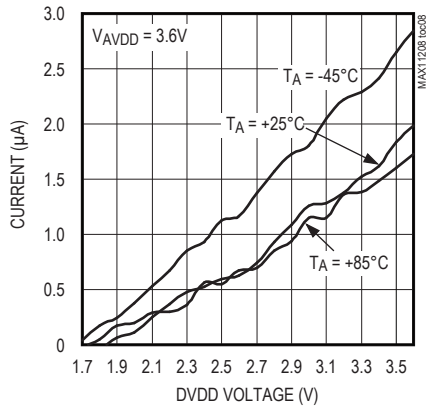
SLEEP CURRENT vs. TEMPERATURE (MAX11208A/MAX11208B)



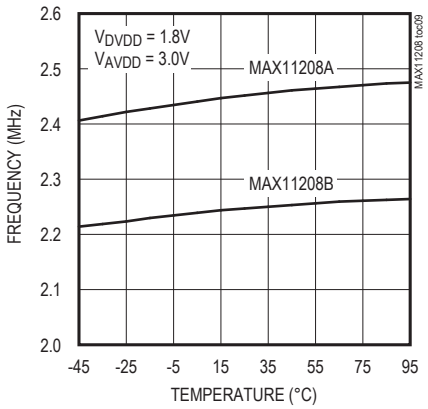
DIGITAL ACTIVE CURRENT vs. DVDD VOLTAGE



DIGITAL SLEEP CURRENT vs. DVDD VOLTAGE (MAX11208A/MAX11208B)



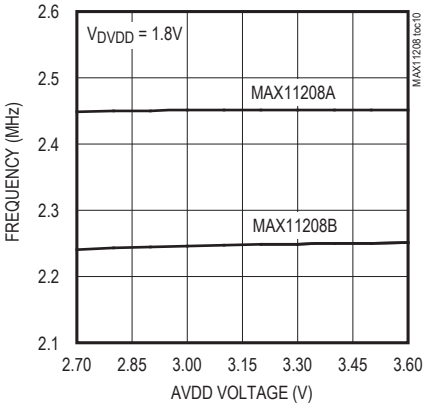
INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



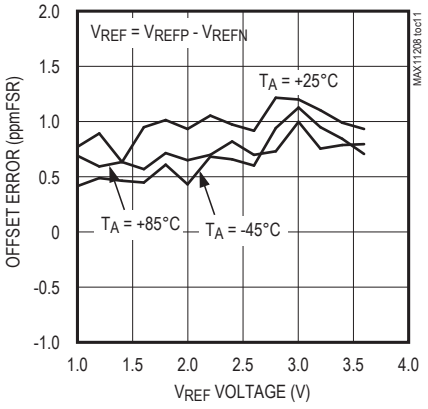
Typical Operating Characteristics (continued)

(V_{AVDD} = 3.6V, V_{DVDD} = 1.8V, V_{REFP} - V_{REFN} = AVDD; internal clock; T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

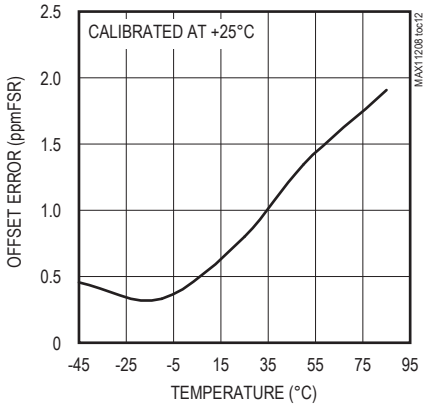
INTERNAL OSCILLATOR FREQUENCY vs. AVDD VOLTAGE



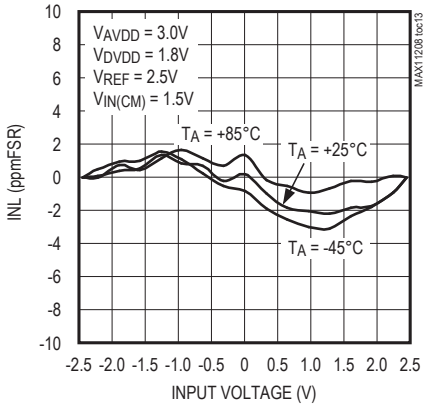
OFFSET ERROR vs. V_{REF} (MAX11208A/MAX11208B)



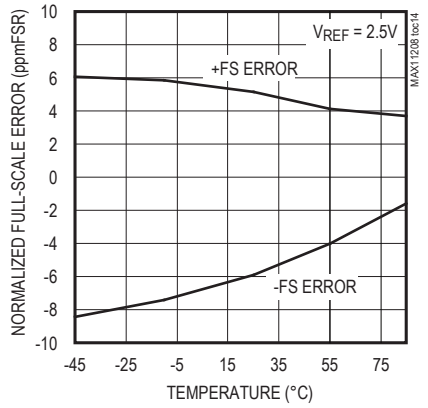
OFFSET ERROR vs. TEMPERATURE (MAX11208A/MAX11208B)



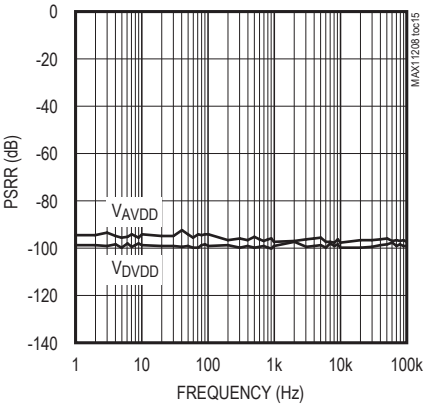
INTEGRAL NONLINEARITY vs. INPUT VOLTAGE (MAX11208A/MAX11208B)



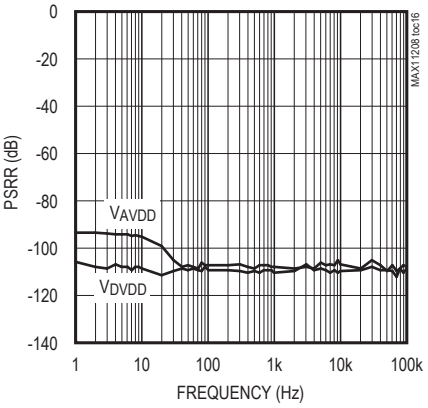
FULL-SCALE ERROR vs. TEMPERATURE (MAX11208A/MAX11208B)



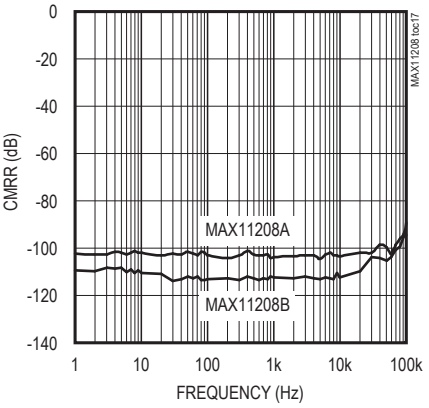
PSRR vs. FREQUENCY (MAX11208A)



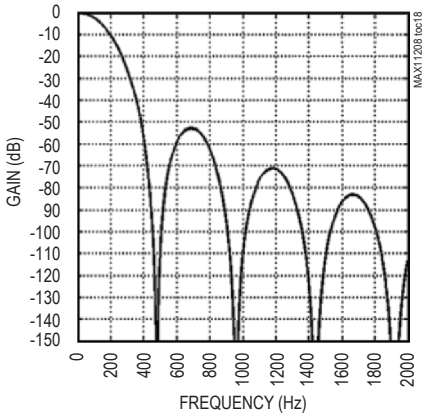
PSRR vs. FREQUENCY (MAX11208B)



CMRR vs. FREQUENCY (MAX11208A/MAX11208B)



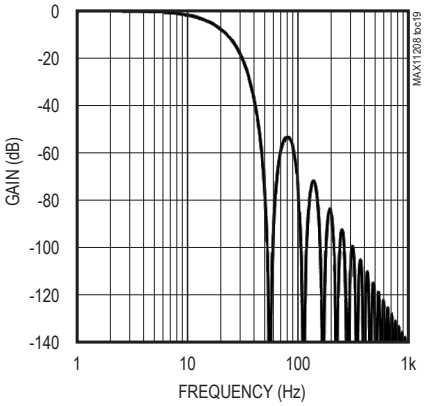
NORMAL-MODE FREQUENCY RESPONSE (MAX11208A)



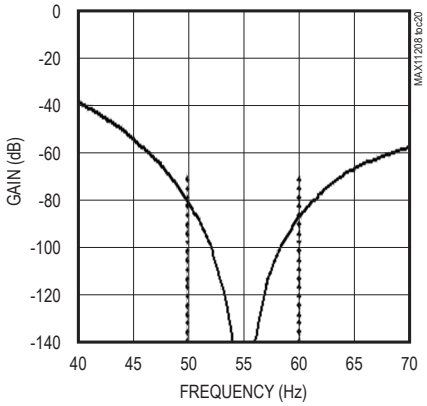
Typical Operating Characteristics (continued)

(V_{AVDD} = 3.6V, V_{DVDD} = 1.8V, V_{REFP} - V_{REFN} = AVDD; internal clock; T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

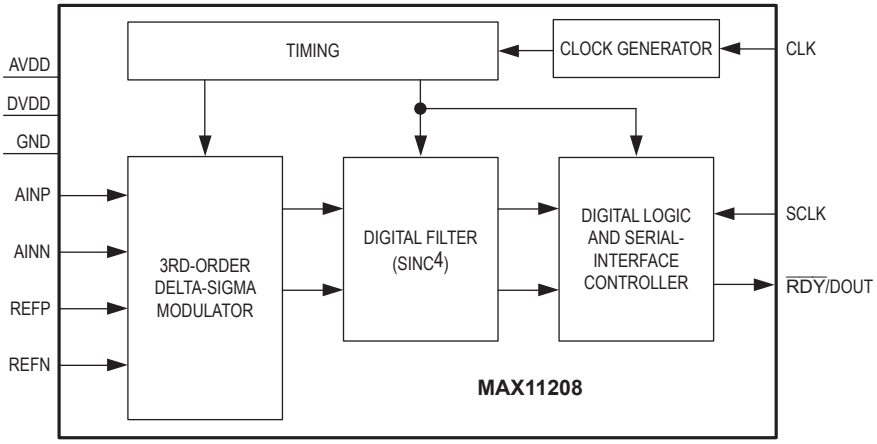
NORMAL-MODE FREQUENCY RESPONSE (MAX11208B)



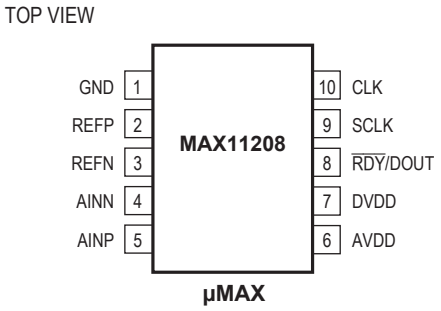
NORMAL MODE REJECTION OF 50Hz TO 60Hz (MAX11208B)



Functional Diagram



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	GND	Ground. Ground reference for analog and digital circuitry.
2	REFP	Differential Reference Positive Input. REFP must be more positive than REFN. Connect REFP to a voltage between AVDD and GND.
3	REFN	Differential Reference Negative Input. REFN must be more negative than REFP. Connect REFN to a voltage between AVDD and GND.
4	AINN	Negative Fully Differential Analog Input
5	AINP	Positive Fully Differential Analog Input
6	AVDD	Analog Supply Voltage. Connect a supply voltage between +2.7V to +3.6V with respect to GND.
7	DVDD	Digital Supply Voltage. Connect a digital supply voltage between +1.7V to +3.6V with respect to GND.
8	$\overline{RDY}$/DOUT	Data-Ready Output/Serial-Data Output. This output serves a dual function. In addition to the serial-data output function, the $\overline{RDY}$/DOUT also indicates that the data is ready when the $\overline{RDY}$ is logic-low. $\overline{RDY}$/DOUT changes on the falling edge of SCLK.
9	SCLK	Serial-Clock Input. Apply an external serial clock to SCLK.
10	CLK	External Clock Signal Input. The internal clock shuts down when CLK is driven by an external clock. Use a 2.4576MHz oscillator (MAX11208A) or a 2.2528MHz oscillator (MAX11208B).

Detailed Description

The MAX11208 is an ultra-low-power (< 240µA active), high-resolution, low-speed, serial-output ADC. This device provides the highest resolution per unit power in the industry and is optimized for applications that require very high dynamic range with low power, such as sensors on a 4mA to 20mA industrial control loop.

The MAX11208 provides a high-accuracy internal oscillator, which requires no external components. When used with the specified data rates, the internal digital filter provides more than 80dB rejection of 50Hz or 60Hz line noise. The MAX11208 provides a simple, system-friendly, 2-wire serial interface in the space-saving, 10-pin µMAX package.

Power-On Reset (POR)

The MAX11208 utilizes power-on reset (POR) supply-monitoring circuitry on both the digital supply (DVDD) and the analog supply (AVDD). The POR circuitry ensures proper device default conditions after either a digital or analog power-sequencing event.

The MAX11208 performs a self-calibration operation as part of the startup initialization sequence whenever a digital POR is triggered. It is important to have a stable reference voltage available at the REFP and REFN pins to ensure an accurate calibration cycle. If the reference voltage is not stable during a POR event, the part should be calibrated once the reference has stabilized. The part can be programmed for calibration by using 26 SCLKs as shown in Figure 3.

The digital POR trigger threshold is approximately 1.2V and has 100mV of hysteresis. The analog POR trigger threshold is approximately 1.25V and has 100mV of hysteresis. Both POR circuits have lowpass filters that prevent high-frequency supply glitches from triggering the POR. The analog supply (AVDD) and the digital supply (DVDD) pins should be bypassed using 0.1µF capacitors placed as close as possible to the package pin.

Analog Inputs

The MAX11208 accepts two analog inputs (AINP and AINN). The modulator input range is bipolar ($-V_{REF}$ to $+V_{REF}$).

Internal Oscillator

The MAX11208 incorporates a highly stable internal oscillator that provides the system clock. The system clock runs the internal state machine and is trimmed to 2.4576MHz (MAX11208A) or 2.2528MHz (MAX11208B). The internal oscillator clock is divided down to run the digital and analog timing.

Reference

The MAX11208 provides differential inputs REFP and REFN, for an external reference voltage. Connect the external reference directly across the REFP and REFN to obtain the differential reference voltage. The common-mode voltage range for V_{REFP} and V_{REFN} is between 0 and V_{AVDD}. The differential voltage range for REFP and REFN is 1V to V_{AVDD}.

Digital Filter

The MAX11208 contains an on-chip, digital lowpass filter that processes the 1-bit data stream from the modulator using a $SINC^4$ $(sinx/x)^4$ response. When the device is operating in single-cycle conversion mode, the filter is reset at the end of the conversion cycle. When operating in continuous conversion latent mode, the filter is not reset. The $SINC^4$ filter has a -3dB frequency equal to 24% of the data rate.

Serial-Digital Interface

The MAX11208 communicates through a 2-wire serial interface with a clock input and data output. The output rate is predetermined based on the package option (MAX11208A at 120sps and MAX11208B at 13.75sps).

2-Wire Interface

The MAX11208 is compatible with the 2-wire interface and uses SCLK and $\overline{RDY}$/DOUT for serial communications. In this mode, all controls are implemented by timing the high or low phase of the SCLK. The 2-wire serial interface only allows for data to be read out through the $\overline{RDY}$/DOUT output. Supply the serial clock to SCLK to shift the conversion data out.

The $\overline{RDY}$/DOUT is used to signal data ready, as well as reading the data out when SCLK pulses are applied. $\overline{RDY}$/DOUT is high by default. The MAX11208 pulls $\overline{RDY}$/DOUT low when data is available at the end of conversion, and stays low until clock pulses are applied at SCLK input; on applying the clock pulses at SCLK, the $\overline{RDY}$/DOUT outputs the conversion data on every SCLK positive edge. To monitor data availability, pull $\overline{RDY}$/DOUT high after reading the 20 bits of data by supplying a 25th SCLK pulse. The different operational modes using this 2-wire interface are described in the following sections.

Data Read Following Every Conversion

The MAX11208 indicates conversion data availability, as well as lets the retrieval of data through the $\overline{RDY}$/DOUT output. The $\overline{RDY}$/DOUT output idles at the value of the last bit read unless a 25th SCLK pulse is provided, causing $\overline{RDY}$/DOUT to idle high. $\overline{RDY}$/DOUT is pulled low when the conversion data is available.

The timing diagram for the data read is shown in Figure 1. Once a low is detected on $\overline{RDY}$/DOUT, clock pulses at SCLK clock out the data. Data is shifted out MSB first and is in binary two's complement format. Once all the data has been shifted out, a 25th SCLK is required to pull the $\overline{RDY}$/DOUT output back to the idle high state. See Figure 2.

If the data is not read before the next conversion data is updated, the old data is lost, as the new data overwrites the old value.

Data Read Followed by Self-Calibration

To initiate self-calibration at the end of a data read, provide a 26th SCLK pulse. After reading the 24 bits of conversion data, a 25th positive edge on SCLK pulls the $\overline{RDY}$/DOUT output back high, indicating the end of data read. Provide a 26th SCLK pulse to initiate a self-calibration routine starting on the falling edge of the 26th SCLK. A subsequent falling edge of $\overline{RDY}$/DOUT indicates data availability at the end of calibration. The timing is illustrated in Figure 3.

Data Read Followed by Sleep Mode

The MAX11208 can be put into sleep mode to save power between conversions. To activate the sleep mode, idle the SCLK high any time after the $\overline{RDY}$/DOUT output goes low (that is, after conversion data is available). It is not required to read out all 20 bits before putting the part in sleep mode. Sleep mode is activated after the SCLK is held high (see Figure 4). The $\overline{RDY}$/DOUT output is pulled high once the device enters sleep mode. To come out of the sleep mode, pull SCLK low. After the sleep mode is deactivated (when the device wakes up), conversion starts again and $\overline{RDY}$/DOUT goes low indicating the next conversion data is available. See Figure 4.

Single Conversion Mode

For operating the MAX11208 in single conversion mode, activate and deactivate sleep mode between conversions (as described in the *Data Read Followed by Sleep Mode* section). Single conversion mode reduces power consumption by shutting down the device when idle between conversions. See Figure 4.

Single Conversion Mode with Self-Calibration at Wakeup

The MAX11208 can be put in self-calibration mode immediately after wake-up from sleep mode. Self-calibration at wake-up helps to compensate for temperature or supply changes if the device is shut down for extensive periods. To automatically start self-calibration at the end of sleep mode, all the data bits must be shifted out followed by the 25th SCLK edge to pull $\overline{RDY}$/DOUT high. On the 26th SCLK, keep it high for as long as shutdown is desired. Once SCLK is pulled back low, the device automatically performs a self-calibration, and when the data is ready, the $\overline{RDY}$/DOUT output goes low. See Figure 5. This also achieves the purpose of single conversions with self-calibration.

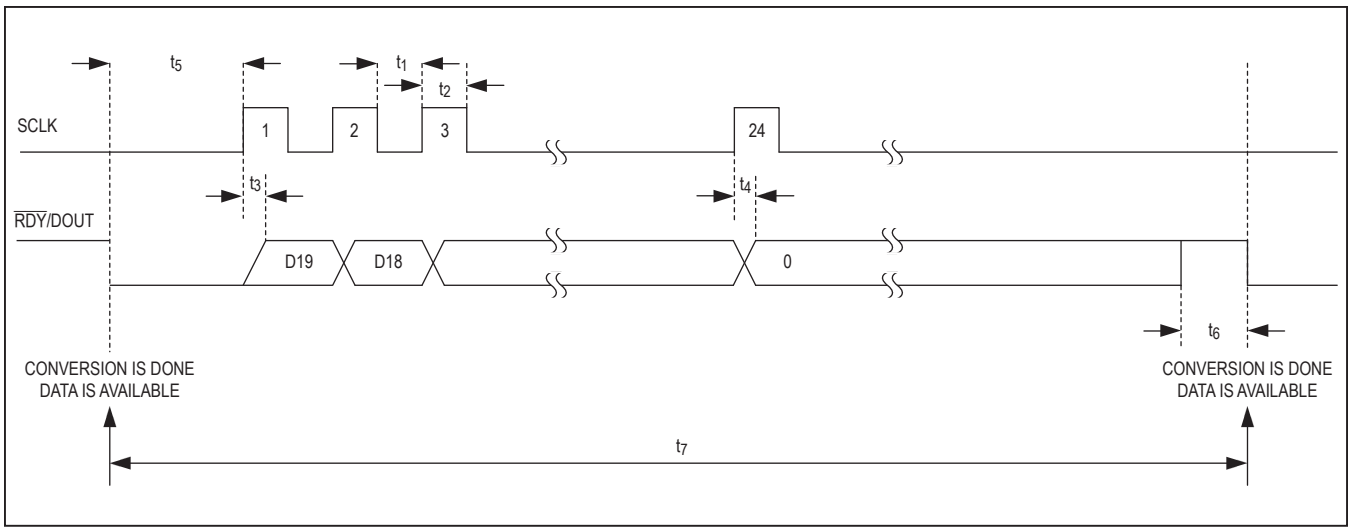


Figure 1. Timing Diagram for Data Read After Conversion

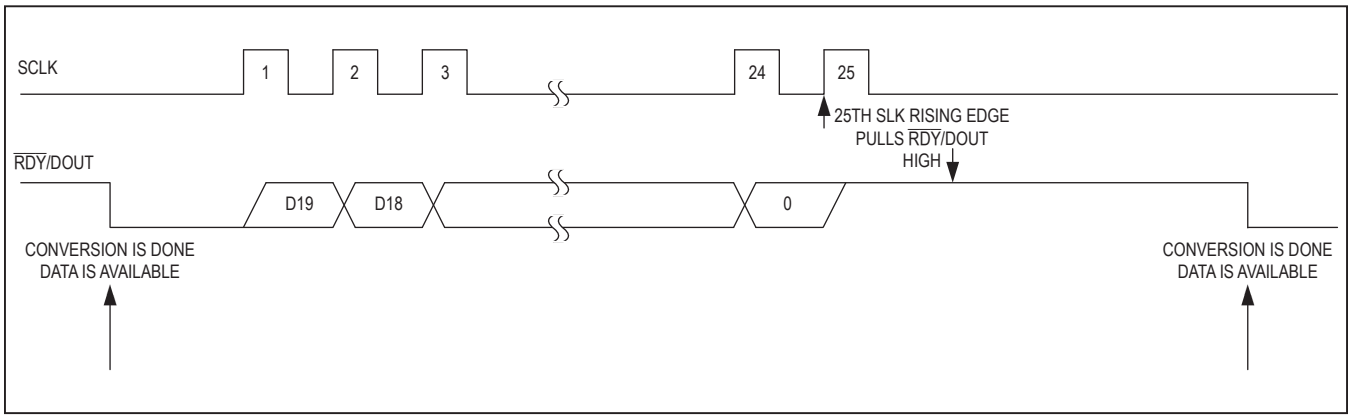


Figure 2. Timing Diagram for Data Read Followed by RDY/DOUT Being Asserted High Using 25th SCLK

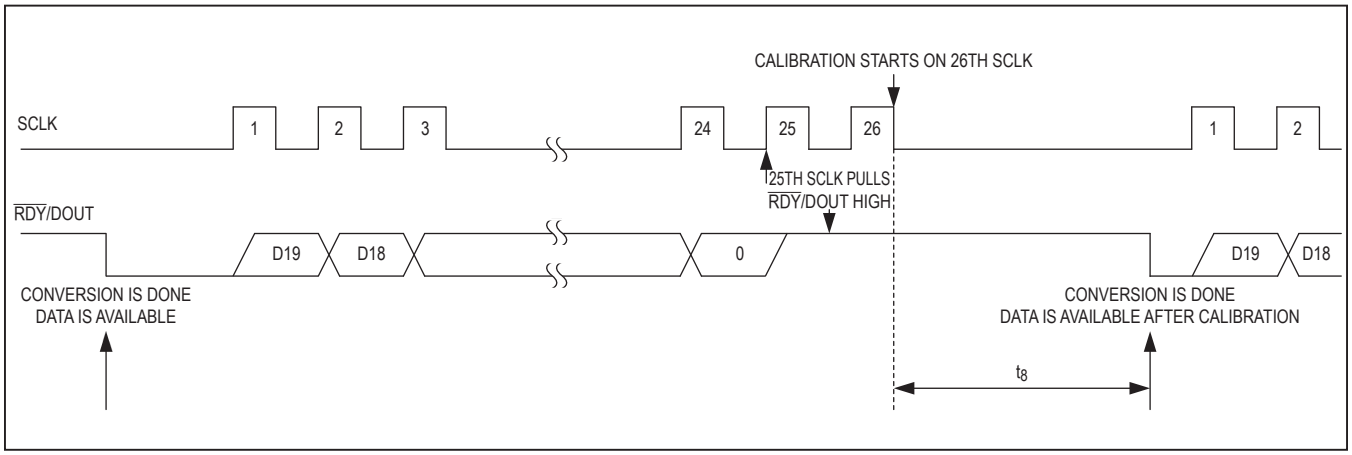


Figure 3. Timing Diagram for Data Read Followed by Two Extra Clock Cycles for Self-Calibration

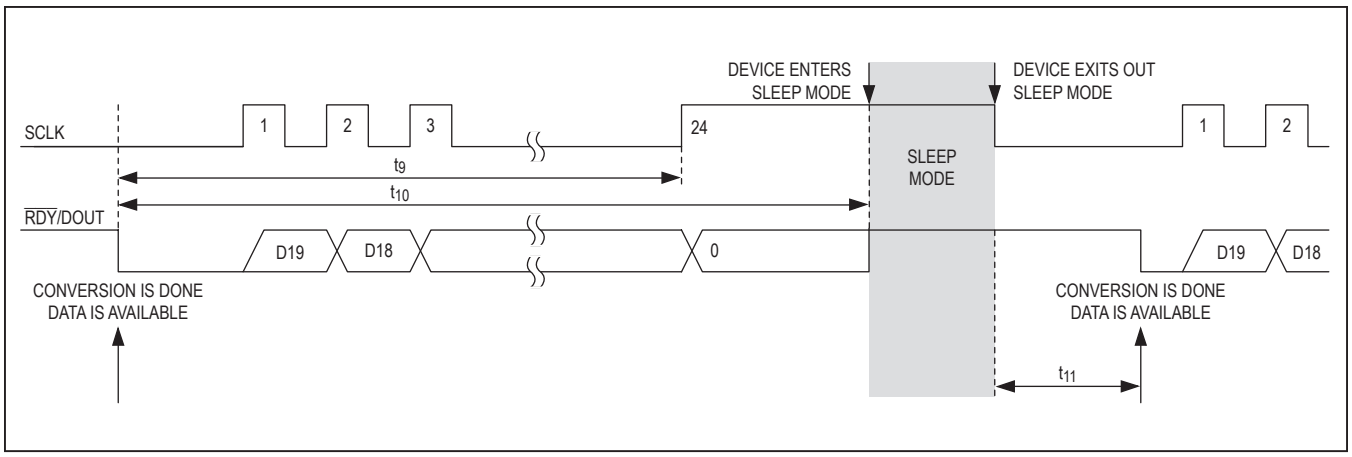


Figure 4. Timing Diagram for Data Read Followed by Sleep-Mode Activation; Single Conversion Timing

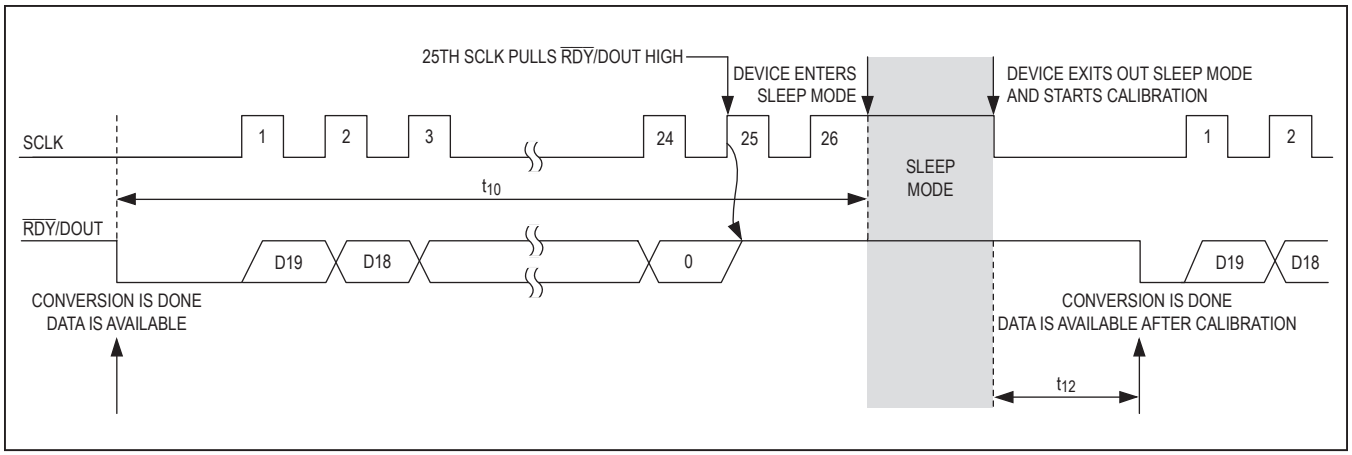


Figure 5. Timing Diagram for Sleep-Mode Activation Followed by Self-Calibration at Wake-Up

Applications Information

See Figure 6 for the RTD temperature measurement circuit and Figure 7 for a resistive bridge measurement circuit.

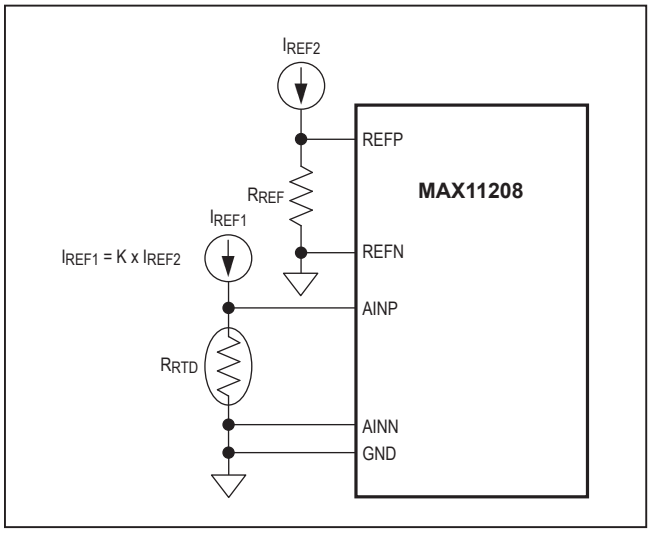


Figure 6. RTD Temperature Measurement Circuit

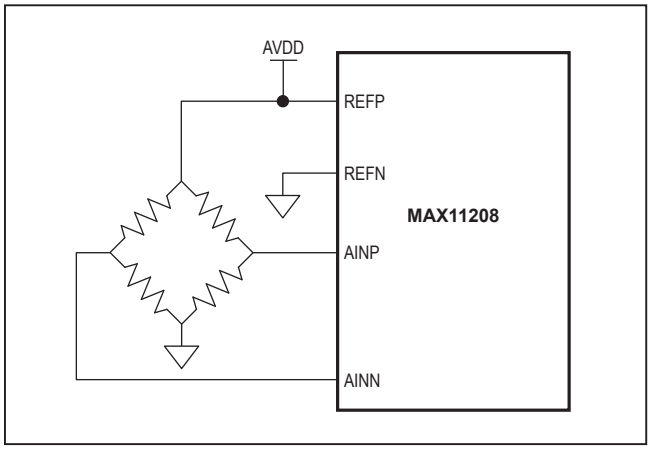


Figure 7. Resistive Bridge Measurement Circuit

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 µMAX	U10+2	21-0061

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/10	Initial release	—
1	7/20	Updated toc18	6

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