ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
All Other Pins to GND .....-0.3V to (Vcc + 0.3V)
Current into Any Pin .....±20mA
Rate-of-Rise, V_{CC} 100V/µs
Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 24.4mW/°C above +70°C).....1951.0mW
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection (all pins, Human Body Model) 2000V
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating s only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specificatio ns is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		2		5.5	V
Active Supply Current (Note 2)	I_{CC}	V_{CC} = +2.0V			110	µA
		V_{CC} = +5V			800	
Timekeeping Supply Current (Note 3)	I_{TK}	V_{CC} = +2.0V		0.4	0.7	µA
		V_{CC} = +5V		1.4	2.2	
32kHz OUTPUT						
Output High Voltage (Note 5)	V_{OH}	V_{CC} = +2.0V, I_{SOURCE} = -0.4mA	1.8			V
		V_{CC} = +5.0V, I_{SOURCE} = -1mA	4.5			
Output Low Voltage (Note 5)	V_{OL}	V_{CC} = +2.0V, I_{SINK} = 1.5mA			0.4	V
		V_{CC} = +5.0V, I_{SINK} = 4mA			0.4	
Duty Cycle				40		%
Output Leakage Current		V_{IN} = 0 to V_{CC}, 32kHz output disabled	-10		10	nA
3-WIRE DIGITAL INPUTS AND OUTPUTS (SCLK, I/O, CS)						
Input High Voltage	V_{IH}	V_{CC} = +2.0V	1.4			V
		V_{CC} = +5.0V	2.2			
Input Low Voltage	V_{IL}	V_{CC} = +2.0V			0.6	V
		V_{CC} = +5.0V			0.8	
Input Leakage Current		V_{IN} = 0 to V_{CC}	-10		10	nA
SCLK, RST Capacitance				5		pF
I/O Capacitance				10		pF
I/O Output Low Voltage	V_{OL}	V_{CC} = +2.0V, I_{SINK} = 1.5mA			0.4	V
		V_{CC} = +5.0V, I_{SINK} = 4mA			0.4	
I/O Output High Voltage	V_{OH}	V_{CC} = +2.0V, I_{SOURCE} = -0.4mA	1.8			V
		V_{CC} = +5.0V, I_{SOURCE} = -1mA	4.5			

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Figures 4, 5 and Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR							
X1 to Ground Capacitance (Note 5)					25		pF
X2 to Ground Capacitance (Note 5)					25		pF
3-WIRE SERIAL TIMING							
Data to CLK Setup	t_{DC}	V_{CC} = +2V		200			ns
		V_{CC} = +5V		50			
CLK to Data Hold	t_{CDH}	V_{CC} = +2V		280			ns
		V_{CC} = +5V		70			
CLK to Data Delay	t_{CDD}	C_L = 50pF	V_{CC} = +2V			800	ns
			V_{CC} = +5V			200	
CLK Low Time	t_{CL}	V_{CC} = +2V		1000			ns
		V_{CC} = +5V		250			
CLK High Time	t_{CH}	V_{CC} = +2V		1000			ns
		V_{CC} = +5V		250			
CLK Frequency	f_{CLK}	V_{CC} = +2V		DC		0.5	MHz
		V_{CC} = +5V		DC		2.0	
CLK Rise and Fall Time	t_R, t_F	V_{CC} = +2V				2000	ns
		V_{CC} = +5V				500	
CS to CLK Setup	t_{CC}	V_{CC} = +2V		4			µs
		V_{CC} = +5V		1			
CLK to CS Hold	t_{CCH}	V_{CC} = +2V		240			ns
		V_{CC} = +5V		60			
CS Inactive Time	t_{CWH}	V_{CC} = +2V		4			µs
		V_{CC} = +5V		1			
CS to I/O High Z	t_{CDZ}	R_L = 1kΩ, C_L = 60pF	V_{CC} = +2V	0		280	ns
			V_{CC} = +5V	0		70	
SCLK to I/O High Z	t_{CCZ}	R_L = 1kΩ, C_L = 60pF	V_{CC} = +2V	0		280	ns
			V_{CC} = +5V	0		70	

Note 1: All parameters are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by design and not production tested.

Note 2: I_{CC} is specified with the I/O grounded, CS high, SCLK = 2MHz at V_{CC} = +5V; SCLK = 500kHz at V_{CC} = +2.0V, 32kHz output enabled, and no load on 32kHz output.

Note 3: Timekeeping current is specified with CS = GND, SCLK = GND, I/O = GND, 32kHz = GND, and 32kHz disabled.

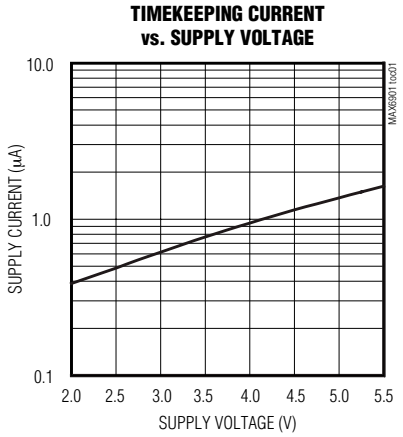
Note 4: All values referred to V_{IH} min and V_{IL} max levels.

Note 5: Guaranteed by design. Not production tested.

3-Wire Serial RTC in a TDFN

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial Clock Input. 3-wire serial clock for I/O data transfers.
2	V_{CC}	Power-Supply Pin. Bypass V_{CC} to GND with a 0.1µF capacitor.
3	X2	External 32.768kHz Crystal Connection
4	X1	External 32.768kHz Crystal Connection
5	32KHZ	Buffered Push-Pull 32.768kHz Output. When enabled, 32KHZ puts a buffered version of the timekeeping clock. When disabled, 32KHZ is high impedance. The power-on reset (POR) default state of 32KHZ is enabled.
6	GND	Ground Connection
7	CS	Chip-Select Input. Active-high for valid data transfers.
8	I/O	Data Input/Output. 3-wire serial data input/output connection.
—	PAD	Ground

Detailed Description

The MAX6901 is a real-time clock/calendar with a 3-wire serial interface and 31 × 8 bits of SRAM. It provides seconds, minutes, hours, day of the week, date of the month, month, and year information, held in seven 8-bit timekeeping registers (*Functional Diagram*). An on-chip 32.768kHz oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies the parameters for the external crystal, and Figure 1 shows a functional schematic of the oscillator circuit. The MAX6901's register addresses and definitions are described in Tables 2 and 3. Time and calendar data are stored in the registers in binary coded decimal (BCD) format. A polled alarm function is included for scheduled timing of user-defined times or intervals.

Command and Control

Address/Command Byte

Each data transfer into or out of the MAX6901 is initiated by an Address/Command byte. The Address/Command byte specifies which registers are to be accessed, and if the access is a read or a write. Table 2 shows the Address/Command bytes and their associated registers, and Table 3 lists the hex codes for all read and write operations. The Address/Command bytes are input LSB (bit 0) first. Bit 0 specifies a write (logic 0) or read (logic 1). Bits 1 to 5 specify the designated register to be written or read. Bit 6 specifies register data (logic 0), or RAM data (logic 1). The MSB (bit 7) must be logic 1. If the MSB is a zero, writes to the MAX6901 are disabled.

Table 1. Acceptable Quartz Crystal Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Frequency	f		32.76		kHz
Equivalent Series Resistance (ESR)	R_S	40		60	kΩ
Parallel Load Capacitance	C_L	11.2	12.5	13.7	pF
Q Factor	Q	40,000		60,000	

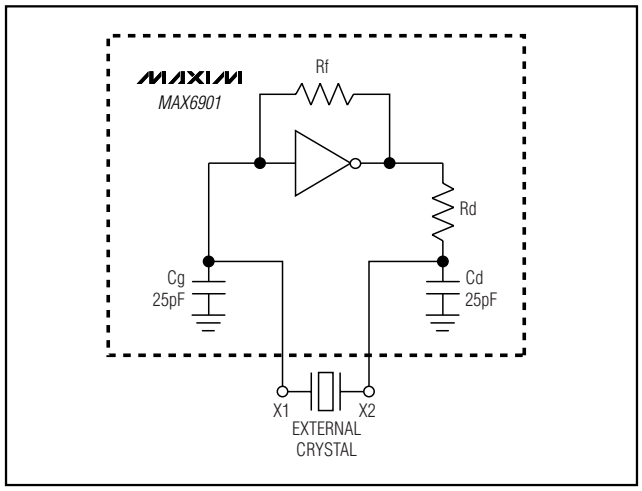


Figure 1. Oscillator Circuit Schematic

Clock Burst Mode

Accessing the Clock Burst register specifies burst-mode operation. In this mode, multiple bytes are read or written with a single Address/Command write. If the Clock Burst register is accessed (BEh for Write and BFh for Read), the first seven clock/calendar registers (Seconds, Minutes, Hours, Date, Month, Day, and Year) and the Control register, are consecutively read or written, starting with the LSB of the Seconds register. When writing to the clock registers in burst mode, all seven registers must be written in order for the data to be transferred (see *Example: Setting the Clock with a Burst Write*).

RAM Burst Mode

Sending the RAM Burst Address/Command specifies Burst-Mode operation. In this mode, the 31 RAM registers can be consecutively read or written, starting with bit 0 of address C0h for Writes, and C1h for Reads. Burst Read outputs all 31 registers of RAM. When writing to RAM in burst mode, it is not necessary to write all 31 bytes for the data to transfer; each complete byte written is transferred to RAM. When reading from RAM, data bits are output until all 31 bytes have been read, or until CS is driven low.

Setting the Clock

Writing to the Timekeeping Registers

The Time and Date are set by writing to the timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year, and Century). During a write operation, an input buffer accepts the new time data while the timekeeping registers continue to increment normally, based on the crystal counter. The buffer also keeps the timekeeping registers from changing as the result of an incomplete Write operation, and collision detection circuitry ensures that a time write does not occur coincident with a Seconds register increment. The updated time data are loaded into the timekeeping registers on the falling edge of CS, at the end of the 3-wire serial Write operation. An incomplete Write operation aborts the update procedure, and the contents of the input buffer are discarded. The timekeeping registers reflect the new time, beginning with the first Seconds register increment after the falling edge of CS.

Although both Single Writes and Burst Writes are possible, the best way to write to the timekeeping registers is with a Burst Write. With a Burst Write, main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year), and the Control register are written sequentially following the Address/Command byte. They must be written as a group of eight registers, with 8 bits each, for proper execution of the Burst Write function. All seven timekeeping registers are simultaneously loaded into the clock counters by the falling edge of CS, at the end of the 3-wire serial Write operation. For a normal burst data transfer, the worst-case error that can occur between the actual time and the written time update is 1 second.

If Single Write operations are used to enter data into the timekeeping registers, error checking is required. If the Seconds register is not to be written, then begin by reading the Seconds register and save it as initial-seconds. Write to the required timekeeping registers and

3-Wire Serial RTC in a TDFN

Table 2. Register Address/Definition

FUNCTION	REGISTER ADDRESS A7	A6	A5	A4	A3	A2	A1	A0		REGISTER DEFINITION VALUE	D7	D6	D5	D4	D3	D2	D1	D0
TIMEKEEPING																		
SECOND	1	0	0	0	0	0	0	RD/W		00-59	32kHz EN	10 SEC			1 SEC			
										*POR STATE	0	0	0	0	0	0	0	0
MINUTE	1	0	0	0	0	0	1	RD/W		00-59	ALM OUT	10 MIN			1 MIN			
										*POR STATE	0	0	0	0	0	0	0	0
HOUR	1	0	0	0	0	1	0	RD/W		00-23	12/24	0	10 HR	10 HR	1 HR			
										01-12	1/0		A/P 0/1					
										*POR STATE	0	0	0	0	0	0	0	0
DATE	1	0	0	0	0	1	1	RD/W		01-28/29 01-30 01-31	0	0	10 DATE		1 DATE			
										*POR STATE	0	0	0	0	0	0	0	1
MONTH	1	0	0	0	1	0	0	RD/W		01-12	0	0	0	10M	1 MONTH			
										*POR STATE	0	0	0	0	0	0	0	1
DAY	1	0	0	0	1	0	1	RD/W		01-07	0	0	0	0	0	WEEKDAY		
										*POR STATE	0	0	0	0	0	0	0	1
YEAR	1	0	0	0	1	1	0	RD/W		00-99	10 YEAR				1 YEAR			
										*POR STATE	0	1	1	1	0	0	0	0
CONTROL	1	0	0	0	1	1	1	RD/W			WP	0	0	0	0	0	0	0
										*POR STATE	0	0	0	0	0	0	0	0
CENTURY	1	0	0	1	0	0	1	RD/W		00-99	1000 YEAR				100 YEAR			
										*POR STATE	0	0	0	1	1	0	0	1

Note: *POR STATE defines power-on reset state of register content.

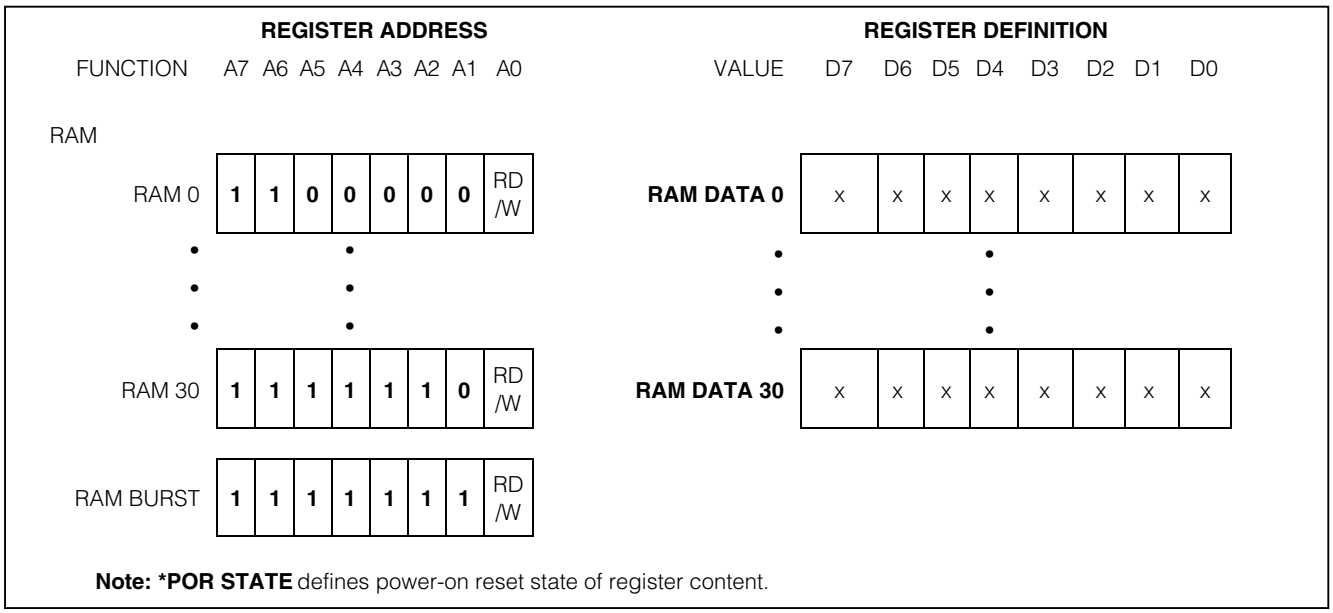
then read the Seconds register again (final-seconds). Check to see that final-seconds is equal to initial-seconds. If not, repeat the write process. If the Seconds register is to be written, update the Seconds register first, and then read it back and store its value (initial-seconds). Update the remaining timekeeping registers and then read the Seconds register again (final-sec-

Table 2. Register Address/Definition (continued)

FUNCTION	REGISTER ADDRESS A7	A6	A5	A4	A3	A2	A1	A0	REGISTER DEFINITION VALUE	D7	D6	D5	D4	D3	D2	D1	D0
ALARM CONFIG	**1**	**0**	**0**	**1**	**0**	**1**	**0**	RD /W		0	YEAR	DAY	MONTH	DATE	HOUR	MINUTE	SECOND
									***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RESERVED Do not write to this location.	1	0	0	1	0	1	1	RD /W		0	0	0	0	0	1	1	1
									***POR STATE**	0	0	0	0	0	1	1	1
ALARM THRESHOLDS																	
SECOND	**1**	**0**	**0**	**1**	**1**	**0**	**0**	RD /W	00-59	0	10 SEC			1 SEC			
									***POR STATE**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
MINUTE	**1**	**0**	**0**	**1**	**1**	**0**	**1**	RD /W	00-59	0	10 MIN			1 MIN			
									***POR STATE**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
HOUR	**1**	**0**	**0**	**1**	**1**	**1**	**0**	RD /W	00-23	12/24	0	10 HR	10 HR	1 HR			
									01-12	1/0		A/P 0/1					
									***POR STATE**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
DATE	**1**	**0**	**0**	**1**	**1**	**1**	**1**	RD /W	01-28/29 01-30 01-31	0	0	10 DATE		1 DATE			
									***POR STATE**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
MONTH	**1**	**0**	**1**	**0**	**0**	**0**	**0**	RD /W	01-12	0	0	0	10 M	1 MONTH			
									***POR STATE**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**
DAY	**1**	**0**	**1**	**0**	**0**	**0**	**1**	RD /W	01-07	0	0	0	0	0	WEEKDAY		
									***POR STATE**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
YEAR	**1**	**0**	**1**	**0**	**0**	**1**	**0**	RD /W	00-99	10 YEAR				1 YEAR			
									***POR STATE**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
CLOCK BURST	**1**	**0**	**1**	**1**	**1**	**1**	**1**	RD /W									

Note: *POR STATE defines power-on reset state of register content.

Table 2. Register Address/Definition (continued)



Note: *POR STATE defines power-on reset state of register content.

onds). Check to see that final-seconds is equal to initial-seconds. If not, repeat the write process.

Note: After writing to any time or date register, no read or write operations are allowed for 45µs.

AM/PM and 12Hr/24Hr Mode

Bit 7 of the Hours register selects 12hr or 24hr mode. When high, 12hr mode is selected. In 12hr mode, bit 5 is the AM/PM bit, logic high for PM. In 24hr mode, bit 5 is the second 10hr bit, logic high for hours 20 through 23.

Write-Protect Bit

Bit 7 of the Control register is the write-protect bit. When high, the write-protect bit prevents write operations to all registers except itself. After initial settings are written to the timekeeping registers, set the write-protect bit to logic 1 to prevent erroneous data from entering the registers during power glitches or interrupted serial transfers. The lower 7 bits (bits 0–6) are unusable, and always read zero. Any data written to bits 0–6 are ignored. Bit 7 must be set to zero before a single byte write to the clock, before a write to RAM, or during a burst write to the clock.

Example: Setting the Clock with a Burst Write

To set the clock with a Burst Write operation to 10:11:31PM, Thursday July 4th, 2002, write BEh as Address/Command byte, followed by 8 bytes, B1h, 11h, B0h, 04h, 07h, 04h, 02h, and 00h (Table 2). BEh accesses the Clock Burst Write register. The first byte, B1h, sets the Seconds register to 31, and disables the 32.768kHz output. The second byte, 11h, sets the Minutes register to 11. The third byte, B0h, sets the Hours register to 12hr mode, and 10PM. The fourth byte, 04h, sets the Date register (day of the month) to the 4th. The fifth byte, 07h, sets the Month register to July. The sixth byte, 04h, sets the Day register (day of the week) to Thursday. The seventh byte, 02h, sets the Year register to 02. The eighth byte, 00h, clears the write-protect bit of the Control register to allow writing to the MAX6901. The Century register is not accessed with a Burst Write and therefore must be written to separately to set the century to 20. Note the Century register corresponds to the thousand and hundred digits of the current year and defaults to 19.

Reading the Clock

Reading the Timekeeping Registers

The main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year) can be read with either Single Reads or a Burst Read. In the MAX6901, a latch buffers each clock counter's data. Clock counter data are latched by the 3-wire serial Read command (on the falling edge of SCLK, after the Address/Command byte has been sent by the Master to read a timekeeping register). Collision-detection circuitry ensures that this

Table 3. HEX Register Address/Description

WRITE ADDRESS/COMMAND BYTE (HEX)	READ ADDRESS/COMMAND BYTE (HEX)	DESCRIPTION	POR CONTENTS (HEX)
80	81	SECONDS	00
82	83	MINUTES	00
84	85	HOUR	00
86	87	DATE	01
88	89	MONTH	01
8A	8B	DAY	01
8C	8D	YEAR	70
8E	8F	CONTROL	00
90	91	RESERVED	Nonapplicable
92	93	CENTURY	19
94	95	ALARM CONFIGURATION	00
96	97	RESERVED	07
98	99	SECONDS ALARM THRESHOLD	7F
9A	9B	MINUTES ALARM THRESHOLD	7F
9C	9D	HOURS ALARM THRESHOLD	BF
9E	9F	DATE ALARM THRESHOLD	3F
A0	A1	MONTH ALARM THRESHOLD	1F
A2	A3	DAY ALARM THRESHOLD	07
A4	A5	YEAR ALARM THRESHOLD	FF
BE	BF	CLOCK BURST	Nonapplicable
C0	C1	RAM 0	Indeterminate
C2	C3	RAM 1	Indeterminate
C4	C5	RAM 2	Indeterminate
C6	C7	RAM 3	Indeterminate
C8	C9	RAM 4	Indeterminate
CA	CB	RAM 5	Indeterminate
CC	CD	RAM 6	Indeterminate
CE	CF	RAM 7	Indeterminate
D0	D1	RAM 8	Indeterminate
D2	D3	RAM 9	Indeterminate
D4	D5	RAM 10	Indeterminate
D6	D7	RAM 11	Indeterminate
D8	D9	RAM 12	Indeterminate
DA	DB	RAM 13	Indeterminate
DC	DD	RAM 14	Indeterminate
DE	DF	RAM 15	Indeterminate
E0	E1	RAM 16	Indeterminate
E2	E3	RAM 17	Indeterminate

Table 3. HEX Register Address/Description (continued)

WRITE ADDRESS/COMMAND BYTE (HEX)	READ ADDRESS/COMMAND BYTE (HEX)	DESCRIPTION	POR CONTENTS (HEX)
E4	E5	RAM 18	Indeterminate
E6	E7	RAM 19	Indeterminate
E8	E9	RAM 20	Indeterminate
EA	EB	RAM 21	Indeterminate
EC	ED	RAM 22	Indeterminate
EE	EF	RAM 23	Indeterminate
F0	F1	RAM 24	Indeterminate
F2	F3	RAM 25	Indeterminate
F4	F5	RAM 26	Indeterminate
F6	F7	RAM 27	Indeterminate
F8	F9	RAM 28	Indeterminate
FA	FB	RAM 29	Indeterminate
FC	FD	RAM 30	Indeterminate
FE	FF	RAM Burst	Nonapplicable

does not happen coincident with a Seconds counter increment to ensure accurate time data is being read. The clock counters continue to count and keep accurate time during the Read operation.

The simplest way to read the timekeeping registers is to use a Burst Read. In a Burst Read, the main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year) and the Control register are read sequentially in the order listed with the Seconds register first. They are read out as a group of eight registers, with 8 bits each. All timekeeping registers (except Century) are latched upon the receipt of the Burst Read command. The worst-case error between the "actual" time and the "read" time is 1 second for a normal data transfer.

The timekeeping registers may also be read using Single Reads. If Single Reads are used, it is necessary to do some error checking on the receiving end, because it is possible that the clock counters could change during the Read operations, and report inaccurate time data. The potential for error is when the Seconds register increments before all the registers are read. For example, suppose a carry of 13:59:59 to 14:00:00 occurs during Single Read operations. The net data read could be 14:59:59, which is erroneous. To prevent errors from occurring with Single Read operations, read the Seconds register first (initial-seconds) and store this value for future comparison. After the remaining timekeeping registers have been read, reread the Seconds register (final-seconds). Check that the final-seconds value equals the initial-seconds value; if not, repeat the entire Single Read process. Using Single Reads at a 100kHz serial speed, it takes under 2.5ms to read all seven of the timekeeping registers, including two reads of the Seconds register.

Example: Reading the Clock with a Burst Read

To read the time with a Burst Read, send BFh as the Address/Command byte. Then clock out 8 bytes, Seconds, Minutes, Hours, Date of the month, Month, Day of the week, Year, and finally the Control byte. All data are output LSB first. Decode the required information based on the register definitions listed in Table 2.

Using the Alarm

A polled alarm function is available by reading the ALM OUT bit. The ALM OUT bit is D7 of the Minutes timekeeping register. A logic 1 in ALM OUT indicates the alarm function is triggered. There are eight registers associated with the alarm function, seven programmable Alarm Threshold registers and one programmable Alarm Configuration register. The Alarm Configuration register determines which Alarm Threshold registers are compared to the timekeeping registers, and the ALM OUT bit sets if the compared registers are equal. Table 2 shows the function of each bit of the Alarm Configuration register. Placing a logic 1 in any given bit of the Alarm Configuration register enables the respec-

tive alarm function. For example, if the Alarm Configuration register is set to 0000 0011, ALM OUT is set when both the minutes and seconds indicated in the Alarm Threshold registers match the respective timekeeping registers. Once set, ALM OUT stays high until it is cleared by reading or writing to the Alarm Configuration register, or by reading or writing to any of the Alarm Threshold registers. The Alarm Configuration register is written with Address/Command 94h, and read with Address/Command 95h.

Using the On-Board RAM

The static RAM is 31 x 8 bits addressed consecutively in the RAM address space. Even-addressed commands (C0h–FCh) are used for Writes, and odd-addressed commands (C1h–FDh) are used for Reads. The contents of the RAM are static and remain valid for V_{CC} down to 2V. All RAM data are lost if power is cycled. The write-protect bit (bit 7 of the Control register), when high, disallows any changes to RAM.

3-Wire Serial Interface

Interfacing the MAX6901 with a microcontroller is accomplished by using a 3-wire, synchronous, serial interface. Required to communicate are a Chip Select signal (CS), a Serial Clock signal (SCLK), and a Data line (I/O).

All data transfers are framed by the CS signal that must be active-high for any data transfer to occur. At the beginning of any data transfer (rising edge of CS), SCLK should be low. This prevents the MAX6901 from misinterpreting the transition of CS as a high-to-low transition of SCLK (if SCLK were to be left high when CS transitions from a low to high). The first 8 bits sent after CS is pulled high by the microcontroller comprise the Address/Command Byte, which tells the MAX6901 if the data transfer is a read or a write, and which register is read to or written from. Data are clocked into the MAX6901, through the I/O pin, on the rising edges of SCLK, and data are clocked out on the falling edge of SCLK. Data format is always LSB first to MSB last. When CS is low, I/O is high impedance.

Single data transfer timing is shown in Figure 2. Burst-mode data transfer timing is shown in Figure 3. Detailed Read and Write timing diagrams are shown in Figures 4 and 5, respectively.

Chip Select

CS serves two functions. First, CS turns on the control logic that allows access to the Shift register for Address/Command and data transfer. Second, CS provides a method of terminating either single-byte or multiple-byte data transfers. All data transfers are initiated by driving CS high. If CS is low, I/O is high impedance. At power-up, CS must be low until $V_{CC} \geq 2.0V$.

Serial Clock

A clock cycle on SCLK is a rising edge followed by a falling edge. For data input, data must be valid at I/O during the rising edge of the clock. For data outputs, bits are valid on I/O after the falling edge of clock. Also, SCLK must be low when CS is driven high.

Data Input (Single-Byte Write)

Following the eight SCLK cycles that input a Single-Byte Write Address/Command, data bits are input on the rising edges of the next eight SCLK cycles. Additional SCLK cycles are ignored. Input data LSB first.

Data Input (Burst Write)

Following the eight SCLK cycles that input a Burst Write Address/Command, data bits are input on the rising edges of the following SCLK cycles. The number of clock cycles depends on whether the timekeeping registers or RAM are being written. A clock Burst Write requires an Address/Command byte, 7 timekeeping data bytes, and 1 Control register byte. A Burst Write to RAM may be terminated after any complete data byte by driving CS low. Input data LSB first (Figures 3 and 5).

Data Output (Single-Byte Read and Burst Read)

A read from the MAX6901 is initiated by an Address/Command Write from the microcontroller (master) to the MAX6901 (slave). The Address/Command Write portion of the data transfer is clocked into the MAX6901 on rising clock edges. On the eighth rising SCLK edge, the last bit of the Address/Command Byte is clocked into the MAX6901. After t_{CDH} (CLK to Data Hold time, Figure 4), the microcontroller must release the data line. On the eighth falling edge of SCLK, the MAX6901 takes control of the data line and begins to output data.

The MAX6901 outputs data on the falling edge of SCLK after t_{CDD} (CLK to Data Delay time, Figure 4). On the next rising edge of SCLK, I/O goes to high impedance after t_{CCZ} (which is specified with a maximum time). Minimum time for t_{CCZ} can be 0ns. Since the I/O line can go to high impedance on the rising edge of SCLK, it is best to read the data from the MAX6901 before the rising edge of SCLK but after t_{CDD} (CLK to Data Delay time). This is best accomplished through the microcontroller I/O port pins by writing a low to SCLK, waiting t_{CDD} (CLK to Data Delay time), reading the MAX6901 I/O pin, and then writing a high to SCLK. Data bytes are output LSB first. Additional SCLK cycles transmit additional data bits, as long as CS remains high. This permits continuous burst-mode read capability.

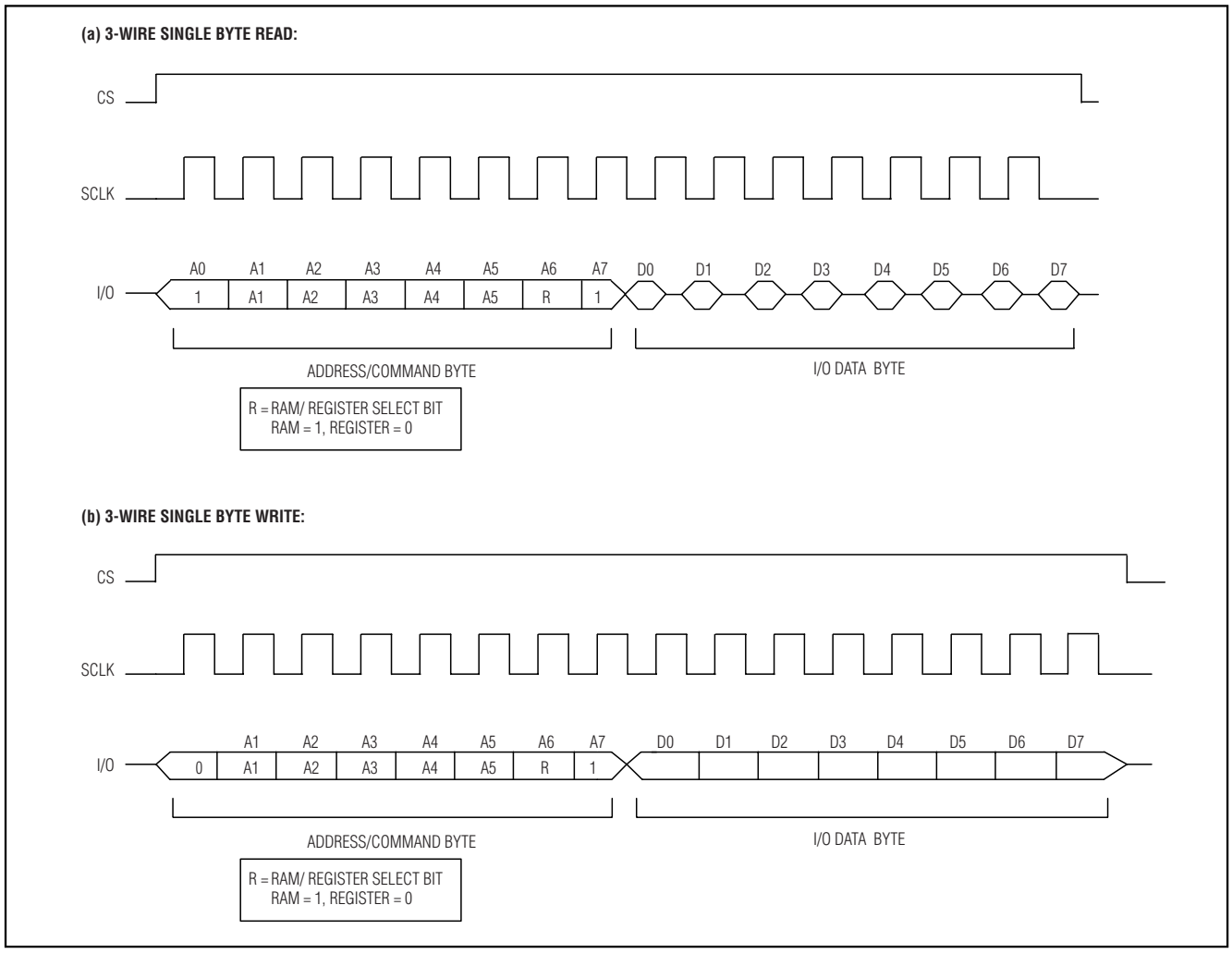


Figure 2. Single Byte Data Transfer

32.768kHz Output (32KHZ)

32KHZ is a push-pull 32.768kHz output for timing or clocking of external devices. Bit D7 in the Clock Seconds register is the active-low enable bit for 32KHZ. When D7 is logic 0, 32KHZ is enabled. When logic 1, 32KHZ is disabled and set to high impedance. Power-on reset enables the 32.768kHz output.

Applications Information

Crystal Selection

The MAX6901 is designed to use a standard 32.768kHz watch crystal. Table 1 details the recommended crystal requirements. Some suggested crystals are listed in Table 4. In addition to the specified SMT devices, some of the listed manufacturers also offer other package options.

Frequency Stability and Temperature

Timekeeping accuracy of the MAX6901 is dependent on the frequency stability of the external crystal. To determine frequency stability, use the parabolic curve in Figure 6 and the following equations:

$$\Delta f = fk (T_0 - T)^2$$

where:

Δf = change in frequency from +25°C

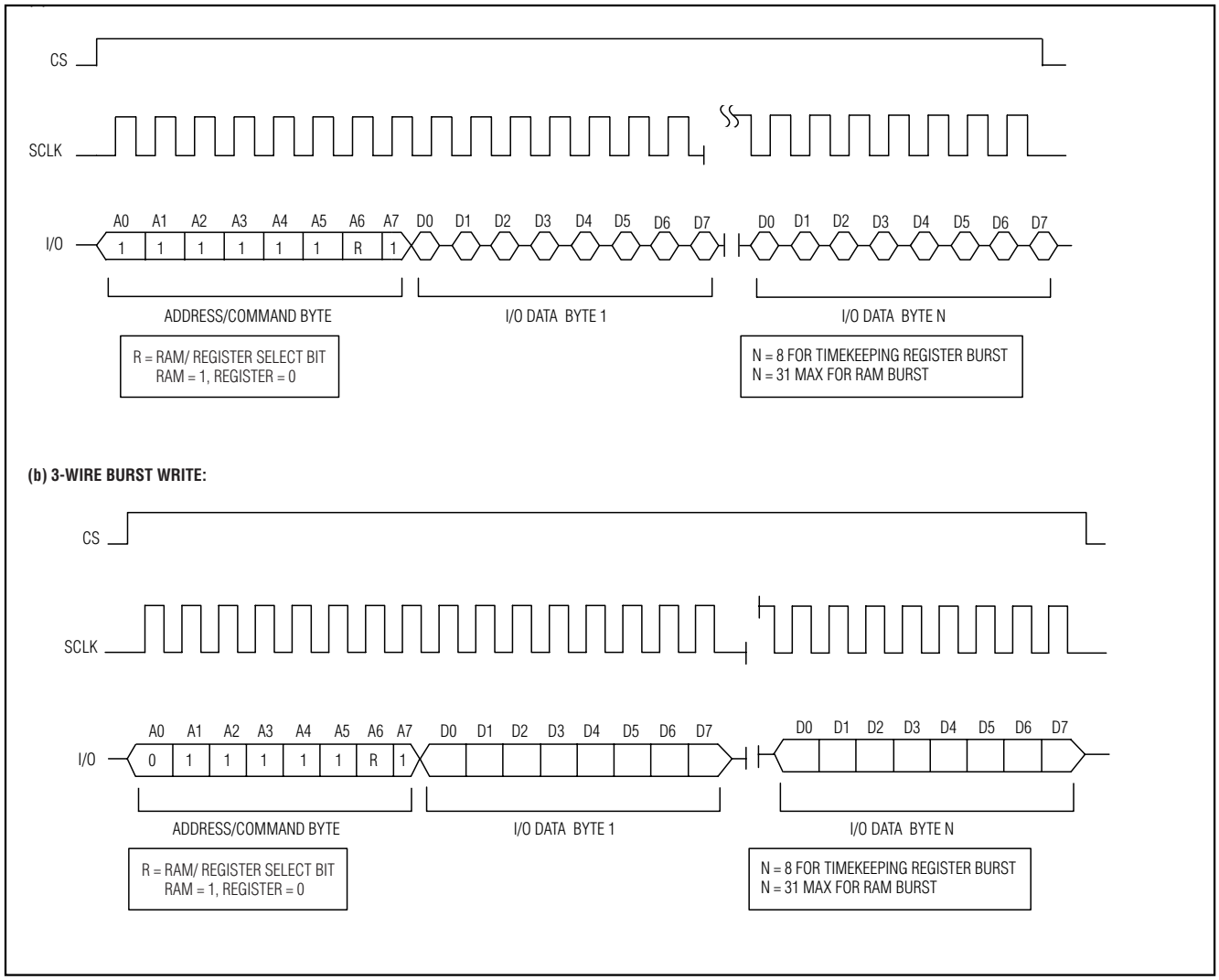


Figure 3. Burst Mode Data Transfer

f = nominal crystal frequency

k = parabolic curvature constant (-0.035ppm/°C2 ±0.005ppm/°C2 for 32.768kHz watch crystals)

T_0 = turnover temperature (+25°C ±5°C for 32.768kHz watch crystals)

T = temperature of interest (°C)

For example: What is the worst-case change in oscillator frequency from +25°C ambient to +45°C ambient?

$$\Delta f_{drift} = 32{,}768 \times (-0.04 \times (1 \times 10^{-6})) \times (20-45)^2$$
$$= -0.8192Hz$$

What is the worst-case timekeeping error per second?

Error due to temperature drift:

$$\Delta t_{drift} = \{[1 / [(f+\Delta f_{drift}) / 32768]]-1s\} / 1s$$

$$\Delta t_{drift} = \{[1 / [(32768 - 0.8192) / 32768]]-1\}/1s$$
$$= 0.000025s/s$$

Error due to +25°C initial crystal tolerance of ±20ppm:

$$\Delta f_{initial} = 32{,}768 \times (-20 \times ((1 \times 10\text{-}6)) = -0.65536Hz$$

$$\Delta t_{initial} = \{[1 / [(f+\Delta f_{initial}) / 32768]]-1s\} / 1s$$

$$\Delta t_{initial} = \{[1 / [(32768-0.65536) / 32768]]-1\} / 1s$$
$$= 0.000025s/s$$

Total timekeeping error per second:

3-Wire Serial RTC in a TDFN

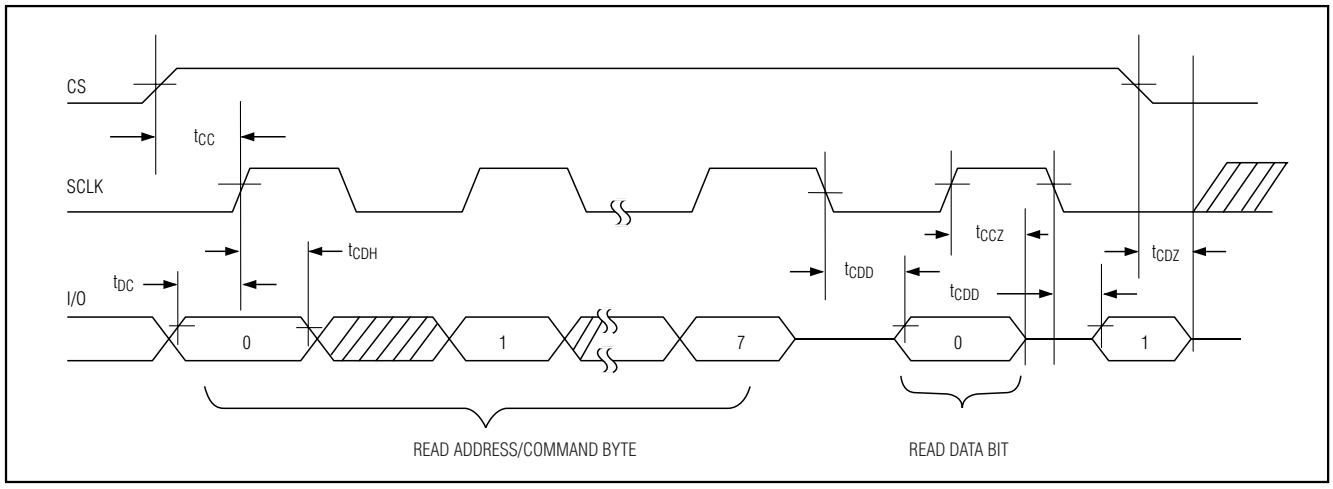


Figure 4. 3-Wire Read Data Transfer Serial Timing Diagram

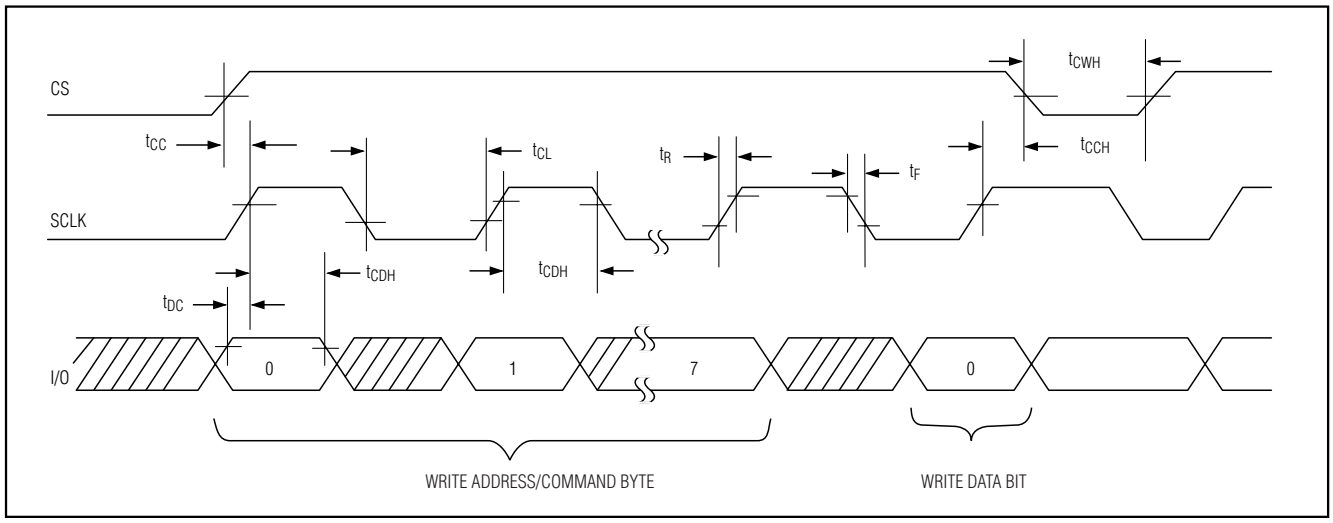


Figure 5. 3-Wire Write Data Transfer Serial Timing Diagram

$$\Delta t_{total} = \Delta t_{drift} + \Delta t_{initial}$$

$$\Delta t_{total} = 0.00002+0.000025=0.000045s/s$$

$$\Delta t = \left(31\,days\right)\times\left(24\frac{hr}{day}\right)\times\left(60\frac{min}{hr}\right)\times\left(60\frac{s}{min}\right)\times$$

$$\left(0.00045s/s\right)=120.528s$$

Total worst-case timekeeping error at the end of 1 month at +45°C is about 120s or 2 min (assumes negligible parasitic layout capacitance).

Oscillator Start Time

The MAX6901 oscillator typically takes 5s to 10s to begin oscillating. To ensure the oscillator is operating correctly, the software should validate proper timekeeping. This is accomplished by reading the Seconds register. Any reading of 1s or more from the POR value of zero is a validation of proper startup.

Power-On Reset

The MAX6901 contains an integral POR circuit that ensures all registers are reset to a known state on power-up. Once V_{CC} rises above 1.6V (typ), the POR circuit releases the registers for normal operation. When

Table 4. 32.768kHz Surface-Mount Watch Crystals

MANUFACTURER	MANUFACTURER PART NO.	TEMP. RANGE	C_L (pF)	+25°C FREQUENCY TOLERANCE (ppm)
Abracon Corporation	ABS25-32.768-12.5-B-2-T	-40°C to +85°C	12.5	±20
Caliber Electronics	AWS2A-32.768kHz,	-20°C to +70°C	12.5	±20
ECS INC International	ECS-.327-12.5-17	-10°C to +60°C	12.5	±20
Fox Electronics	FSM327	-40°C to +85°C	12.5	±20
M-tron	SX2010/ SX2020	-20°C to +75°C	12.5	±20
Raltron	RSE-32.768-12.5-C-T	-10°C to +60°C	12.5	±20
SaRonix	32S12A	-40°C to +85°C	12.5	±20

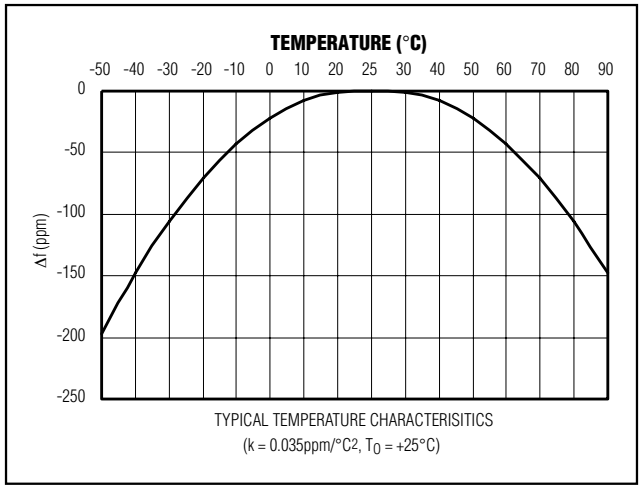


Figure 6. Typical Temperature Curve for 32.768kHz Watch Crystal

V_{CC} drops to less than 1.6V (typ), the MAX6901 resets all register contents to the POR defaults (Table 2).

RESERVED Registers

Addresses/Commands 90h, 91h, 96h, and 97h are reserved for factory testing ONLY. Do not write to these registers. If inadvertent Writes are done to any of these registers, cycle power to the MAX6901.

Power-Supply Considerations

For most applications, a 0.1µF capacitor from V_{CC} to GND provides adequate bypassing for the MAX6901. A series resistor can be added to the supply line for operation in extremely harsh or noisy environments.

Timekeeping Current—Normal Operation

When I/O is high impedance (CS = low, or after each rising-clock edge for a data output transfer), there is a potential for increased timekeeping current (up to 100x) if the I/O is allowed to float. If minimum timekeeping current is desired, the microcontroller port pin should be configured as an input with a weak pullup. Alternatively, use a 100k Ω or less pulldown or pullup resistor (for microcontroller port pins with ≤1µA input leakage).

There are similar considerations for 32KHZ if it is placed in its high-impedance state. For lowest timekeeping current, it should not be allowed to float. Force it high or low, or terminate it with a pullup or pulldown resistor.

Timekeeping Current—Battery Backup Systems

Often times, an RTC is operated in a system with a backup battery. A microprocessor supervisory circuit with backup battery switchover, or other switching arrangement, is used to switch power from V_{CC} to V_{BATT} when V_{CC} falls below a set threshold. Most of these systems leave only the RTC and some SRAM to run from V_{BATT}. The microcontroller that communicates with the RTC is powered only from V_{CC}. When the microcontroller is reset, its port pins typically become high impedance. This essentially floats I/O, CS, and SCLK on the MAX6901. There is a potential for increased timekeeping current (up to x100) as V_{CC} falls through the linear region of the input gates for I/O, SCLK, and CS. The duration of this effect depends on the discharge rate of V_{CC}. To minimize current draw from V_{BATT} in such systems, ensure that V_{CC} falls rapidly at power down. One option is a V_{CC} discharge resistor of 100kΩ or less from V_{CC} to ground. This also ensures sufficient impedance when V_{CC} is gone back through the microcontroller's ESD protection, to keep I/O, SCLK, and CS from floating. Alternately, a 100k Ω pulldown (for microcontroller port pins with ≤1µA input leakage) on each pin (I/O, SCLK, and CS) ensures that timekeeping current specifications are met during the power switchover.

3-Wire Serial RTC in a TDFN

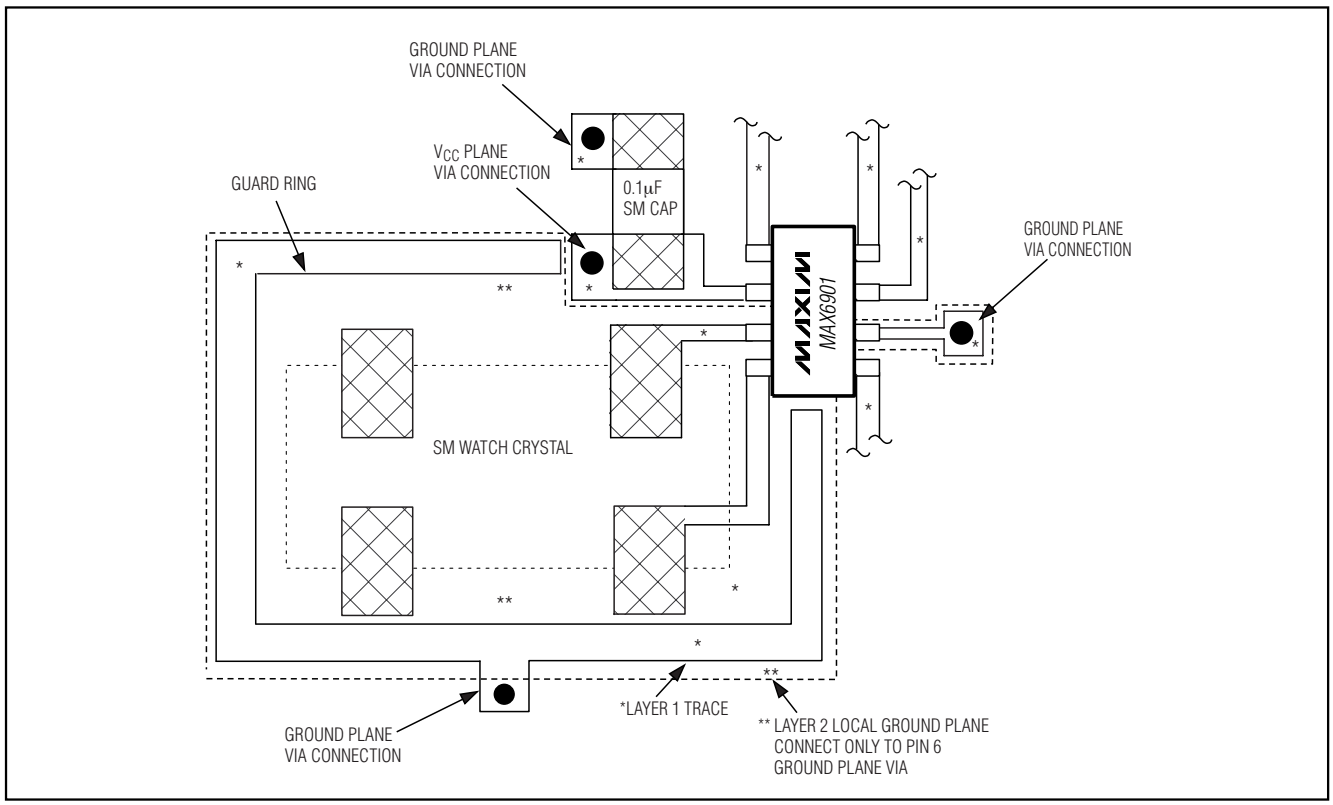


Figure 7. Printed Circuit Board Layout for Crystal Connections

There are similar considerations for 32KHZ if it is placed in its high-impedance state. For lowest timekeeping current, it should not be allowed to float. Force it high or low, or terminate it with a pullup or pulldown resistor.

PC Board Layout Considerations

The MAX6901 uses a very-low-current oscillator to minimize supply current. This causes the oscillator pins, X1 and X2, to be relatively high impedance. Exercise care to prevent unwanted noise pickup.

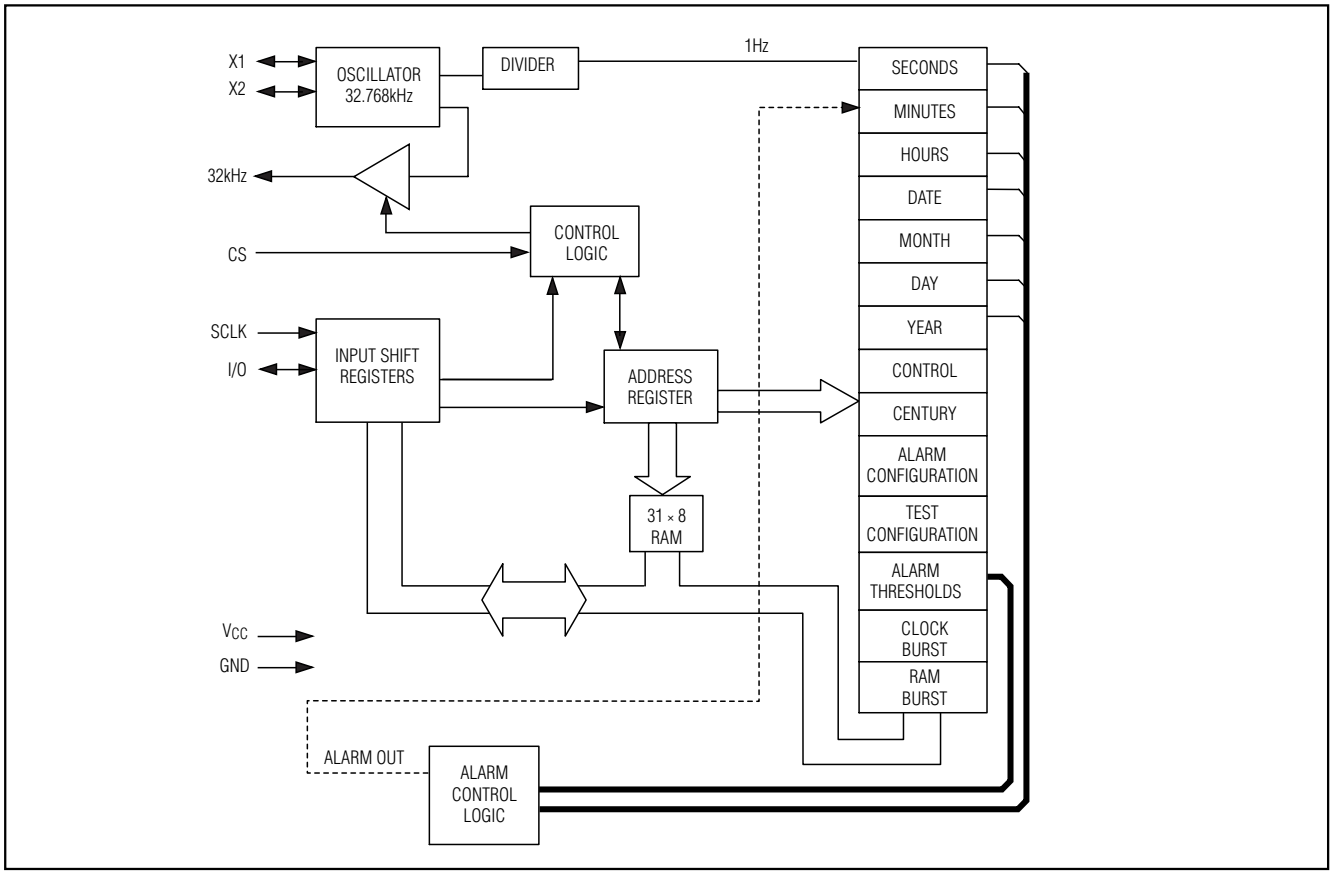
Connect the 32.768kHz crystal directly across X1 and X2 of the MAX6901. To eliminate unwanted noise pickup, design the PC board using these guidelines (Figure 7): place the crystal as close to X1 and X2 as possible and keep the trace lengths short; place a guard ring around the crystal, X1 and X2 traces (where applicable), and connect the guard ring to GND; keep all signal traces away from beneath the crystal, X1, and X2. Finally, an additional local ground plane can be added under the crystal on an adjacent PC board layer. The plane should be isolated from the regular PC board ground plane, and tied to ground at the MAX6901 ground pin. Restrict the plane to be no larger than the perimeter of the guard ring. Do not allow this ground plane to contribute significant capacitance between X1 and X2.

Chip Information

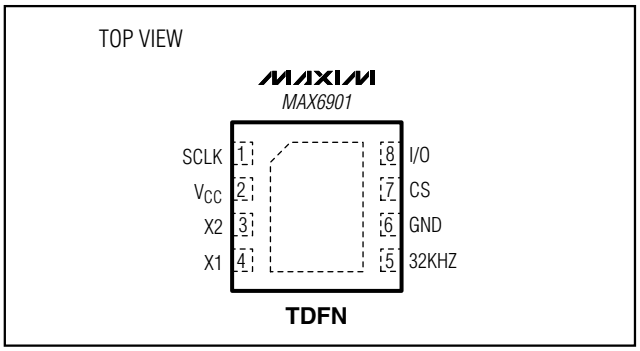
TRANSISTOR COUNT: 26,214

PROCESS: CMOS

Functional Diagram



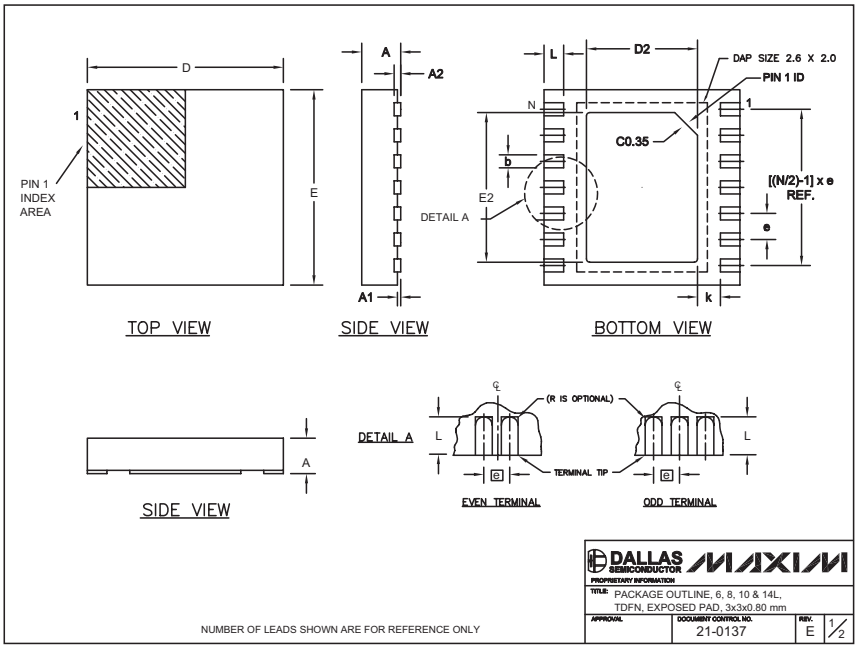
Pin Configuration



3-Wire Serial RTC in a TDFN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline info rmation go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.03	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1.
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 6, 8, 10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. E
2/2

Mouser Electronics

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Maxim Integrated:

MAX6901ETA-T