+48V, Single-Port Network Power Switch For Power-Over-LAN

ABSOLUTE MAXIMUM RATINGS

(All voltages with respect to AGND_S, unless otherwise noted.)
IN .....-0.3V to +76V
UVLO .....-0.3V to +6V
V_{DIG} to DGND .....-0.3V to +6V
OUT .....-0.3V to (V_{DRAIN} + 0.3V)
DRAIN .....-0.3V to (V_{IN} + 0.3V)
RDT .....-0.3V to +12V
RCL to IN .....-10V to +0.3V
EN, DET_DIS, DCA, CLASS, ZC_EN, and LATCH to DGND .....-0.3V to +6V
POK, $\overline{ZC}$, CL0, CL1, CL2, and $\overline{FAULT}$ to DGND .....-0.3V to +6V
DGND .....-5V to +5V
Maximum Current into Drain 0.8A
Maximum Current into POK, $\overline{ZC}$, CL0, CL1, CL2, $\overline{FAULT}$ ...20mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP (Derate 12.8mW/°C above +70°C) 1026mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 48V, V_{DIG} = 3.3V, AGND_S = AGND = DGND = 0V, R_{SENSE} = 0.5Ω ±1%, UVLO = open, EN = V_{DIG}, R_{RCL} = 150Ω ±1%, R_{RDT} = 18.2kΩ ±1%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Input Voltage Range	V_{IN}			32		60	V
Analog Input Supply Current	I_{IN}	V_{IN} = 60V, measured at AGND after OUT has stopped slewing			1	1.6	mA
Digital Input Voltage Range	V_{DIG}			1.65		5.50	V
Digital Input Supply Current	I_{DIG}	V_{DIG} = 5V			0.05	0.1	mA
DGND to AGND Operating Voltage Range				-4		+4	V
Current-Limit Response Time		OUT shorted to AGND (Note 2)			1		µs
OUT Current-Limit Foldback Voltage	V_{FBSTOP}	(Note 3)			18		V
Current-Limit Sense Voltage (V_{IN} - V_{DRS}) (Note 4)	V_{ILIM}	Maximum voltage across R_{SENSE} at V_{OUT} > V_{FBSTOP}		198	212	223	mV
		0°C to +70°C		203	212	221	
Current-Limit Sense Foldback Voltage (V_{IN} - V_{DRS})	V_{ILIM_fb}	V_{OUT} = 0V		64	70	76	mV
Overcurrent Timeout	t_{OC}	OUT shorted to AGND (Note 5)		50	60	75	ms
D_{MOS} On-Resistance	R_{DSON}	I_{OUT} = 100mA	T_A = +25°C		0.45		Ω
			T_A = +85°C			0.75	
Power-Off OUT Sink Current		EN = DGND, V_{OUT} = 48V				15	µA
Maximum Output Voltage Slew Rate	dV_{OUT}/dt	V_{OUT} rising, no load			100		V/ms
Maximum Output Current Slew Rate	dI_{OUT}/dt	V_{OUT} rising, C_{LOAD} = 100µF			35		A/ms
Power-OK Threshold (V_{IN} - V_{OUT})	V_{THPOK}	V_{OUT} rising, POK from low to high		650	750	850	mV
		Hysteresis			10		%
POK Output Low Voltage	V_{POK_LOW}	I_{POK} = 3mA				0.4	V
POK Output Leakage Current		V_{POK} = 3.3V			0.05	1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 48V, V_{DIG} = 3.3V, AGND_S = AGND = DGND = 0V, R_{SENSE} = 0.5Ω ±1%, UVLO = open, EN = V_{DIG}, R_{RCL} = 150Ω ±1%, R_{RDT} = 18.2kΩ ±1%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POK Output Delay (Note 6)	t_{POK_LOW}	POK from high to low, V_{OUT} falling		1.0	1.4	1.8	ms
	t_{POK_HIGH}	POK from low to high, V_{OUT} rising		74	88	102	
Zero-Current Detection Threshold Voltage (V_{IN} - V_{DRS})	V_{ZCTH}	(Note 4)		2.7	3.75	4.8	mV
$\overline{ZC}$ Output Low Voltage	$V_{\overline{ZC}\_LOW}$	$I_{\overline{ZC}}$ = 3mA				0.4	V
$\overline{ZC}$ Output Leakage Current		$V_{\overline{ZC}}$ = 3.3V			0.05	1	µA
Zero-Current Detection Delay	t_{ZCDEL}	$\overline{ZC}$ from high to low, I_{OUT} falling (Note 7)		300	350	400	ms
Zero-Current Deglitch Time	t_{ZC_DEG}	I_{OUT} rising			10		ms
Thermal Shutdown		Temperature rising			150		°C
		Hysteresis			30		°C
Shutdown Autorestart Time	$t_{RESTART}$	LATCH = low (Note 8)		1.60	1.92	2.24	s
UNDERVOLTAGE LOCKOUT							
Default V_{IN} UVLO	$UVLO_{TH}$	UVLO floating, V_{IN} rising	MAX5922A	36	38	40	V
			MAX5922B/ MAX5922C	26	28	30	
		Hysteresis	MAX5922A		4.4		
			MAX5922B/C		2.5		
UVLO Comparator Threshold	V_{REF}	Referenced to AGND_S, V_{UVLO} rising	MAX5922A	1.36	1.38	1.41	V
			MAX5922B/ MAX5922C	1.31	1.33	1.36	
		Hysteresis	MAX5922A		160		mV
			MAX5922B/ MAX5922C		120		
UVLO Input Resistance				50			kΩ
LOGIC SIGNALS							
EN, LATCH, DCA, DET_DIS CLASS, and ZC_EN Input High Voltage	V_{IH}	1.65V < V_{DIG} < 5.5V		0.7 × V_{DIG}			V
EN, LATCH, DCA, DET_DIS CLASS, and ZC_EN Input Low Voltage	V_{IL}	1.65V < V_{DIG} < 2.0V				0.3 × V_{DIG}	V
		2.0V < V_{DIG} < 5.5V				0.8	
EN, LATCH, DCA, DET_DIS CLASS, and ZC_EN Input Current				-1		+1	µA
EN Low Pulse Width				3			µs
$\overline{FAULT}$, CL0, CL1 and CL2, Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
$\overline{FAULT}$, CL0, CL1 and CL2, Output Leakage Current		$V_{\overline{FAULT}}$ = V_{CL0} = V_{CL1} = V_{CL2} = 3.3V, CLASS = 0V			0.05	1	µA

+48V, Single-Port Network Power Switch For Power-Over-LAN

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 48V, V_{DIG} = 3.3V, AGND_S = AGND = DGND = 0V, R_{SENSE} = 0.5Ω ±1%, UVLO = open, EN = V_{DIG}, R_{RCL} = 150Ω ±1%, R_{RDT} = 18.2kΩ ±1%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PD DETECTION (See Figure 3, *PD Detection* Section)						
Detection Probe Voltage Phase I	V_{PBI}	R_{PD} = 19kΩ to 26.5kΩ	3.6	4	4.4	V
Detection Probe Voltage Phase II	V_{PBII}	R_{PD} = 19kΩ to 26.5kΩ	7.2	8	8.8	V
Detection Short-Circuit Current	I_{SC_DET}	OUT shorted to AGND	0.68		1.50	mA
Valid PD Detected Lower-Limit Threshold	R_{PDL}	(Note 9)	15		19	kΩ
Valid PD Detected Upper-Limit Threshold	R_{PDH}	(Note 9)	26.5		33.0	kΩ
Total Detection Time	t_{det}			170	196	ms
Reject Capacitance During Detection	C_{PDH}	R_{PD} = 19kΩ to 26.5kΩ	6			µF
Allowable Capacitance During Detection	C_{PDL}	R_{PD} = 19kΩ to 26.5kΩ			0.6	µF
PD CLASSIFICATION (See *PD Classification Mode* Section)						
Classification Probe Voltage	V_{CLASS}	I_{OUT} = 0.5mA to 45mA	15		20	V
		No load			28	
Classification Short-Circuit Current	I_{SC_CLASS}	Shorted to AGND	48		65	mA
Classification Time Duration	t_{CLASS}	From detection completion	15	21.3	26	ms
Total Detection and Classification Delay Time	t_{TOT}	From channel-enabled to power delivered at the OUT pin		191	230	ms
Class 0 to Class 1 Threshold	I_{CLASS_1L}		5.5	6.5	7.5	mA
Class 1 to Class 2 Threshold	I_{CLASS_1-2}		13	14.5	16	mA
Class 2 to Class 3 Threshold	I_{CLASS_2-3}		21	23	25	mA
Class 3 to Class 4 Threshold	I_{CLASS_3-4}		31	33	35	mA
Default To Class 0 High-Current Lower-Limit Threshold	I_{CLASS_4-0}		43	46.5		mA
Collision Detection Delay Time (MAX5922A/MAX5922C Only)	t_{DCA}	DCA = high, R_{PD} = 15kΩ	2.38	2.8	3.22	s

Note 1: All specifications are 100% production tested at T_A = +25°C, unless otherwise noted. All temperature limits are guaranteed by design.

Note 2: This is the time from an output overcurrent or short-circuit condition until the output goes into regulated current limit.

Note 3: OUT voltage above which the output current limit is at its full value (see Figure 8).

Note 4: To be consistent with the IEEE 802.3af standard, choose R_{SENSE} = 0.5Ω ±1%.

Note 5: This is the time the part stays in current-limit mode during overload condition. After t_{OC} elapses (or when the junction temperature hits +150°C) the part shuts down.

Note 6: See the *Typical Operating Characteristics* and Figure 6.

Note 7: This is the delay from I_{OUT} falling below the zero-current threshold until $\overline{ZC}$ goes low and the IC shuts down (see the *Zero-Current Detection* section).

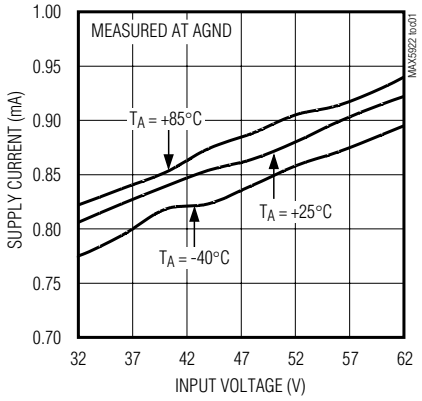
Note 8: See the *Fault Management* section.

Note 9: PD is detected by the procedures specified by the IEEE 802.3af standard. A probe voltage V_{PBI} (+4V typically) is forced at OUT and the current I_{S1} is measured after t_{DET}/2. A second probe voltage V_{PBII} (+8V typically) is then forced and I_{S2} measured after t_{DET} / 2 again. The voltage increment is then divided by the difference of the two currents (I_{S2} - I_{S1}). This is the PD resistance value.

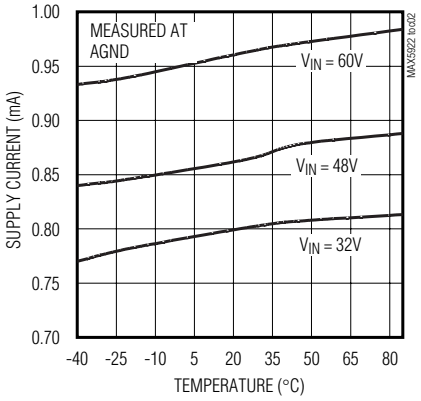
Typical Operating Characteristics

(MAX5922A, V_{IN} = 48V, V_{DIG}, EN, LATCH, CLASS, and ZC_EN = 3.3V, DCA, AGND_S = AGND = DGND = 0V, R_{SENSE} = 0.5Ω ±1%, UVLO floating, R_{RCL} = 150kΩ, R_{RDT} = 18.2kΩ, T_A = +25°C, unless otherwise noted.)

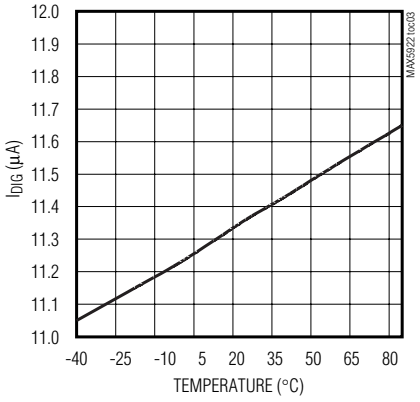
V_{IN} SUPPLY CURRENT vs. INPUT VOLTAGE



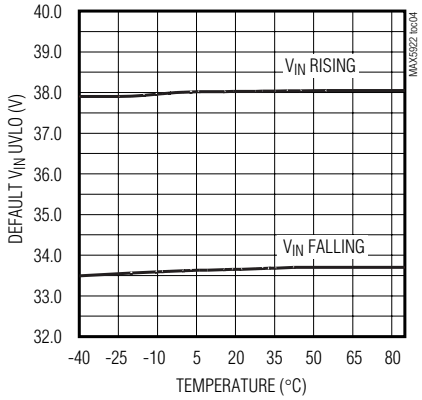
V_{IN} SUPPLY CURRENT vs. TEMPERATURE



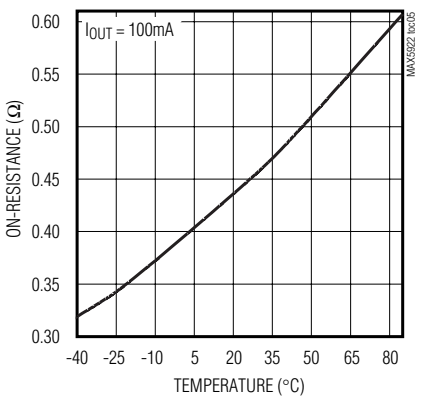
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



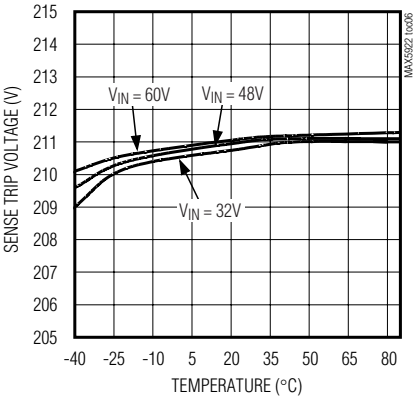
V_{IN} UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



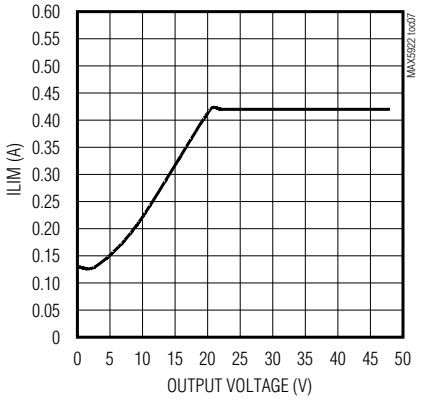
MOSFET R_{DSON} vs. TEMPERATURE



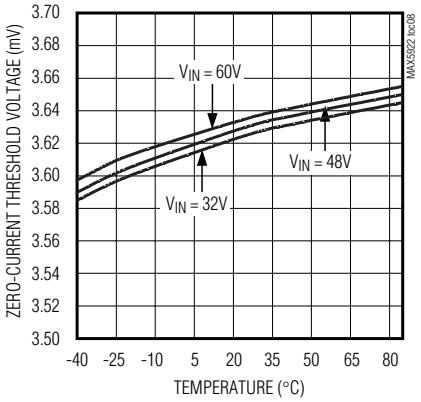
SENSE TRIP VOLTAGE vs. TEMPERATURE



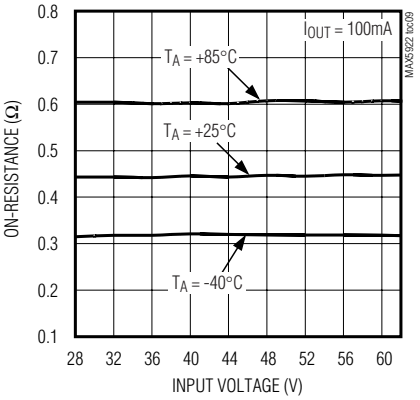
FOLDBACK-CURRENT LIMIT (ILIM vs. V_{OUT})



ZERO-CURRENT DETECTION THRESHOLD VOLTAGE vs. TEMPERATURE



ON-RESISTANCE vs. V_{DRAIN}

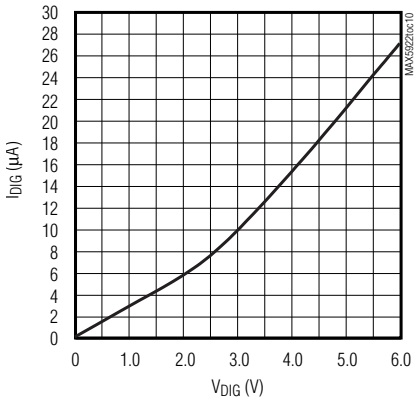


+48V, Single-Port Network Power Switch For Power-Over-LAN

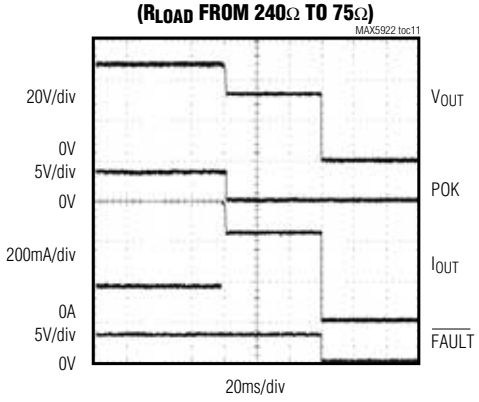
Typical Operating Characteristics (continued)

(MAX5922A, V_{IN} = 48V, V_{DIG}, EN, LATCH, CLASS, and ZC_EN = 3.3V, DCA, AGND_S = AGND = DGND = 0V, R_{SENSE} = 0.5Ω ±1%, UVLO floating, R_{RCL} = 150kΩ, R_{RDT} = 18.2kΩ, T_A = +25°C, unless otherwise noted.)

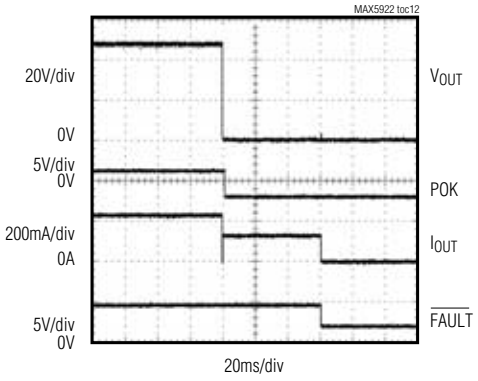
DIGITAL SUPPLY CURRENT vs. V_{DIG}



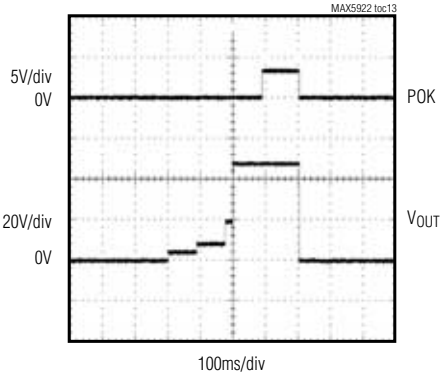
OVERCURRENT TIMEOUT (R_{LOAD} FROM 240Ω TO 75Ω)



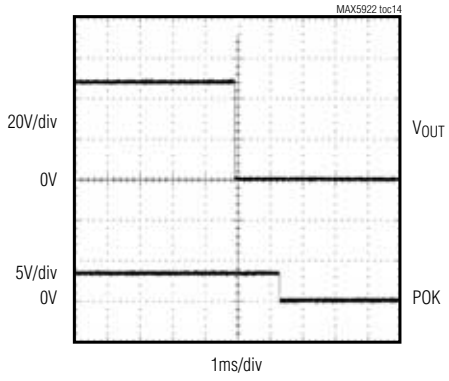
SHORT-CIRCUIT RESPONSE TIME



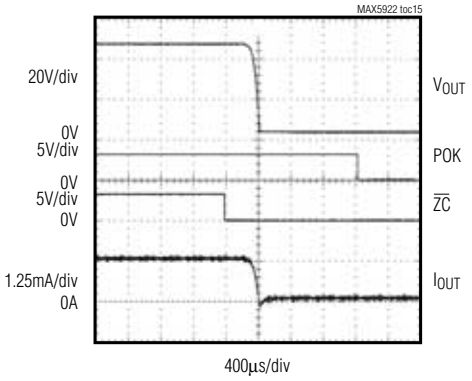
POK LOW-TO-HIGH DELAY TIME



POK HIGH-TO-LOW DELAY TIME



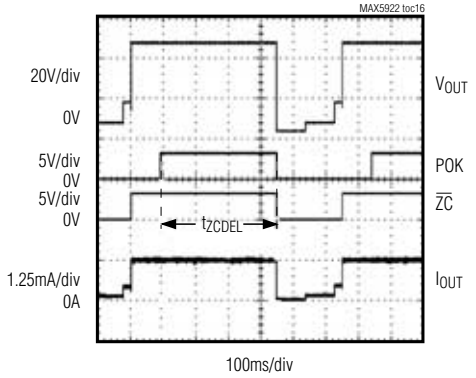
$\overline{ZC}$ TO OUT DELAY



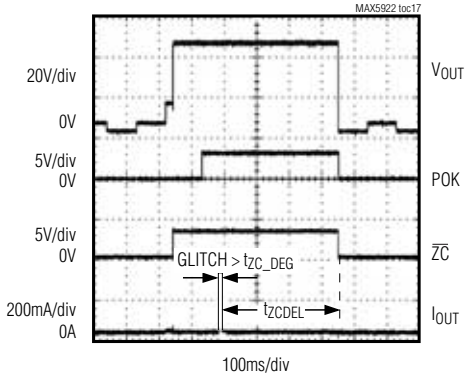
Typical Operating Characteristics (continued)

(MAX5922A, V_{IN} = 48V, V_{DIG}, EN, LATCH, CLASS, and ZC_EN = 3.3V, DCA, AGND_S = AGND = DGND = 0V, R_{SENSE} = 0.5Ω ±1%, UVLO floating, R_{RCL} = 150kΩ, R_{RDT} = 18.2kΩ, T_A = +25°C, unless otherwise noted.)

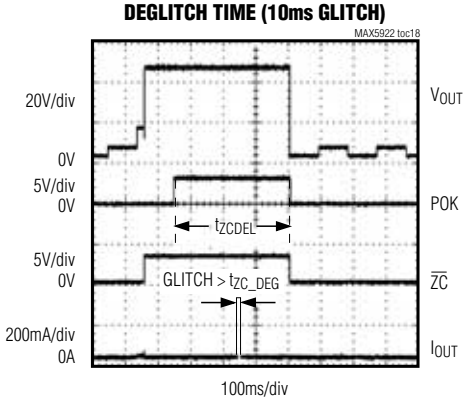
ZERO-CURRENT HIGH-TO-LOW DETECTION TIME



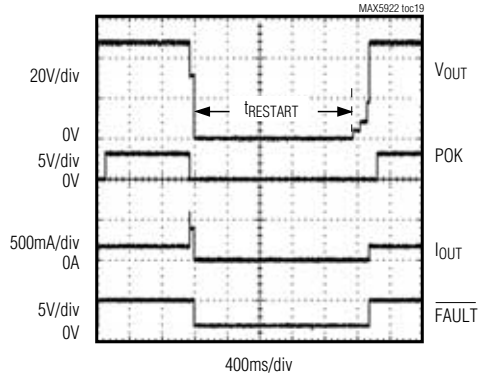
ZERO-CURRENT (IIms GLITCH) DEGLITCH TIME



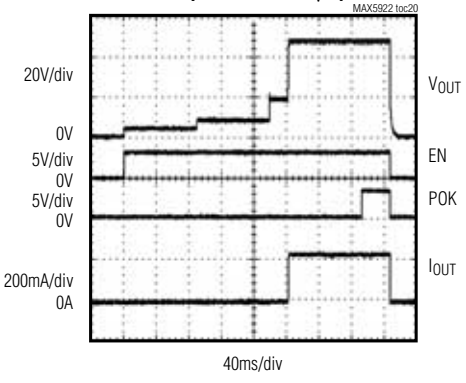
ZERO-CURRENT DEGLITCH TIME (10ms GLITCH)



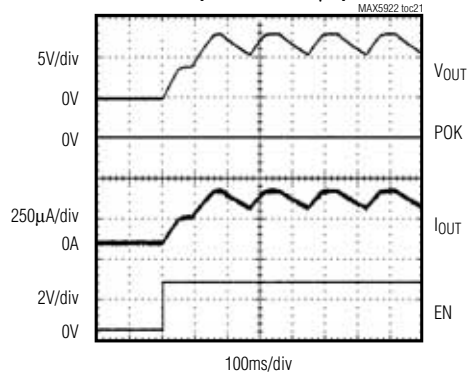
OVERCURRENT RESTART DELAY



STARTUP WITH VALID PD (25kΩ AND 0.1μF)



STARTUP WITH INVALID PD (25kΩ AND 10μF)

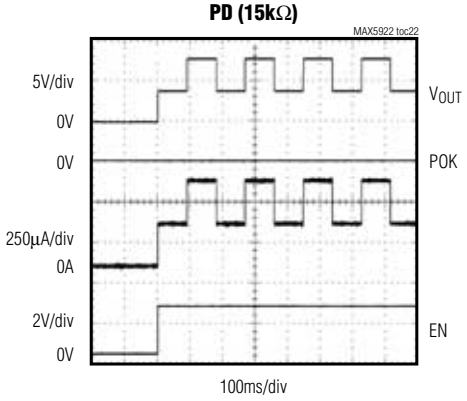


+48V, Single-Port Network Power Switch For Power-Over-LAN

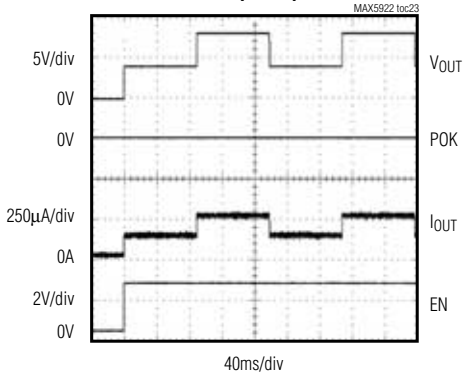
Typical Operating Characteristics (continued)

(MAX5922A, V_{IN} = 48V, V_{DIG}, EN, LATCH, CLASS, and ZC_EN = 3.3V, DCA, AGND_S = AGND = DGND = 0V, R_{SENSE} = 0.5Ω ±1%, UVLO floating, R_{RCL} = 150kΩ, R_{RDT} = 18.2kΩ, T_A = +25°C, unless otherwise noted.)

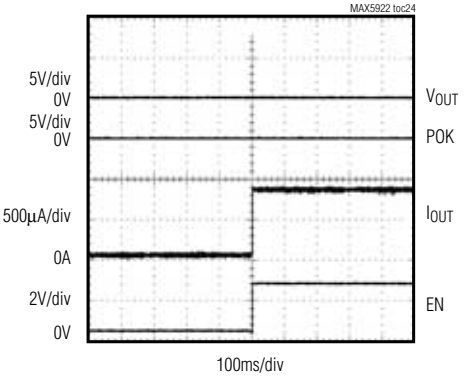
STARTUP WITH INVALID PD (15kΩ)



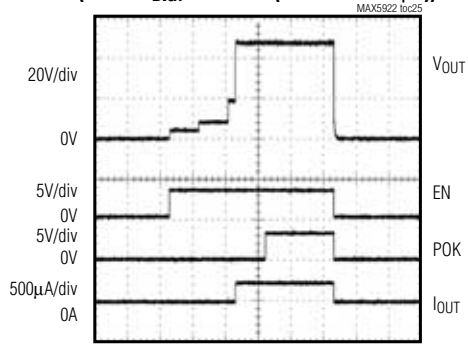
STARTUP WITH INVALID PD (33kΩ)



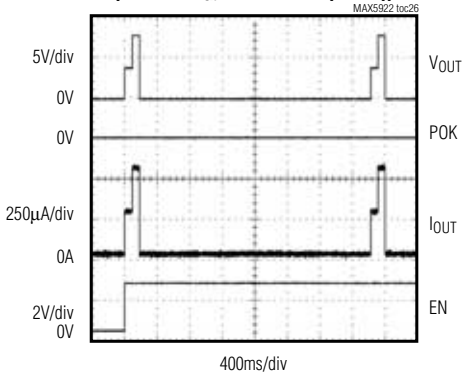
STARTUP WITH OUTPUT SHORTED TO AGND



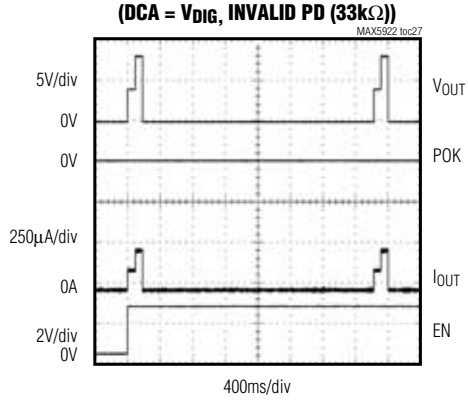
STARTUP WITH MIDSPAN MODE (DCA = V_{DIG}, VALID PD (25kΩ AND 0.1µF))



STARTUP WITH MIDSPAN MODE (DCA = V_{DIG}, INVALID PD (15kΩ))



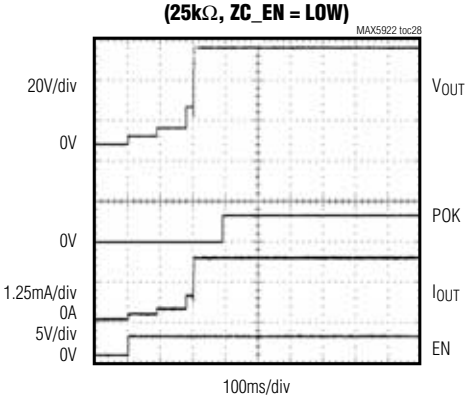
STARTUP WITH MIDSPAN MODE (DCA = V_{DIG}, INVALID PD (33kΩ))



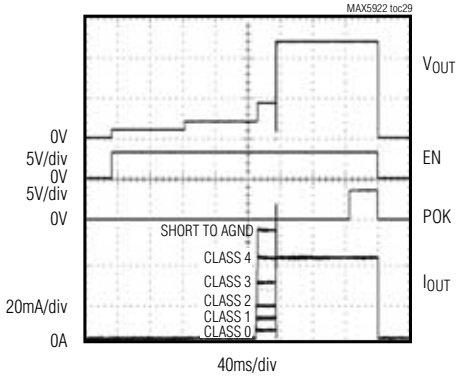
Typical Operating Characteristics (continued)

(MAX5922A, V_{IN} = 48V, V_{DIG}, EN, LATCH, CLASS, and ZC_EN = 3.3V, DCA, AGND_S = AGND = DGND = 0V, R_{SENSE} = 0.5Ω ±1%, UVLO floating, R_{RCL} = 150kΩ, R_{RDT} = 18.2kΩ, T_A = +25°C, unless otherwise noted.)

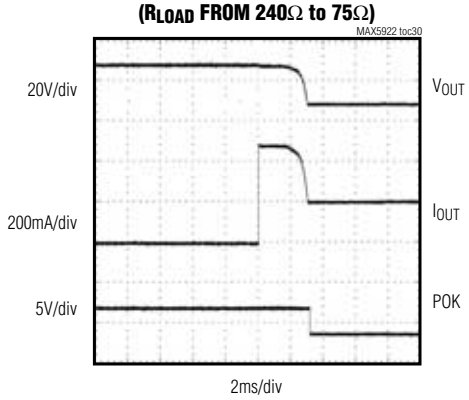
STARTUP WITH VALID PD (25kΩ, ZC_EN = LOW)



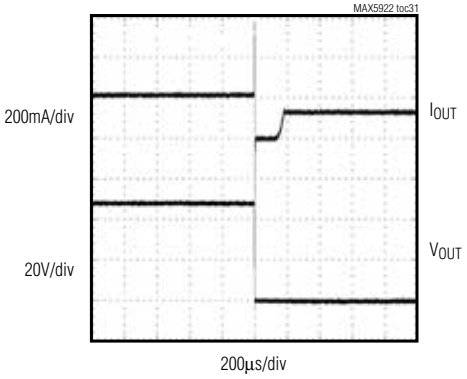
STARTUP WITH DIFFERENT PD CLASSES



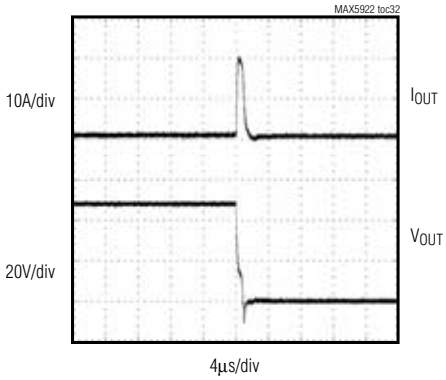
OVERCURRENT TIMEOUT (R_{LOAD} FROM 240Ω to 75Ω)



OUTPUT SHORT-CIRCUIT RESPONSE



OUTPUT SHORT-CIRCUIT RESPONSE



+48V, Single-Port Network Power Switch For Power-Over-LAN

Pin Description

PIN	NAME	FUNCTION
*	AGND	Analog Ground. This is the return of analog power input. AGND can vary ±4V from DGND. AGND and DGND must be connected together at a single point in the system.
1, 2	DRAIN	Drain connection for the integrated MOSFET. Connect a sense resistor, R_{SENSE}, from DRAIN to IN. These pins are also the current-sense resistor negative terminal. R_{SENSE} sets the overcurrent-limit and open-circuit detection threshold. These two pins must be connected together.
3, 6, 26	N.C.	No Connection. Not internally connected. Leave pins 6 and 26 open. Pins 6 and 26 are left unconnected to provide additional spacing between the high-voltage pins and other pins.
4	IN	Input Voltage. Connect to a positive voltage source between +32V to +60V from IN to AGND. This is the current-sense resistor positive terminal. Bypass to AGND with a 47µF, 100V electrolytic capacitor and a 0.1µF, 100V ceramic capacitor. Place the ceramic capacitor close to this pin.
5	RCL	Classification Sense Resistor. Connect a 150Ω ±1% resistor from RCL to IN for sensing the classification current. Leave RCL floating when the PD classification function is not used.
7	AGND_S	Analog Ground Sense. Connect a 1Ω resistor from AGND_S to AGND. This resistor protects the IC during an output short-circuit condition.
8	UVLO	Undervoltage Lockout Adjustment Input. Referenced to AGND. Connect to the center point of a resistive-divider from IN to AGND to adjust the UVLO threshold. Leave open for default value.
9	RDT	Detection Sense Resistor. Connect an 18.2kΩ ±1% resistor from RDT to AGND for sensing the PD detection current. Add a 680nF capacitor in parallel to this resistor to filter out the power-line noise. Connect RDT to AGND when the PD detection function is not used.
10	$\overline{FAULT}$	Fault Signal Open-Drain Logic Output. Reference to DGND. $\overline{FAULT}$ is latched low when: 1. An overtemperature condition occurs and/or, 2. An overcurrent condition that has lasted for more than t_{OC}.
11	POK	Power-OK, Open-Drain Logic Output. Reference to DGND. POK goes open drain a time t_{POK_HIGH} after V_{OUT} raises to within V_{THPOK} from V_{IN}. POK goes low a time t_{POK_LOW} after V_{OUT} falls out of the V_{THPOK} from V_{IN}.
12	$\overline{ZC}$	Zero-Current Fault Signal. Open-drain logic output. Reference to DGND. $\overline{ZC}$ is latched low when there is a zero-current condition lasting longer than t_{ZCDEL}. $\overline{ZC}$ is open-drain otherwise. The zero-current detection circuit is enabled immediately after the POK signal goes high. The $\overline{ZC}$ is unlatched after a valid PD has been detected and eventually classified.
13	TP1	Must be Left Open or Connected to AGND
14	TP2	Must be Left Open or Connected to AGND
15	TP3	Must be Left Open or Connected to AGND
16	CL2	Classification Report Logic Output Bit 2. See the *PD Classification* section (Table 2).
17	CL1	Classification Report Logic Output Bit 1. See the *PD Classification* section (Table 2).
18	CL0	Classification Report Logic Output Bit 0. See the *PD Classification* section (Table 2).
19	DGND	Digital Ground. DGND can vary ±4V from AGND. DGND and AGND must to be connected together at a single point in the system.
20	LATCH	Fault Management Selection Digital Input. Referenced to DGND. Connect to a logic high to latch off after a fault condition. Connect to a logic low for automatic restart after a fault condition (see the *Fault Management* section).

**This is not a device pin.*

Pin Description (continued)

PIN	NAME	FUNCTION
21	ZC_EN	Zero-Current-Detection Enable Logic Input. Referenced to DGND. Connect ZC_EN to a logic high to enable the zero-current detection circuitry. Connect ZC_EN to a logic low to disable this function.
22	EN	ON/OFF Control-Logic Input. Referenced to DGND. Connect to a logic high to enable the device. Connect to a logic low to disable the device and reset a latched-off condition.
23	V_{DIG}	Digital Supply Voltage. V_{DIG} is the supply voltage for the internal digital logic circuity. EN, LATCH, CLASS, DET_DIS, DCA, and ZC_EN input logic thresholds are automatically scaled to the voltage on V_{DIG}. See the *Typical Application Circuit* for proper filtering.
24	CLASS	Classification Enable Digital Input. Connect to DGND to disable the classification function. Connect to V_{DIG} to enable the classification function.
25	DET_DIS	PD Detection Disable Logic Input. When DET_DIS is connected to a logic high, the part skips the detection and classification (regardless of the status of CLASS) phases and powers on immediately after EN = high (MAX5922B/MAX5922C only).
	DCA	Detection Collision Avoidance Logic Input. Connect to a logic high to activate the detection collision avoidance circuitry for midspan system. Connect to DGND to disable this function. (MAX5922A only). See the *Detection Collision Avoidance* section.
27, 28	OUT	Output Voltage

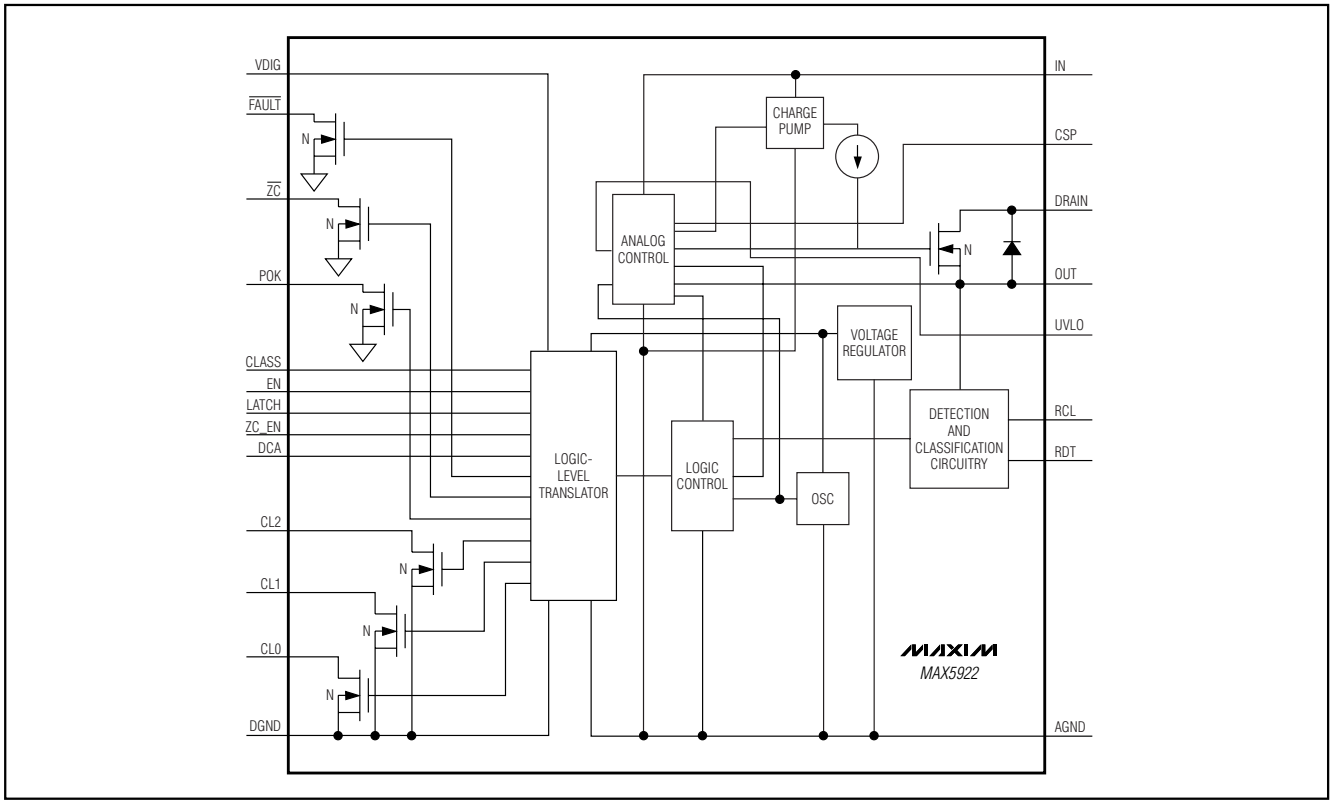


Figure 1. MAX5922 Block Diagram

+48V, Single-Port Network Power Switch For Power-Over-LAN

Detailed Description

The MAX5922 is a single-port network power controller with an integrated power MOSFET, operating from a +32V to +60V supply rail. The device is specifically designed for PSE in power-over-LAN applications and is fully compliant to the IEEE 802.3af standard. The MAX5922 provides PD discovery, classification, current limit, and other necessary functions for an IEEE 802.3af-compliant PSE.

The MAX5922 operates in three different modes: PD detection mode, PD classification mode, and power mode. Figures 2 and 4 illustrates the device's functional operation.

PD Detection Mode

Once powered up and enabled, the MAX5922 probes the output for a valid PD. A valid PD should have a 25kΩ discovery signature characteristic as specified in the IEEE 802.3af standard. Table 1 shows the IEEE 802.3af specification for a PSE detection of PDs (see the *Typical Application Circuit* and Figure 3 (MAX5922 startup sequence)).

The MAX5922 performs the PD detection by forcing a probe voltage (V_{PBI} = 4V) at the OUT pin and senses the current out of this pin. The sensed current is sampled and held t_{DET} (88ms) after the probing voltage is sent. The probe voltage is then switched to V_{PBII} = 8V. At the end of another t_{DET} period, the ratio of the difference of the two test voltages and sensed currents (ΔV/ΔI) is calculated to determine the PD resistance. The MAX5922 PD detection circuitry checks for a valid PD resistive signature between 19kΩ and 26.5kΩ, with a parallel capacitance of up to 0.6µF. The MAX5922 PD detection circuit rejects all PDs showing resistive signature of less than 15kΩ or greater than 33kΩ, and/or a capacitive signature greater than 6µF. Any resistive signature between 15kΩ to 19kΩ, or between 26.5kΩ to 33kΩ, and/or a capacitance between 0.6µF to 6µF can produce unpredictable detection results. If the MAX5922 does not detect a valid PD signature, it continually sends the probe voltages to the output indefinitely (see Figure 5).

The detection current reference is set by an external resistor (R_{RDT}) connected from the RDT pin to AGND. This resistor should be an 18.2kΩ ±1%, with an optional 680nF capacitor in parallel for filtering out power-line noise. An internal diode in series with the detection voltage source and OUT is provided to restrict PD detection to the 1st quadrant as specified by the IEEE standard 802.3af (see Figure 3). To prevent damage to non-PD devices and to protect itself from output short circuit, the MAX5922 limits the current out of the OUT pin during PD detection to 1.5mA (max).

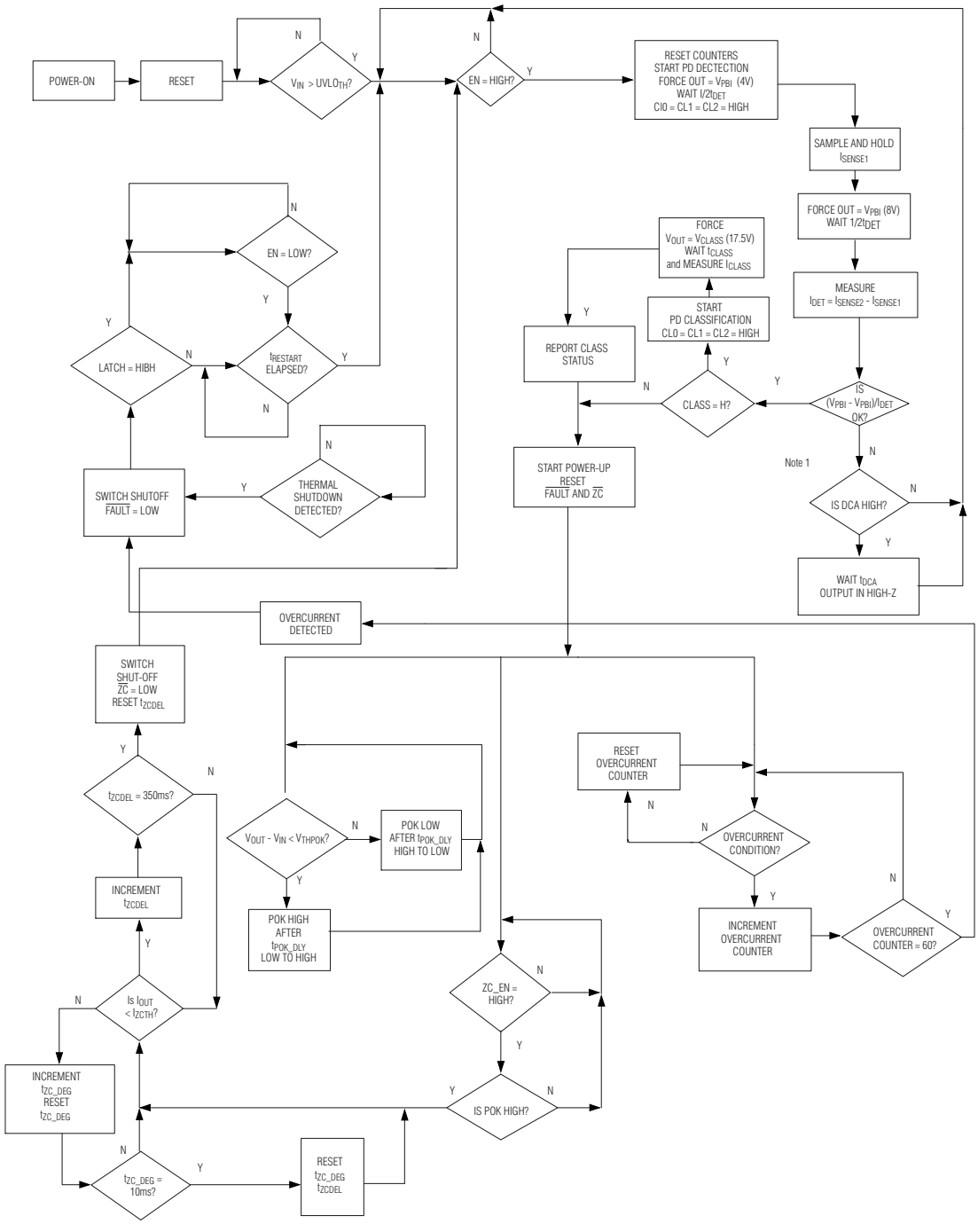
Table 1. IEEE802.3af PD Specification

PARAMETER	VALID PD DETECTION SIGNATURE	NON-VALID PD DETECTION SIGNATURE
V/I (Slope)	19kΩ < R_{PD} < 26.5kΩ	15kΩ > R_{PD} or R_{RD} > 33kΩ
Input Capacitance	C_{PD} < 0.6µF	C_{PD} > 6µF
Offset Voltage	Up to 2.0V	—
Current Offset	Up to 12µA	—

For midspan systems where power is delivered to the PD through the spare pairs, the detection collision avoidance must be activated. In this mode, after every failed PD detection cycle, the MAX5922A/MAX5922C enter a back-off mode where they drive the OUT pin into high impedance for t_{DCA} (2.8s). The DCA pin must be connected high (MAX5922A) to activate the detection collision avoidance circuitry (if connected low, the detection collision avoidance circuitry is disabled). The MAX5922C has the detection collision avoidance circuitry permanently enabled (see the *Typical Application Circuit*). After t_{DCA}, the MAX5922A (with DCA high) and the MAX5922C resume PD detection operation. The MAX5922B has the detection collision avoidance circuitry permanently disabled.

Detection Enable/Disable

The MAX5922A has the PD detection mode permanently enabled. The MAX5922B/MAX5922C are equipped with a DET_DIS pin, which provides the option of enabling or disabling the power-device detection phase. With the DET_DIS pin connected high, the PD detection and classification phases are disabled regardless of the status of the class pin. With the DET_DIS pin connected low, the PD detection is enabled.



*FOR THE MAX5922B, THE DCA FUNCTION IS INTERNALLY DISABLED. FOR THE MAX5922C, THE DCA FUNCTION IS INTERNALLY ENABLED.

Figure 2. Operational Flow Chart (MAX5922A and MAX5922B/MAX5922C with DET_DIS Connected Low)

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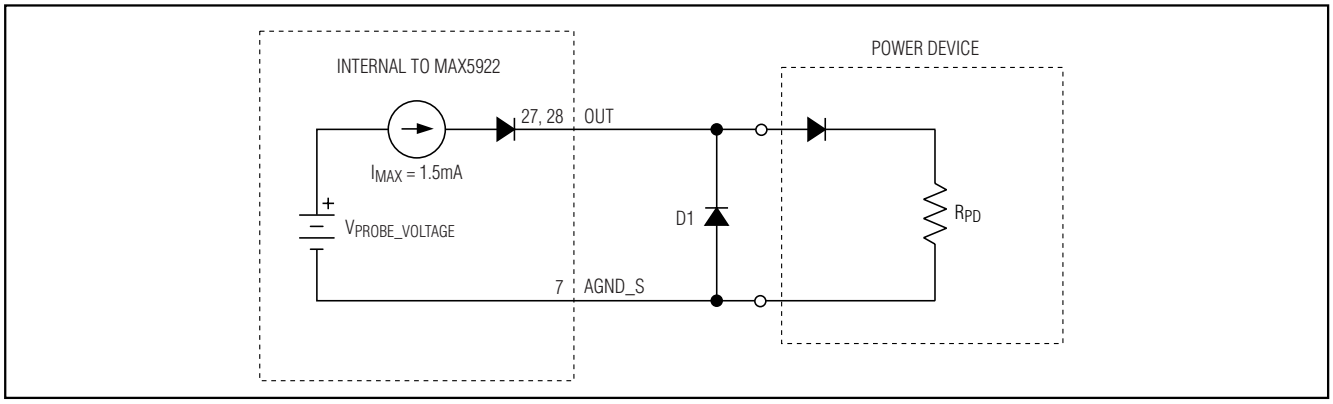

Figure 3. PSE Detection Source

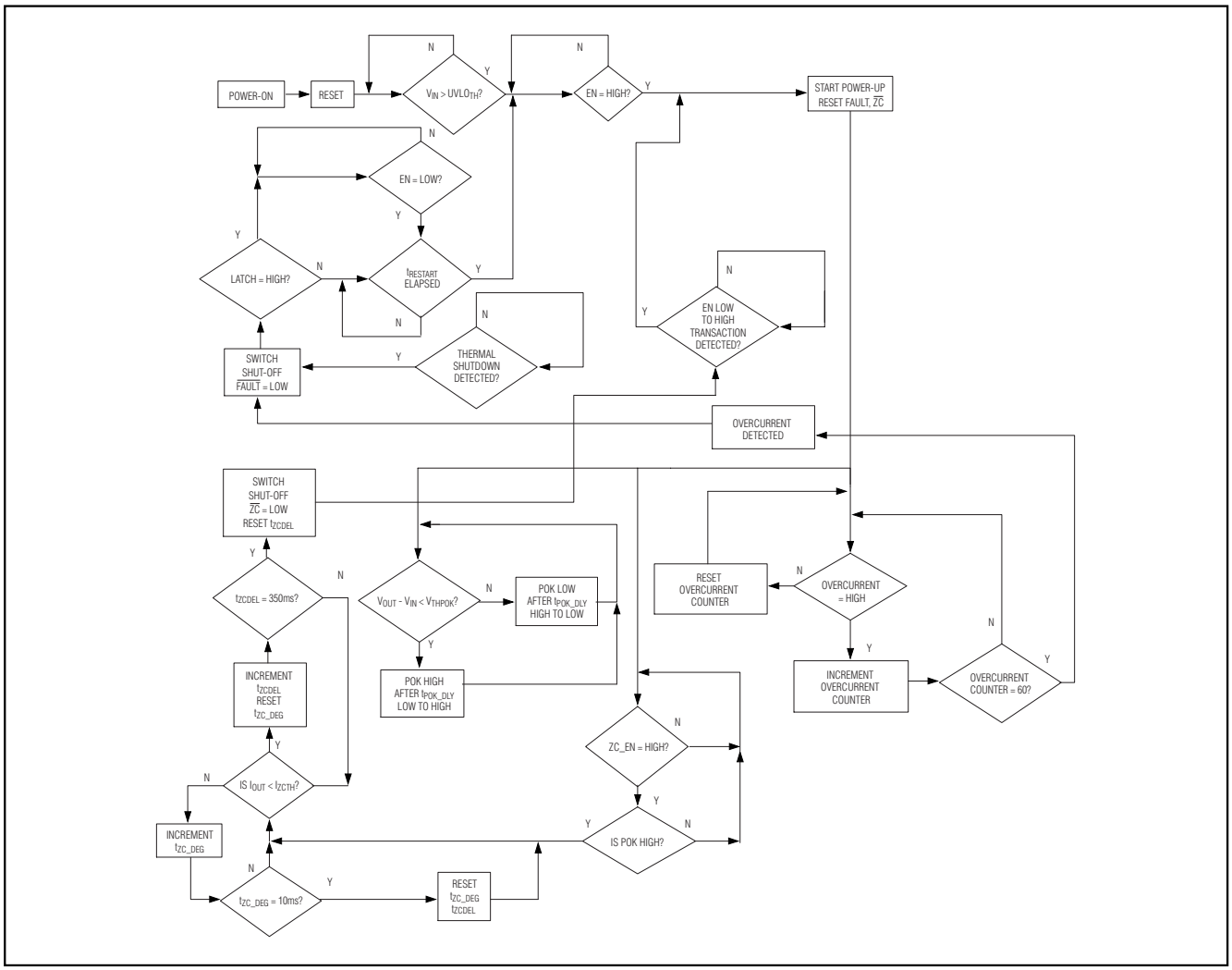

Figure 4. Operational Flow Chart (MAX5922B/MAX5922C with DET_DIS Connected High)

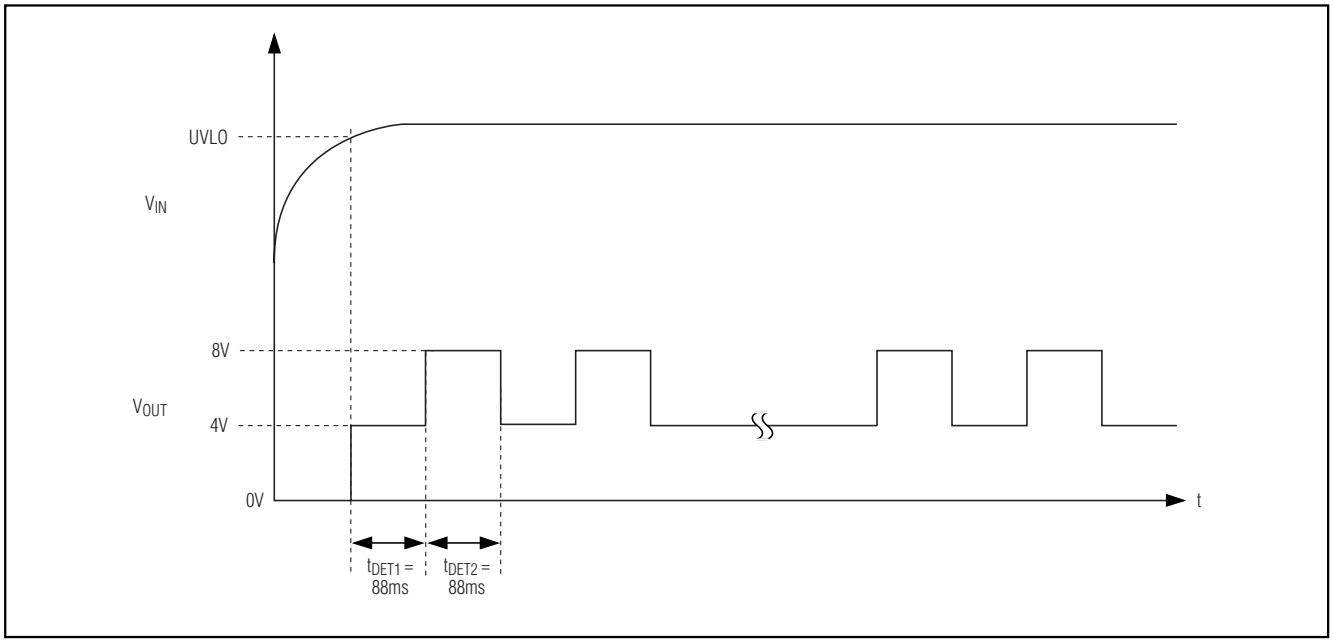

Figure 5. PD Detection with an Invalid PD Signature

Table 2. PD Classification Threshold Limits

SENSED CURRENT (mA)	CL2	CL1	CL0	CLASS TYPES
0.5 to 4 or above 43	0	0	0	Class 0
9 to 12	0	0	1	Class 1
17 to 20	0	1	0	Class 2
26 to 30	0	1	1	Class 3
36 to 42	1	0	0	Class 4
N/A	1	0	1	Not used
N/A	1	1	0	Successful detection (classification disabled or DET_DIS = low)
Power device not detected yet or CLASS pin connected low.	1	1	1	Detection ongoing

PD Classification Mode (PD Classification)

Following a valid PD detection, and if the CLASS pin is high, the MAX5922 enters the PD classification mode. If the CLASS pin is low, the PD classification mode is skipped and the MAX5922 goes directly from PD detection to the power mode. During the PD classification mode, the MAX5922 forces a probe voltage (17.5V) at the OUT pin and measures the current out of this pin. The measured current determines the class of the PD. The classification results are reported at the classification logic outputs CL0, CL1, CL2. Table 2 shows the classification threshold limits and the corresponding logic outputs CL0, CL1, and CL2.

Connect an external 150Ω ±1% resistor (R_{RCL}) from RCL to IN to set the classification current reference. If the PD classification function is not used, RCL can be left floating. For the MAX5922B/MAX5922C, the DET_DIS pin must be connected low to enable the classification phase. If DET_DIS is connected high, the classification phase is disabled regardless of the state of the CLASS pin. After the classification phase, the MAX5922 enters power-up.

Power-Up Mode

After the PD is successfully detected and classified, the MAX5922 enters power-up mode. During this mode, the MAX5922 gradually turns on the integrated N-channel MOSFET. To minimize EMI, the MAX5922 limits the

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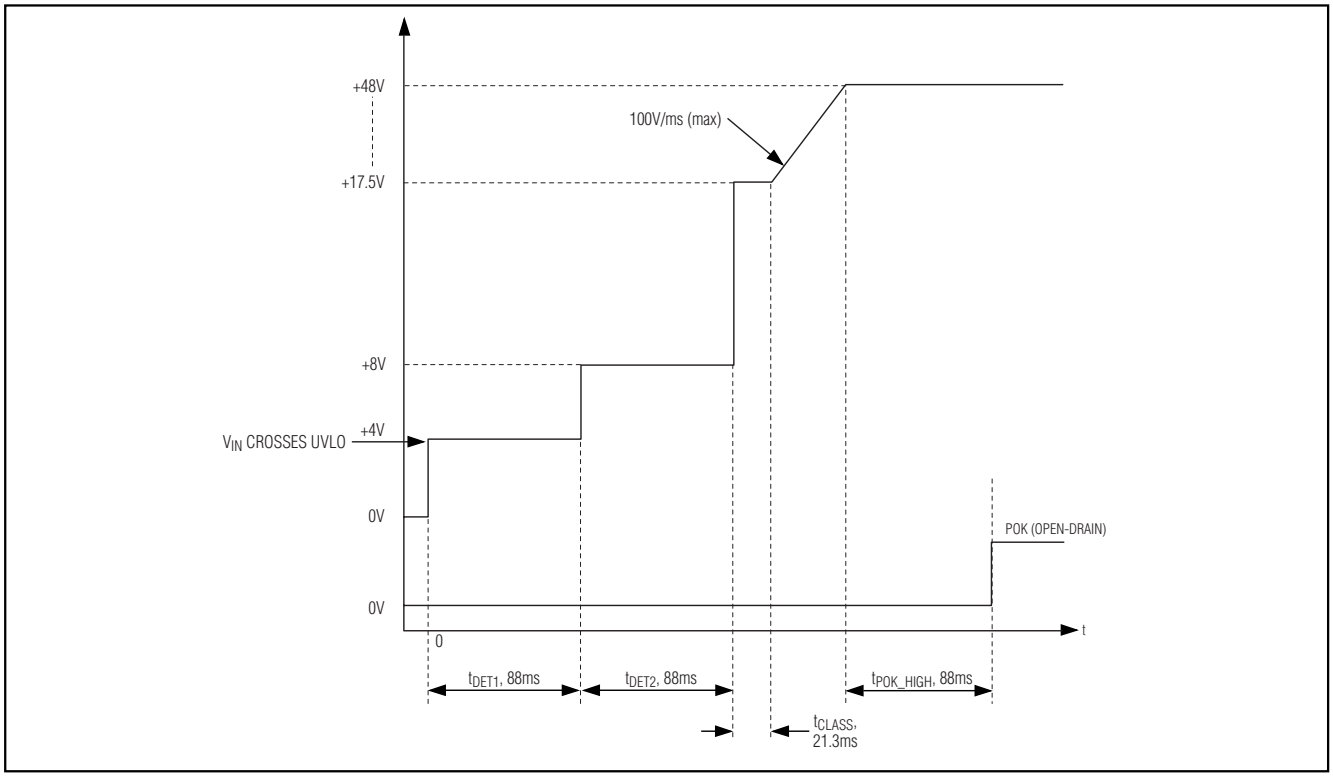

Figure 6. Startup Sequence

output voltage slew rate at the OUT pin to dV_{OUT}/dt = 100V/ms (max) and the output-current slew rate out of the OUT pin to dI_{OUT}/dt = 35A/ms (max).

The MAX5922 has an integrated 0.45Ω N-channel power MOSFET. The MOSFET's drain is connected to the DRAIN pin and its source is connected to the OUT pin. The MAX5922 monitors and provides current-limit protection to the load at all times. The current limit is programmable using an external current-sensing resistor connected from IN to DRAIN. To be compatible with the IEE802.3af standard, use a 0.5Ω ±1%, 50ppm/°C resistor. The MAX5922 features current-limit foldback and duty-cycle limit to ensure robust operation during load-fault and short-circuit conditions (see the *Overcurrent Protection* section).

When V_{OUT} is within 750mV of V_{IN} for more than t_{POK_HIGH}, POK goes open drain. Figure 6 shows a typical startup sequence.

After POK is asserted, the MAX5922 activates the zero-current detection function. This function monitors the output for an undercurrent condition and eventually turns off the power to the output if the PD is disconnected (see the *Zero-Current Detection* section).

Undervoltage Lockout (UVLO)

The MAX5922 operates from a +32V to +60V supply voltage range and has a default UVLO set at +38V (MAX5922A) or +28V (MAX5922B/MAX5922C). The UVLO threshold is adjustable using a resistive-divider connected to the UVLO pin (see Figure 7). When the input voltage is below the UVLO threshold, all operation stops and the MOSFET is held off. When the input voltage is above the UVLO threshold and EN is high, the MAX5922 goes into operation. See Figures 2 and 4 for the operational flow charts.

To adjust the UVLO threshold, connect an external resistive-divider from IN to UVLO and then from UVLO to AGND. Use the following equation to calculate the new UVLO threshold:

$$V_{UVLO\_TH} = V_{REF}\left(1 + \frac{R1}{R2}\right)$$

V_{REF} is typically 1.38V (MAX5922A) or 1.33V (MAX5922B/MAX5922C). The UVLO pin input resistance is 50kΩ (min), keep the R1 and R2 parallel combination value at least 20 times smaller than 50kΩ to minimize the new UVLO threshold error.

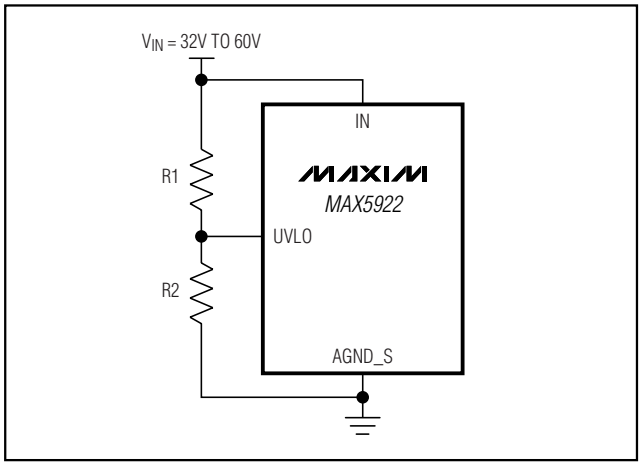

Figure 7. Setting Undervoltage Lockout with an External Resistive-Divider

Digital Logic

V_{DIG} is the input supply for the internal logic circuitry. The logic input thresholds of EN, LATCH, CLASS, DCA (MAX5922A), DET_DIS (MAX5922B/MAX5922C), and ZC_EN are CMOS compatible and are determined by the voltage at V_{DIG} which can range from 1.65V to 5.5V. The POK, $\overline{ZC}$, CL0, CL1, CL2, and $\overline{FAULT}$ outputs are open drain. V_{DIG} and all logic inputs and outputs are referenced to DGND. DGND is not connected to AGND internally and must be connected externally at a single point in the system to AGND. The maximum allowable difference in the voltage between DGND and AGND is ±4V.

Enable (EN)

EN is a logic input to enable the MAX5922. Bringing EN low halts all operations and turns off the internal power MOSFET. When EN is high and the input voltage is above the UVLO threshold, the MAX5922 begins operating. Enable is also used to unlatch the part after a latched fault condition. This is done by toggling EN low and high again after a fault condition.

Overcurrent Protection

The MAX5922 provides a sophisticated overcurrent protection circuitry to ensure the device's robustness under output-current transient and current fault conditions. The current protection circuitry employs a constant current limit, a current foldback, and an overcurrent timeout. The device monitors the voltage drop, V_{SENSE} ($V_{SENSE} = V_{IN} - V_{DRAIN}$) to determine the load current.

Constant Current Limit

The MAX5922 monitors V_{SENSE} at all times during power mode and regulates the current through the power MOSFET as necessary to keep V_{SENSE} (max) to the current-limit sense voltage (V_{ILIM} = 212mV). The load-current limit, I_{LIM}, is programmed by the current-sense resistor, R_{SENSE}, connected from IN to DRAIN ($I_{LIM} = V_{ILIM}/R_{SENSE}$). When the load current is less than I_{LIM}, the MOSFET is fully on. When the load is trying to draw more than I_{LIM}, the OUT pin works like a constant current source, limiting the output current to I_{LIM}. If I_{OUT} is at I_{LIM} for greater than the current-limit timeout, a current-limit fault is generated and the power MOSFET is turned off (see the *Overcurrent Timeout* and *Fault Management* sections).

Current Foldback

While in current-limit condition, the voltage at the OUT pin drops. As the load resistance reduces (more loading), the output voltage reduces accordingly to maintain a constant load current. The power dissipation in the power MOSFET is ($V_{DRAIN} - V_{OUT}$) × I_{LIM}. As the output voltage drops lower, more power is dissipated across the power MOSFET. To reduce this power dissipation, the MAX5922 offers a current foldback feature where it linearly reduces the V_{ILIM} value when V_{OUT} drops below the OUT current-limit foldback voltage (V_{FBSTOP} = 18V). Figure 8 illustrates this current foldback limit behavior.

Overcurrent Timeout

The MAX5922 keeps track of the time it is in current limit. An internal digital counter begins incrementing its count at 1count/ms when V_{SENSE} exceeds its limit (either V_{ILIM} or V_{ILIM} foldback in foldback mode). The counter is reset to zero if the current falls back below the current limit. When the cumulative count reaches 60, an overcurrent fault is generated. After an overcurrent fault condition, the switch is turned off and the $\overline{FAULT}$ signal goes low (see Figure 9).

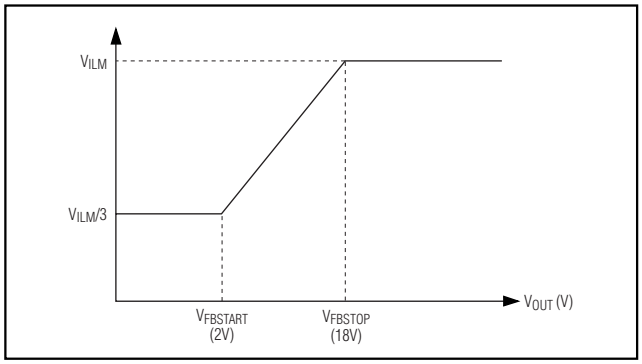

Figure 8. Current Foldback Characteristic

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This overcurrent timeout enables the MAX5922 to operate in a periodic overcurrent condition without causing a fault (see Figure 9).

Power-OK (POK)

POK goes open-drain t_{POK_HIGH} (88ms) after V_{OUT} rises to within V_{THPOK} (0.75V) from V_{IN}. POK goes low t_{POK_LOW} (1.4ms) after V_{OUT} drops 0.82V below V_{IN}.

Zero-Current Detection

Zero-current detection is enabled if ZC_EN is high and only after the startup period has finished (indicated by POK going high). When V_{SENSE} falls below the zero-current threshold (V_{ZCTH}) for a continuous t_{ZCDEL} = 350ms, a zero-current fault is generated. The MOSFET is turned off and $\overline{ZC}$ is latched low. The MAX5922A and the MAX5922B/MAX5922C (with DET_DIS = low) immediately begin a PD detection sequence, regardless of the status of the LATCH input. $\overline{ZC}$ is unlatched and goes high impedance after a PD is detected. $\overline{ZC}$ is also high impedance during initial power-up. When DET_DIS is high (MAX5922B/MAX5922C), a zero-current fault shuts down the MOSFET and the EN pin needs to be toggled to unlatch the fault.

At any time during a zero-current condition, if V_{SENSE} goes above V_{ZCTH} for the zero-current deglitch time (t_{ZC_DEG} = 10ms), the zero-current counter resets to zero and a zero-current fault is not generated. Bring ZC_EN low to disable the zero-current detection function. $\overline{ZC}$ stays high impedance in this mode.

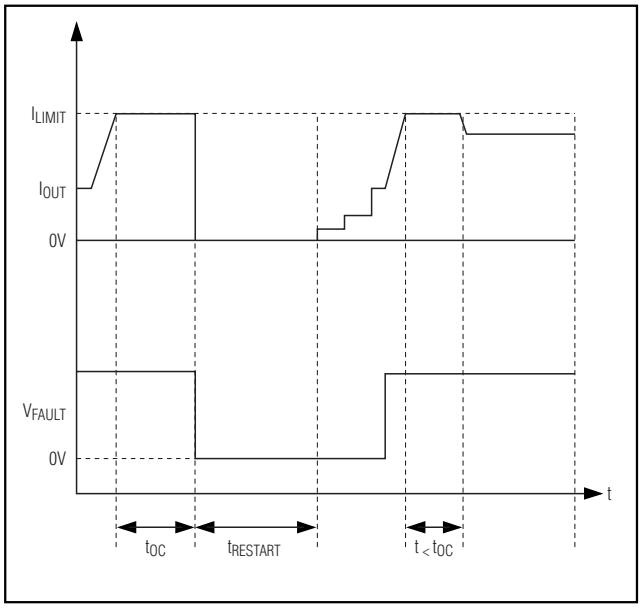

Figure 9. Overcurrent Response

Thermal Shutdown

If the MAX5922 die temperature reaches +150°C, an overtemperature fault is generated. The MOSFET turns off and $\overline{FAULT}$ goes low. The MAX5922 die temperature must cool down below 120°C before the overtemperature fault condition is removed (see *Fault Management* section).

Fault Report ($\overline{FAULT}$)

$\overline{FAULT}$ goes low when there is an overcurrent fault and/or an overtemperature fault. $\overline{FAULT}$ is open-drain otherwise. After a fault, the $\overline{FAULT}$ signal is latched low. $\overline{FAULT}$ is unlatched at the beginning of the next power mode.

Fault Management

The MAX5922 offers either latched-off or auto-retry fault management configurable by the LATCH input. Bringing LATCH high puts the device into latch mode while pulling LATCH low selects the autoretry option.

In latch mode, the MAX5922 turns the MOSFET off and keeps it off after an overcurrent fault or an over-temperature fault. After the fault condition goes away, recycle the power supplies or toggle the EN pin low and high again to unlatch the part. However, the part waits a $t_{RESTART}$ period (1.92s) before recovering from a fault condition and resuming normal operation.

In autoretry mode, the MAX5922 turns the MOSFET off after an overcurrent or overtemperature fault. After the fault condition is removed, the device waits a $t_{RESTART}$ period (1.92s) and then automatically restarts and enters the PD detection mode (MAX5922A and MAX5922B/MAX5922C with DET_DIS low). If DET_DIS is high (MAX5922B/MAX5922C), the MAX5922B/MAX5922C automatically restart into the power-up mode after $t_{RESTDRT}$. If the fault was due to an overtemperature condition, the MAX5922 waits for its die temperature to cool down below the hysteresis level before starting the $t_{RESTART}$ time.

Detection Collision Avoidance

Detection collision avoidance is enabled by connecting the DCA pin directly to V_{DIG} and disabled by connecting it to DGND. When DCA is high, the MAX5922A activates a back-off time, t_{DCA} (2.8s), after every failed detection during PD detection mode. During this back-off time, the MAX5922A turns off the MOSFET and drives the OUT pin to high impedance. This function is required by the IEEE 802.3af standard if the PSE resides in a midspan system. After t_{DCA}, the MAX5922A starts a PD detection sequence. The MAX5922B has this function internally disabled and the MAX5922C has this function internally enabled.

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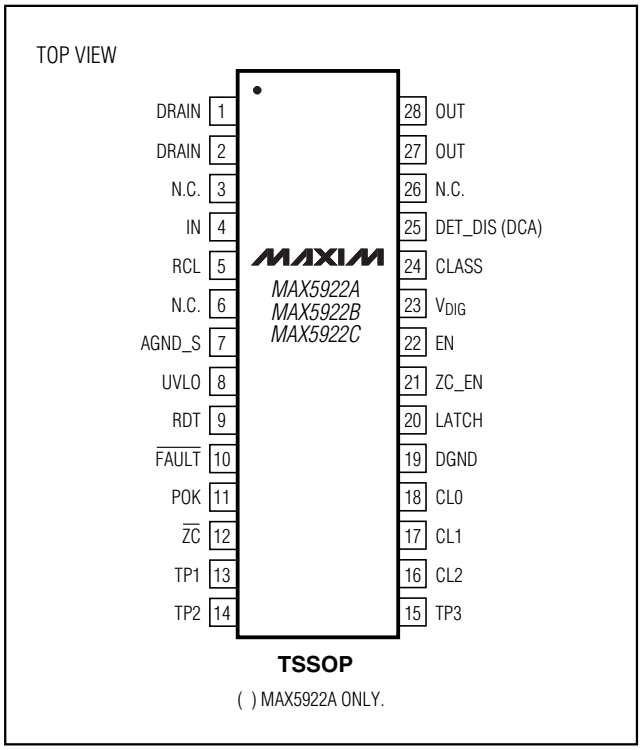
Selector Guide

PART	PIN-PACKAGE	DETECTION COLLISION AVOIDANCE	PD DETECTION DISABLE
MAX5922AEUI	28 TSSOP	Selectable	—
MAX5922BEUI	28 TSSOP	Disabled	Selectable
MAX5922CEUI	28 TSSOP	Enabled	Selectable

Pin Configuration



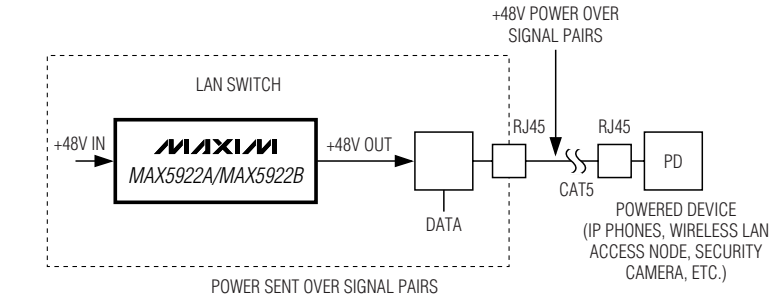
Chip Information

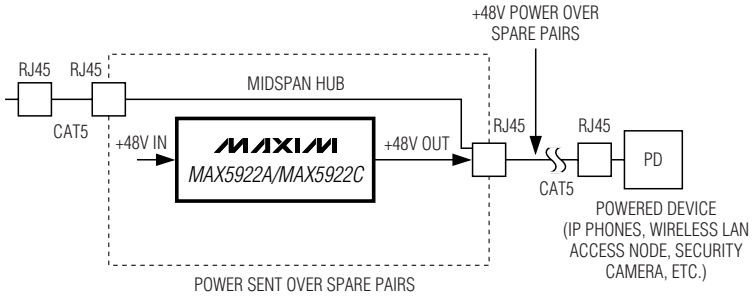
TRANSISTOR COUNT: 8687

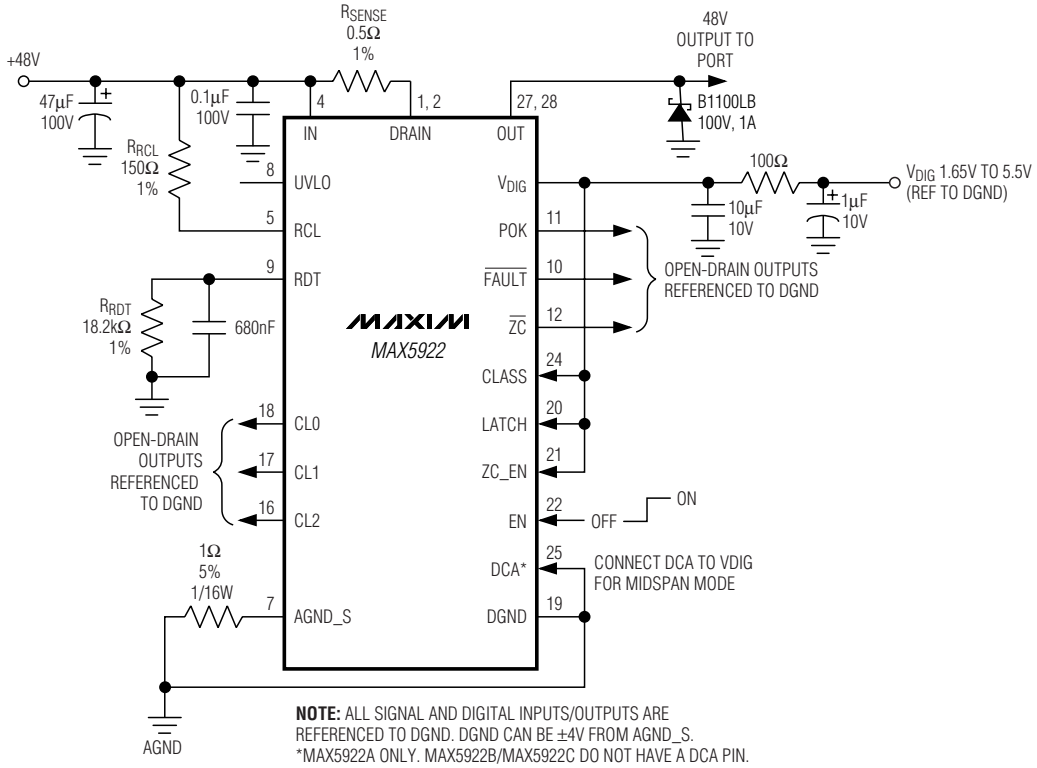
PROCESS: BiCMOS

+48V, Single-Port Network Power Switch For Power-Over-LAN

Typical Application Circuits



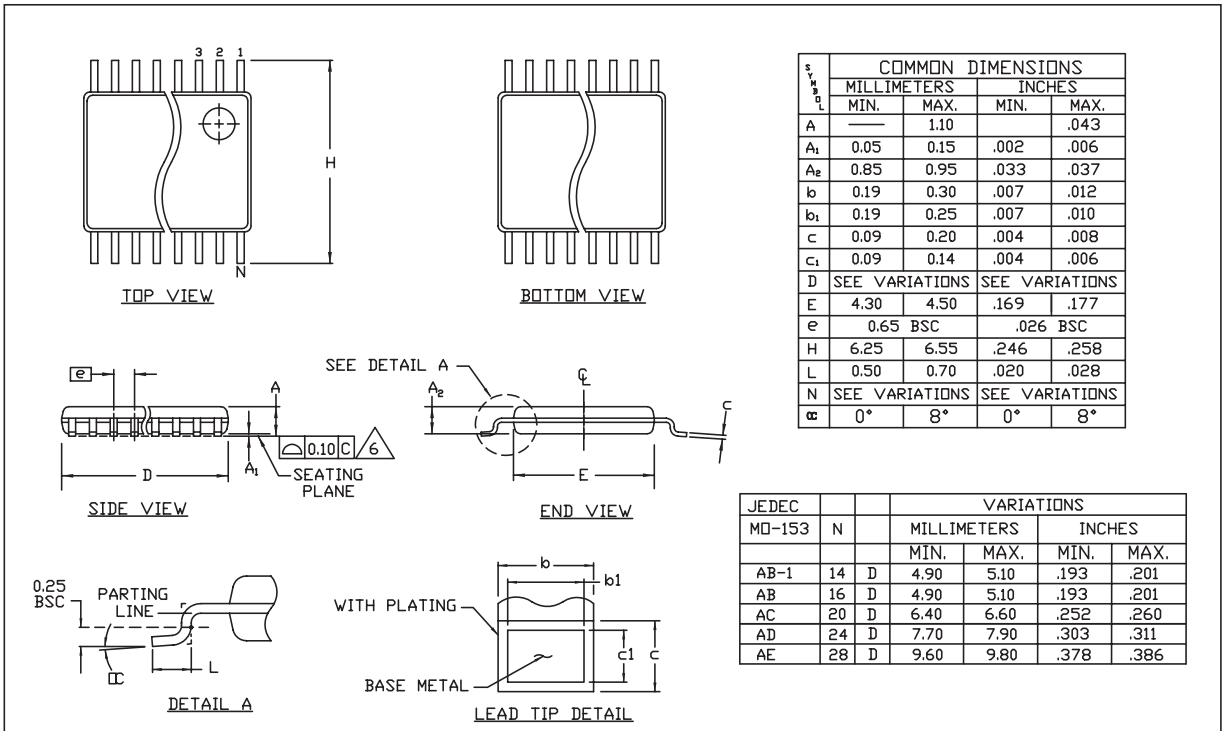




Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX5922AEUI+ MAX5922AEUI+T MAX5922BEUI+ MAX5922BEUI+T MAX5922CEUI+ MAX5922CEUI+T