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REVISION HISTORY

5/15—Rev. 0 to Rev. A

Updated Outline Dimensions ... 22
Changes to Ordering Guide ... 22

4/07—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = V_{TTI} = V_{TTO} = 3.3 V, V_{EE} = 0 V, R_L = 50 Ω, two outputs active with no pre-emphasis, data rate = 3.2 Gbps, ac-coupled, PRBS7 test pattern, V_{ID} = 800 mV p-p, T_A = 25°C, unless otherwise noted.[1]

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Data Rate/Channel (NRZ)		DC		3.2	Gbps
Deterministic Jitter	Data rate = 3.2 Gbps, high EQ		16		ps p-p
Random Jitter	RMS, high EQ		500		fs
Propagation Delay	Input to output		640		ps
Lane-to-Lane Skew			55		ps
Switching Time			5		ns
Output Rise/Fall Time	20% to 80%		85		ps
INPUT CHARACTERISTICS					
Input Voltage Swing	Differential	200		2000	mV p-p
Input Voltage Range	Common mode, V_{ID} = 800 mV p-p	V_{EE} + 1.0		V_{CC} + 0.3	V
Input Capacitance			2		pF
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Differential, @ dc	700	800	900	mV p-p
Output Voltage Range	Single-ended absolute voltage level	V_{cc} − 1.6		V_{cc} + 0.6	V
Output Current	No pre-emphasis		16		mA
Output Current	Maximum pre-emphasis, all ports		28		mA
Output Capacitance			2		pF
TERMINATION CHARACTERISTICS					
Resistance	Differential		100		Ω
Temperature Coefficient			0.1		Ω/°C
POWER SUPPLY					
Operating Range					
V_{CC}	V_{EE} = 0 V	3.0	3.3	3.6	V
V_{TTI}	V_{EE} = 0 V		V_{CC}		V
V_{TTO}	V_{EE} = 0 V		V_{CC}		V
Supply Current	Two outputs active, no pre-emphasis, 400 mV I/O swings (800 mV p-p differential)				
I_{CC}		27	31	35	mA
$I_{I/O}$ = I_{TTO} + I_{TTI}		26	32	39	mA
Supply Current	Three outputs active, maximum pre-emphasis, 400 mV I/O swings (800 mV p-p differential)				
I_{CC}		53	58	63	mA
$I_{I/O}$ = I_{TTO} + I_{TTI}		74	84	95	mA
THERMAL CHARACTERISTICS					
Operating Temperature Range		−40		+85	°C
θ_{JA}	Still air		30.0		°C/W
LOGIC INPUT CHARACTERISTICS					
Input High (V_{IH})		2.4		V_{CC}	V
Input Low (V_{IL})		V_{EE}		0.8	V

[1] V_{ID}: Input differential voltage swing.

I²C TIMING SPECIFICATIONS

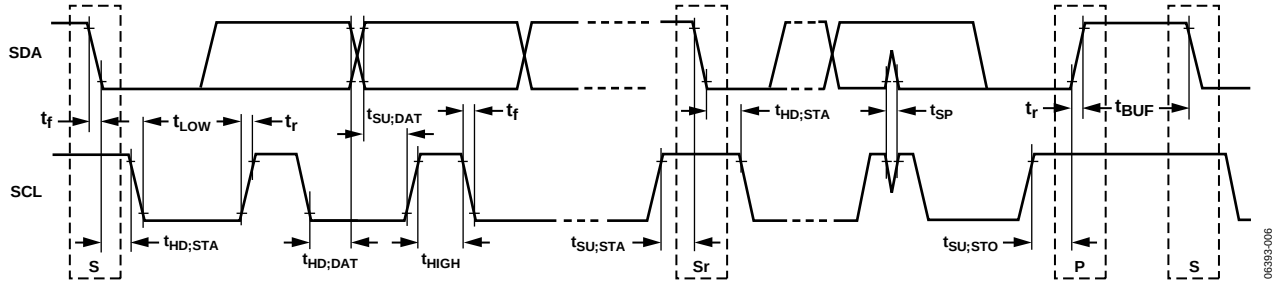


Figure 2. I²C Timing Diagram

Table 2.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{SCL}	0	400+	kHz
Hold Time for a Start Condition	$t_{HD;STA}$	0.6	–	µs
Set-up Time for a Repeated Start Condition	$t_{SU;STA}$	0.6	–	µs
Low Period of the SCL Clock	t_{LOW}	1.3	–	µs
High Period of the SCL Clock	t_{HIGH}	0.6	–	µs
Data Hold Time	$t_{HD;DAT}$	0	–	µs
Data Set-Up Time	$t_{SU;DAT}$	10	–	ns
Rise Time for Both SDA and SCL	t_r	1	300	ns
Fall Time for Both SDA and SCL	t_f	1	300	ns
Set-Up Time for Stop Condition	$t_{SU;STO}$	0.6	–	µs
Bus Free Time Between a Stop Condition and a Start Condition	t_{BUF}	1	–	ns
Capacitance for Each I/O Pin	C_i	5	7	pF

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{CC} to V_{EE}	3.7 V
V_{TTI}	V_{CC} + 0.6 V
V_{TTO}	V_{CC} + 0.6 V
Internal Power Dissipation	4.1 W
Differential Input Voltage	2.0 V
Logic Input Voltage	V_{EE} − 0.3V < V_{IN} < V_{CC} + 0.6 V
Storage Temperature Range	−65°C to +125°C
Lead Temperature	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

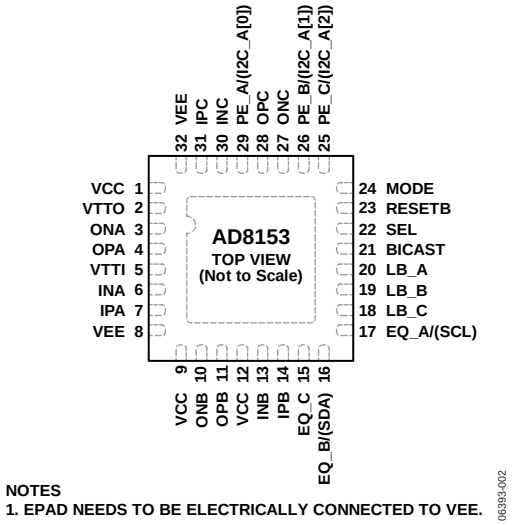


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 9, 12	VCC	Power	Positive Supply.
2	VTTO	Power	Output Termination Supply.
3	ONA	I/O	High Speed Output Complement.
4	OPA	I/O	High Speed Output.
5	VTTI	Power	Input Termination Supply.
6	INA	I/O	High Speed Input Complement.
7	IPA	I/O	High Speed Input.
8, 32, EPAD	VEE	Power	Negative Supply.
10	ONB	I/O	High Speed Output Complement.
11	OPB	I/O	High Speed Output.
13	INB	I/O	High Speed Input Complement.
14	IPB	I/O	High Speed Input.
15	EQ_C	Control	Port C Input Equalization Control.
16	EQ_B/(SDA)	Control	Port B Input Equalization Control/(I^2C Data when MODE = 1).
17	EQ_A/(SCL)	Control	Port A Input Equalization Control/(I^2C Clock when MODE = 1).
18	LB_C	Control	Port C Loopback Enable.
19	LB_B	Control	Port B Loopback Enable.
20	LB_A	Control	Port A Loopback Enable.
21	BICAST	Control	Bicast Enable.
22	SEL	Control	A/B Select.
23	RESETB	Control	Configuration Registers Reset.
24	MODE	Control	Configuration Mode. 1 for Serial/Mixed Mode, 0 for Pin Mode.
25	PE_C/(I2C_A[2])	Control	Port C Pre-Emphasis Control/(I^2C Slave Address Bit 2 when MODE = 1).
26	PE_B/(I2C_A[1])	Control	Port B Pre-Emphasis Control/(I^2C Slave Address Bit 1 when MODE = 1).
27	ONC	I/O	High Speed Output Complement.
28	OPC	I/O	High Speed Output.
29	PE_A/(I2C_A[0])	Control	Port A Pre-Emphasis Control/(I^2C Slave Address Bit 0 when MODE = 1).
30	INC	I/O	High Speed Input Complement.
31	IPC	I/O	High Speed Output.
	EPAD		Exposed Pad. The EPAD needs to be electrically connected to VEE.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = V_{TTI} = V_{TTO} =3.3 V, V_{EE} = 0 V, R_L = 50 Ω, two outputs active with no pre-emphasis, high EQ, data rate = 3.2 Gbps, ac-coupled, PRBS7 test pattern, V_{ID} = 800 mV p-p, T_A = 25°C, unless otherwise noted.

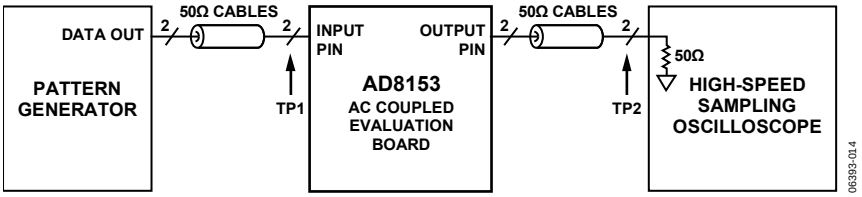


Figure 4. Standard Test Circuit (No Channel)

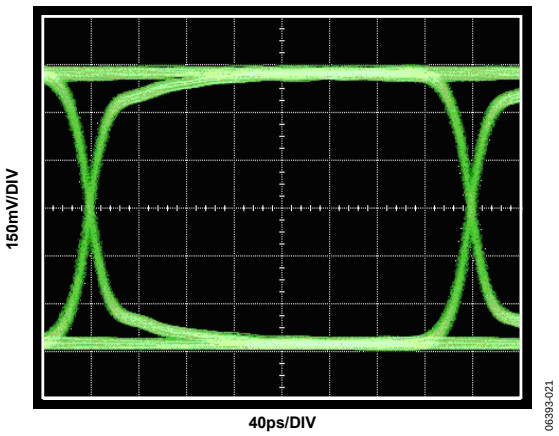


Figure 5. 3.2 Gbps Input Eye (TP1 from Figure 4)

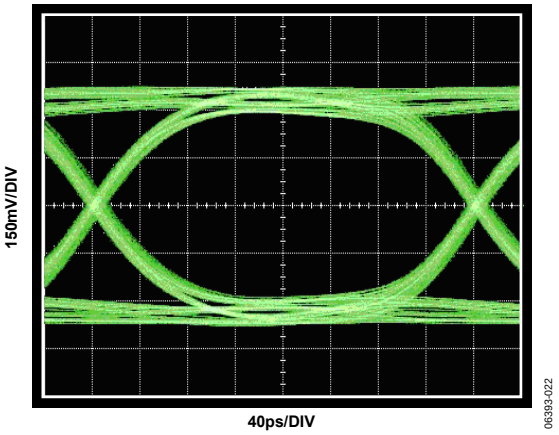


Figure 6. 3.2 Gbps Output Eye, No Channel (TP2 from Figure 4)

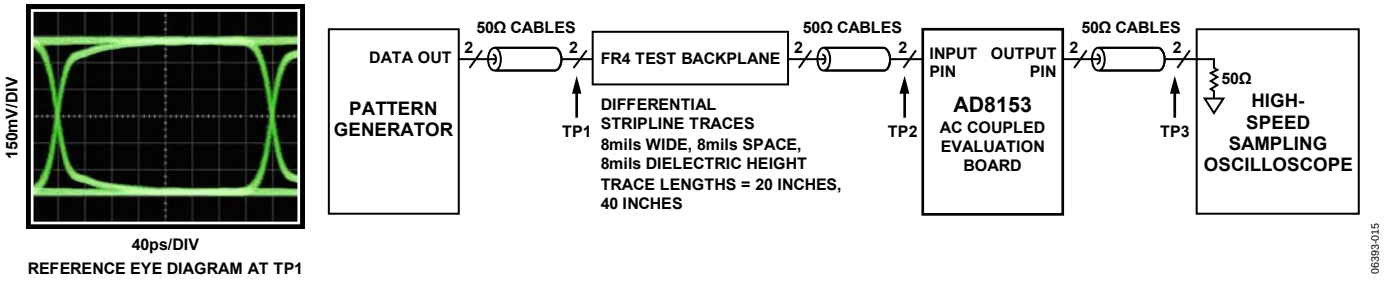


Figure 7. Input Equalization Test Circuit

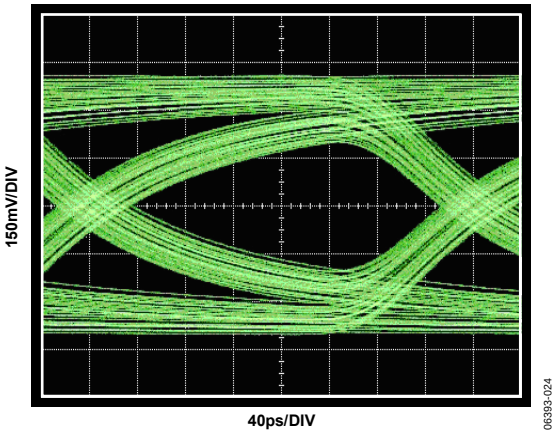


Figure 8. 3.2 Gbps Input Eye, 20 Inch FR4 Input Channel (TP2 from Figure 7)

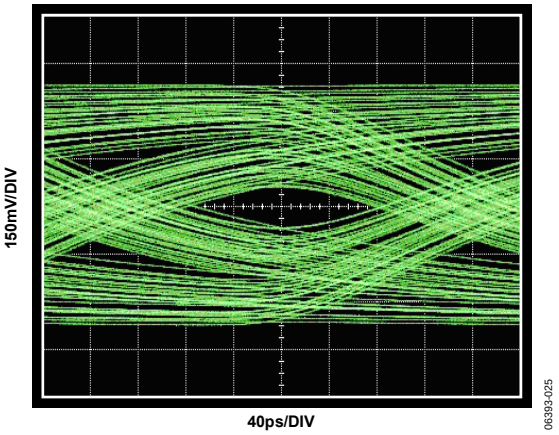


Figure 9. 3.2 Gbps Input Eye, 40 Inch FR4 Input Channel (TP2 from Figure 7)

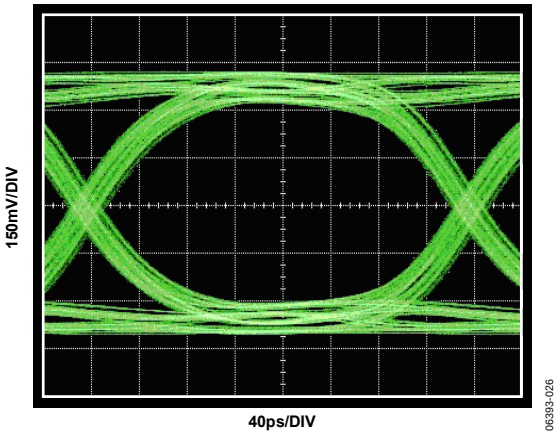


Figure 10. 3.2 Gbps Output Eye, 20 Inch FR4 Input Channel, High EQ (TP3 from Figure 7)

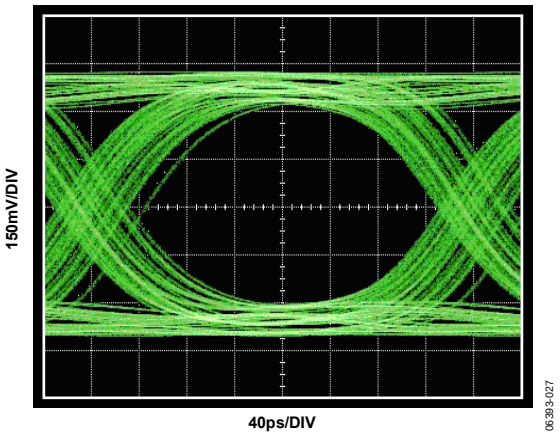


Figure 11. 3.2 Gbps Output Eye, 40 Inch FR4 Input Channel, High EQ (TP3 from Figure 7)

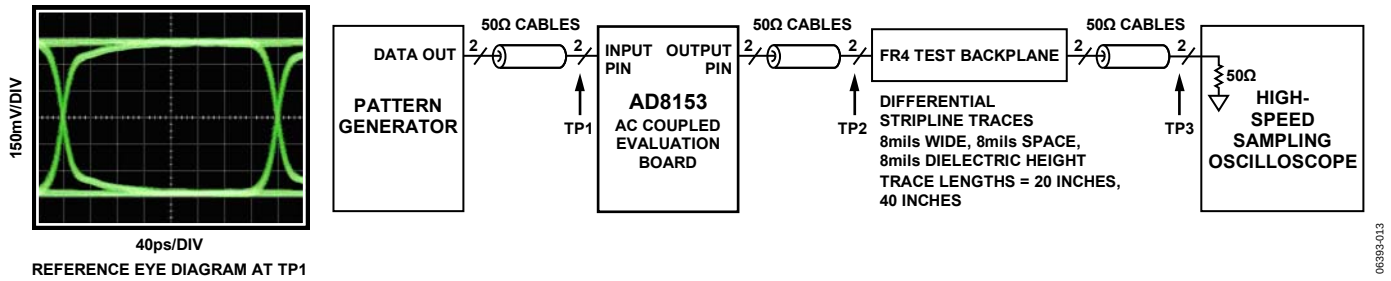


Figure 12. Output Pre-Emphasis Test Circuit

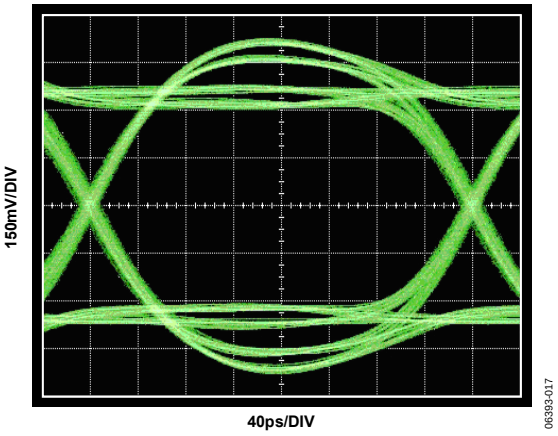


Figure 13. 3.2 Gbps Output Eye, Pre-Channel, PE = 2 (TP2 from Figure 12)

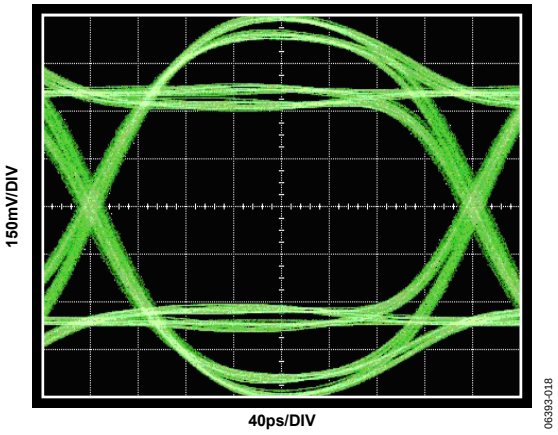


Figure 14. 3.2 Gbps Output Eye, Pre-Channel, PE = 3 (TP2 from Figure 12)

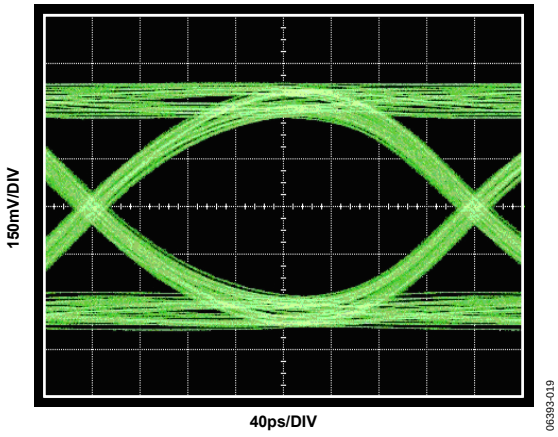


Figure 15. 3.2 Gbps Output Eye, 20 Inch FR4 Output Channel, PE = 2 (TP3 from Figure 12)

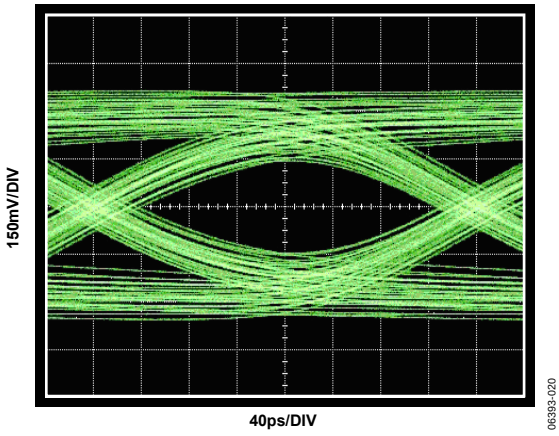


Figure 16. 3.2 Gbps Output Eye, 40 Inch FR4 Output Channel, PE = 3 (TP3 from Figure 12)

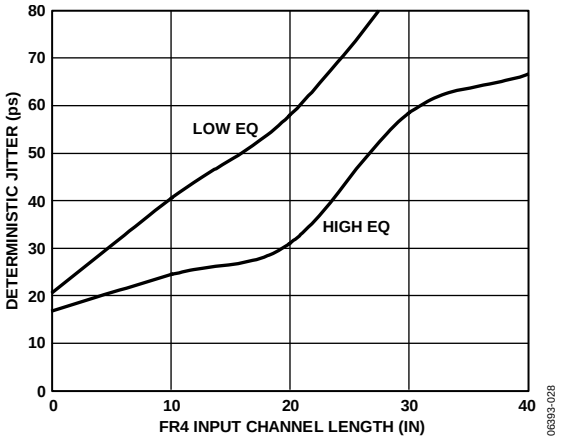


Figure 17. Deterministic Jitter vs. FR4 Input Channel Length

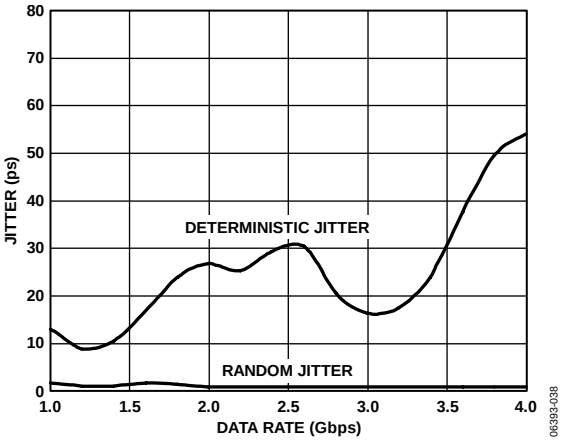


Figure 18. Jitter vs. Data Rate

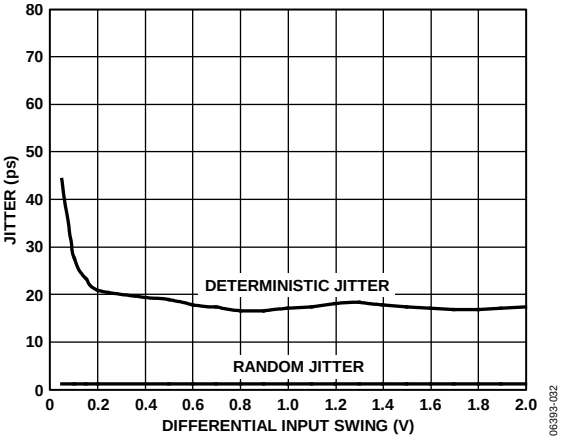


Figure 19. Jitter vs. Differential Input Swing

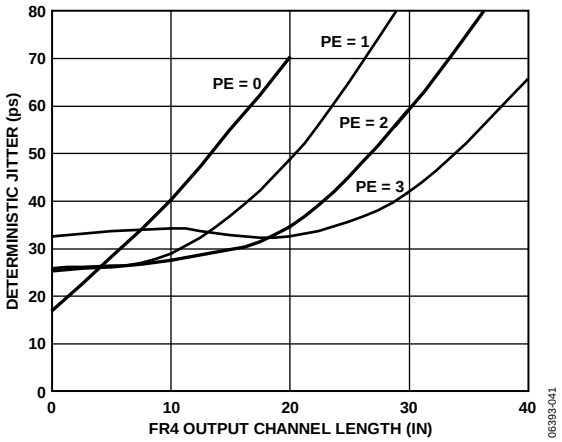


Figure 20. Deterministic Jitter vs. FR4 Output Channel Length

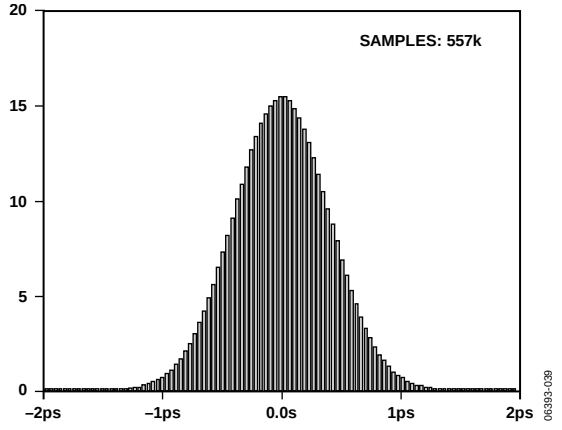


Figure 21. Random Jitter Histogram, 3.2 Gbps

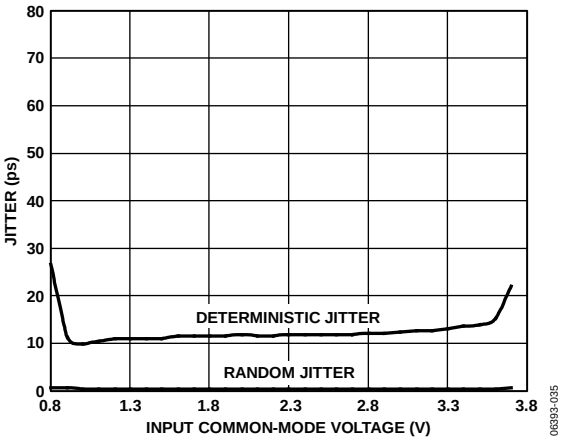


Figure 22. Jitter vs. Input Common-Mode Voltage

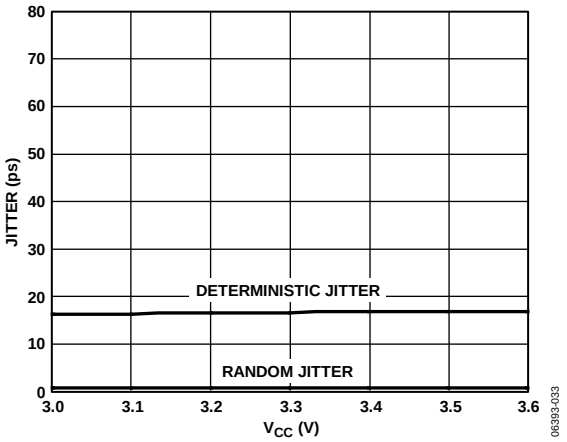


Figure 23. Jitter vs. Core Supply Voltage

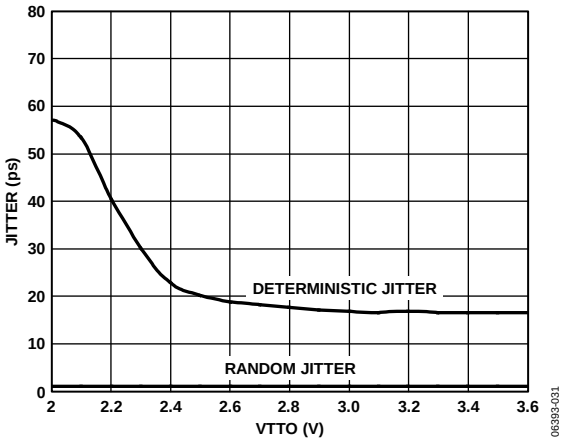


Figure 26. Jitter vs. Output Termination Voltage

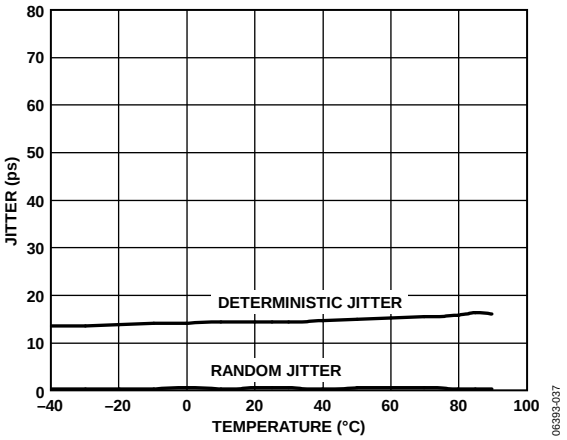


Figure 24. Jitter vs. Temperature

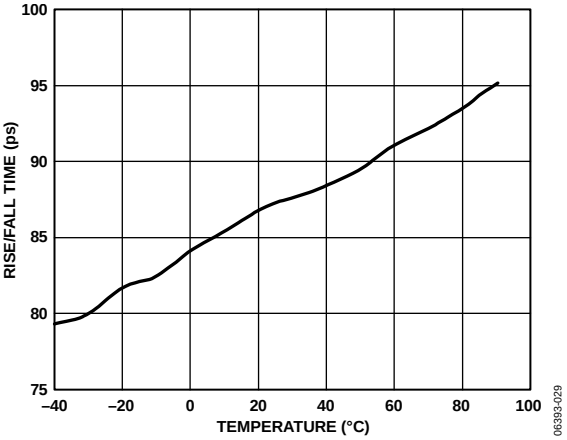


Figure 27. Rise/Fall Time vs. Temperature

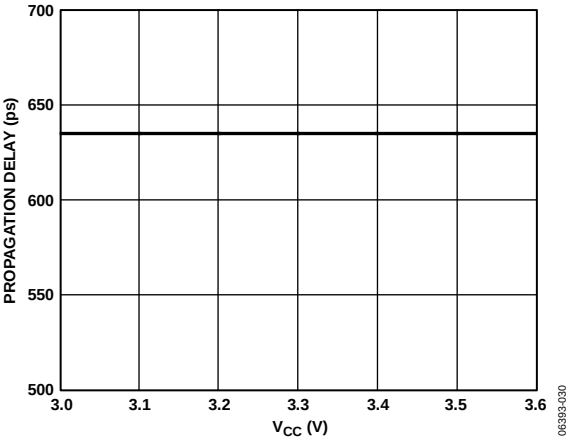


Figure 25. Propagation Delay vs. Core Supply Voltage

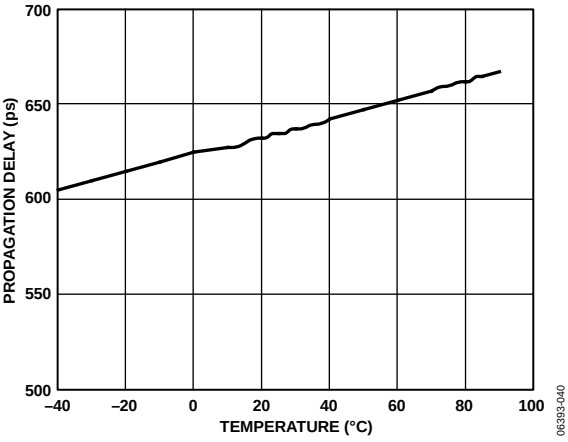


Figure 28. Propagation Delay vs. Temperature

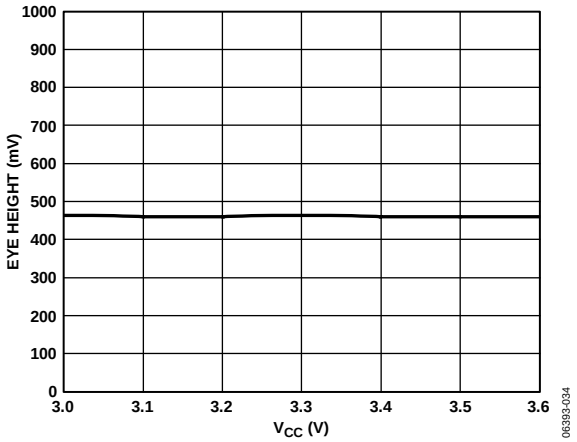


Figure 29. Eye Height vs. Core Supply Voltage

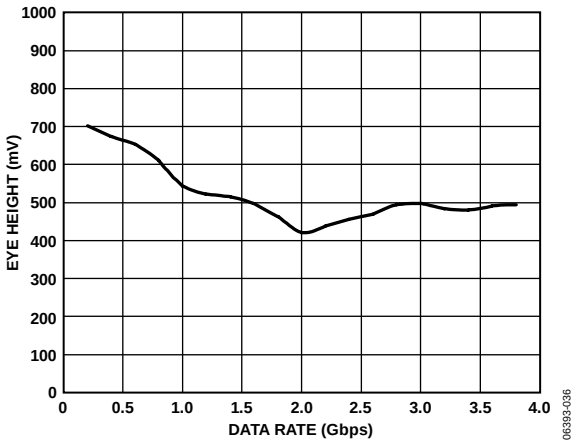


Figure 30. Eye Height vs. Data Rate

THEORY OF OPERATION

The AD8153 consists of a 2:1 multiplexer and a 1:2 demultiplexer. There are three operating modes: pin mode, serial mode, and mixed mode. In pin mode, lane switching, equalization, and pre-emphasis are controlled using external pins. In serial mode, an I^2C interface is used to control the device and to provide access to advanced features, such as additional pre-emphasis settings and output disable. In mixed mode, the user accesses the advanced features using I^2C but controls lane switching using external pins.

SWITCH CONFIGURATIONS

On the demultiplexer side, the AD8153 relays received data on Input Port C to Output Port A and/or Output Port B, depending on the state of the BICAST and SEL bits. On the multiplexer side, the device relays received data on either Input Port A or Input Port B to Output Port C, depending on the state of the SEL bit.

When bicast mode is off, the outputs of either Port A or Port B are in an idle state. In the idle state, the output tail current is set to 0, and the P and N sides of the lane are pulled up to the output termination voltage through the on-chip termination resistors.

The device also supports loopback on all ports, illustrated in Figure 31. Enabling loopback on any port overrides configurations set by the BICAST and SEL control bits. Table 5 summarizes the possible switch configurations.

The AD8153 output disable feature can be used to force an output into the idle (powered-down) state. This feature is only accessible through the serial control interface.

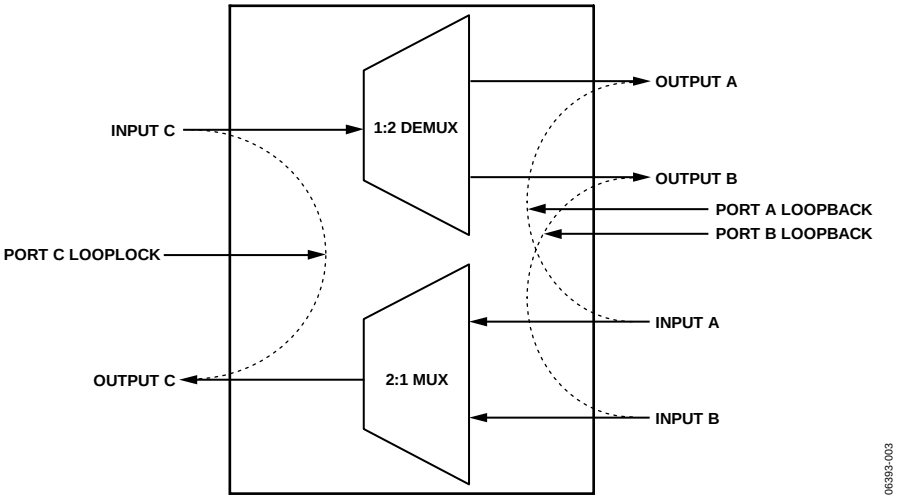


Figure 31. Loopback Configurations

Table 5. Switch Configurations

LB_A	LB_B	LB_C	SEL	BICAST	Output A	Output B	Output C
0	0	0	0	0	Input C	Idle	Input A
0	0	0	0	1	Input C	Input C	Input A
0	0	0	1	0	Idle	Input C	Input B
0	0	0	1	1	Input C	Input C	Input B
0	0	1	0	0	Input C	Idle	Input C
0	0	1	X	1	Input C	Input C	Input C
0	0	1	1	0	Idle	Input C	Input C
0	1	0	0	X	Input C	Input B	Input A
0	1	0	1	0	Idle	Input B	Input B
0	1	0	1	1	Input C	Input B	Input B
0	1	1	0	X	Input C	Input B	Input C
0	1	1	1	0	Idle	Input B	Input C
0	1	1	X	1	Input C	Input B	Input C
1	0	0	0	0	Input A	Idle	Input A
1	0	0	0	1	Input A	Input C	Input A
1	0	0	1	X	Input A	Input C	Input B
1	0	1	0	0	Input A	Idle	Input C

LB_A	LB_B	LB_C	SEL	BICAST	Output A	Output B	Output C
1	0	1	X	1	Input A	Input C	Input C
1	0	1	1	X	Input A	Input C	Input C
1	1	0	0	X	Input A	Input B	Input A
1	1	0	1	X	Input A	Input B	Input B
1	1	1	X	X	Input A	Input B	Input C

RECEIVE EQUALIZATION

In backplane applications, the AD8153 needs to compensate for signal degradation caused by long traces. The device supports two levels of input equalization, configured on a per-port basis. Table 6 summarizes the high-frequency asymptotic gain boost for each setting.

Table 6. Receive Equalization Settings

EQ_A/B/C	EQ Boost
0	6 dB
1	12 dB

TRANSMIT PRE-EMPHASIS

Transmitter pre-emphasis levels can be set by pin control or through the control registers when using the I^2C interface. Pin control allows two settings of PE. The control registers provide two additional settings.

Table 7. Pre-Emphasis Settings

Serial Mode PE_A/B/C Setting	Pin Mode PE_A/B/C	PE Boost (%)	PE Boost (dB)
0	0	0	0
1	N/A	25	1.9
2	1	50	3.5
3	N/A	75	4.9

I²C SERIAL CONTROL INTERFACE

REGISTER SET

The AD8153 can be controlled in one of three modes: pin mode, serial mode, and mixed mode. In pin mode, the AD8153 control is derived from the package pins, whereas in serial mode a set of internal registers controls the AD8153. There is also a mixed mode where switching is controlled via external pins, and equalization and pre-emphasis are controlled via the internal registers. The methods for writing data to and reading data from the AD8153 are described in the I²C Data Write section and the I²C Data Read section.

The mode is controlled via the MODE pin. To set the part in pin mode, MODE should be driven low to VEE. When MODE is driven high to VCC, the part is set to serial or mixed mode.

In pin mode, all controls are derived from the external pins. In serial mode, each channel's equalization and pre-emphasis are controlled only through the registers, as described in Table 8. Additionally, further functionality is available in serial mode as each channel's output can be enabled/disabled with the Output Enable control bits, which is not possible in pin mode. To change the switching in the AD8153 to serial mode, the mask bits (Register 0x00) must be set to 1 by writing the value 0x1F to this register, as explained in the following sections. Once all the mask bits are set to 1, switching is controlled via the LB_A, LB_B, LB_C, SEL, and BICAST bits in the register set.

In mixed mode, each channel's equalization and pre-emphasis are controlled through the registers as described above. The switching, however, can be controlled using either the external pins or the internal register set. The source of the control is selected using the mask bits (Register 0x00). If a mask bit is set to 0, the external pin acts as the source for that specific control. If a mask bit is set to 1, the associated internal register acts as the source for that specific control. As an example, if Register 0x00 were set to the value 0x0C, the SEL and LB_C controls would come from the internal register set (Bit 0 of Register 0x04 and Bit 3 of Register 0x03, respectively), and the BICAST, LB_A, and LB_B controls would come from the external pins.

GENERAL FUNCTIONALITY

The AD8153 register set is controlled through a 2-wire I²C interface. The AD8153 acts only as an I²C slave device. Therefore, the I²C bus in the system needs to include an I²C master to configure the AD8153 and other I²C devices that may be on the bus. When the MODE pin is set to a Logic 1, data transfers are controlled through the use of the two I²C wires: the input clock pin, SCL, and the bidirectional data pin, SDA.

The AD8153 I²C interface can be run in the standard (100 kHz) and fast (400 kHz) modes. The SDA line only changes value when the SCL pin is low with two exceptions. To indicate the beginning or continuation of a transfer, the SDA pin is driven low while the SCL pin is high, and to indicate the end of a transfer, the SDA line is driven high while the SCL line is high. Therefore, it is important to control the SCL clock to only toggle when the SDA line is stable unless indicating a start, repeated start, or stop condition.

Table 8. Register Map

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
00000000 (0x00)				BICAST MASK	SEL MASK	LB_C MASK	LB_B MASK	LB_A MASK	00000000 (0x00)
00000001 (0x01)				OUTPUT DISABLE A	LB_A	EQ_A	PE_A [1]	PE_A [0]	00000000 (0x00)
00000010 (0x02)				OUTPUT DISABLE B	LB_B	EQ_B	PE_B [1]	PE_B [0]	00000000 (0x00)
00000011 (0x03)				OUTPUT DISABLE C	LB_C	EQ_C	PE_C [1]	PE_C [0]	00000000 (0x00)
0000100 (0x04)							BICAST	SEL	00000000 (0x00)

I²C DATA WRITE

To write data to the AD8153 register set, a microcontroller, or any other I²C master, needs to send the appropriate control signals to the AD8153 slave device. The steps that need to be followed are listed below, where the signals are controlled by the I²C master unless otherwise specified. A diagram of the procedure is shown in Figure 32.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the AD8153 part address (seven bits) whose upper four bits are the static value b1001 and whose lower three bits are controlled by the input pins I2C_A[2:0]. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8153 to acknowledge the request.
5. Send the register address (eight bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the AD8153 to acknowledge the request.
7. Send the data (eight bits) to be written to the register whose address was set in Step 5. This transfer should be MSB first.
8. Wait for the AD8153 to acknowledge the request.
9. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.
10. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 in this procedure to perform another write.
11. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the read procedure (in the I²C Data Read section) to perform a read from another address.
12. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with step 8 of the read procedure (in the I²C Data Read section) to perform a read from the same address set in Step 5.

The AD8153 write process is shown in Figure 32. The SCL signal is shown along with a general write operation and a specific example. In the example, data 0x92 is written to Address 0x6D of an AD8153 part with a part address of 0x4B. The part address is seven bits wide and is composed of the AD8153 static upper four bits (b1001) and the pin programmable lower three bits (I2C_ADDR[2:0]). In this example, the I2C_ADDR bits are set to b011. In Figure 32, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I²C master and never by the AD8153 slave. As for the SDA line, the data in the shaded polygons is driven by the AD8153, whereas the data in the non-shaded polygons is driven by the I²C master. The end phase case shown is that of 9a.

It is important to note that the SDA line only changes when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, Step 1 and Step 9 in this case.

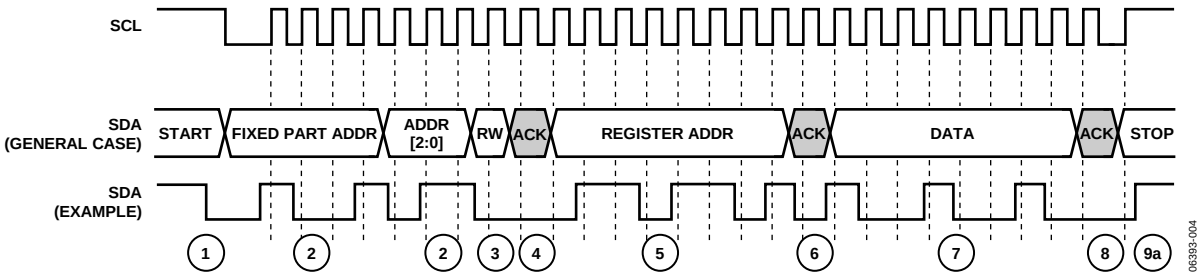


Figure 32. I²C Write Diagram

I²C DATA READ

To read data from the AD8153 register set, a microcontroller, or any other I²C master, needs to send the appropriate control signals to the AD8153 slave device. The steps to be followed are listed below, where the signals are controlled by the I²C master unless otherwise specified. A diagram of the procedure can be seen in Figure 33.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the AD8153 part address (seven bits) whose upper four bits are the static value b1001 and whose lower three bits are controlled by the input pins I2C_ADDR[2:0]. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8153 to acknowledge the request.
5. Send the register address (eight bits) from which data is to be read. This transfer should be MSB first. The register address is kept in memory in the AD8153 until the part is reset or the register address is written over with the same procedure (Step 1 to Step 6).
6. Wait for the AD8153 to acknowledge the request.
7. Send a repeated start condition (while holding the SCL line high, pull the SDA line low).
8. Send the AD8153 part address (seven bits) whose upper four bits are the static value b1001 and whose lower three bits are controlled by the input pins I2C_ADDR[1:0]. This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the AD8153 to acknowledge the request.
11. The AD8153 then serially transfers the data (eight bits) held in the register indicated by the address set in Step 5.
12. Acknowledge the data.
13. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.
14. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the write procedure (see the I²C Data Write section) to perform a write.
15. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of this procedure to perform a read from another address.
16. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

The AD8153 read process is shown in Figure 33. The SCL signal is shown along with a general read operation and a specific example. In the example, Data 0x49 is read from Address 0x6D of an AD8153 part with a part address of 0x4B. The part address is seven bits wide and is composed of the AD8153 static upper four bits (b1001) and the pin programmable lower three bits (I2C_ADDR[2:0]). In this example, the I2C_ADDR bits are set to b011. In Figure 33, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I²C master and never by the AD8153 slave. As for the SDA line, the data in the shaded polygons is driven by the AD8153, whereas the data in the nonshaded polygons is driven by the I²C master. The end phase case shown is that of 13a.

It is important to note that the SDA line only changes when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, as in Step 1, Step 7, and Step 13. In Figure 33, A is the same as ACK in Figure 32. Equally, Sr represents a repeated start where the SDA line is brought high before SCL is raised. SDA is then dropped while SCL is still high.

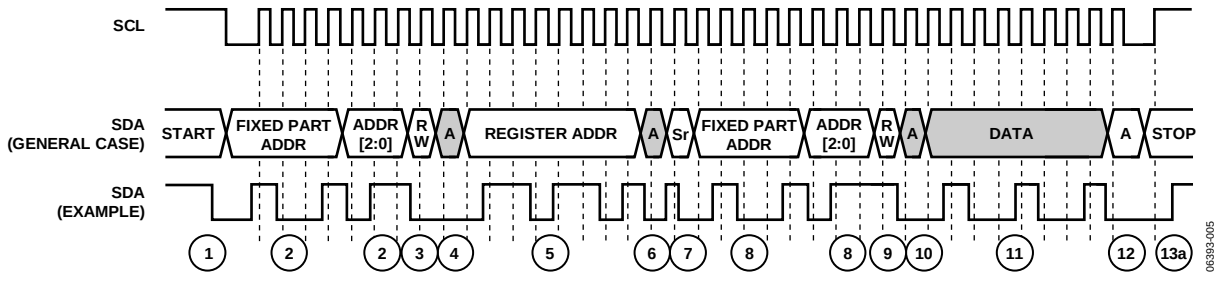


Figure 33. I²C Read Diagram

APPLICATIONS INFORMATION

The main application of the AD8153 is to support redundancy on both the backplane side and the line interface side of a serial link. Figure 34 illustrates redundancy in a typical backplane system. Each line card is connected to two switch fabrics (primary and redundant). The device can be configured to support either 1 + 1 or 1:1 redundancy.

Another application for the AD8153 is in test equipment for evaluating high speed serial links. Figure 36 illustrates a possible application of the AD8153 in a simple link tester.

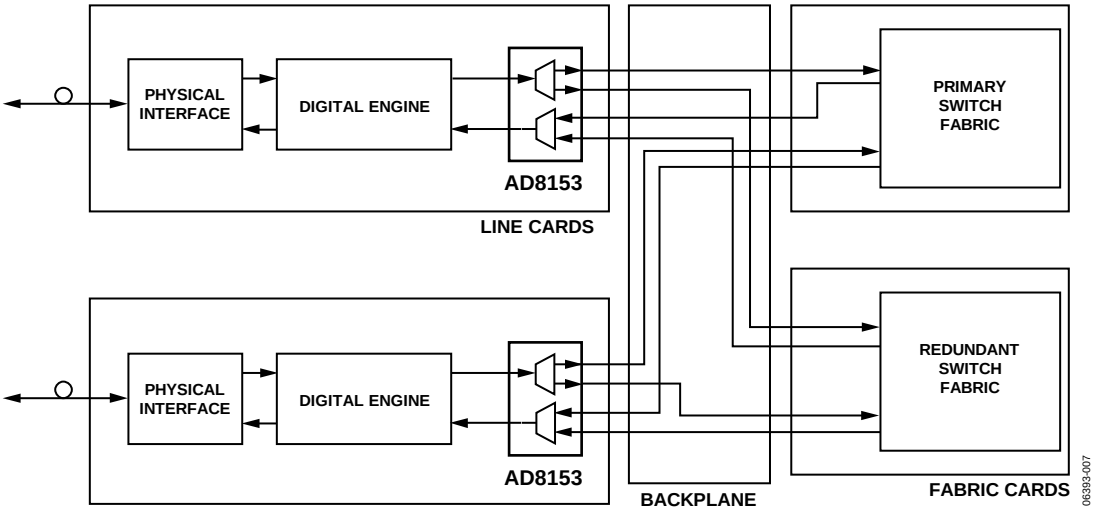


Figure 34. Switch Redundancy Application

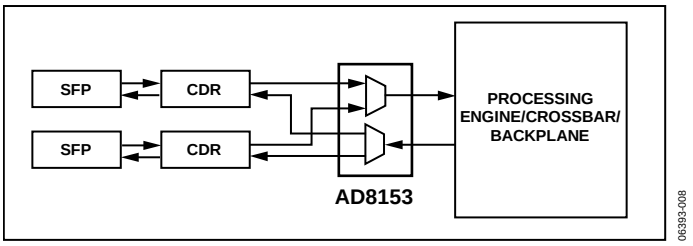


Figure 35. Line Interface Redundancy Application

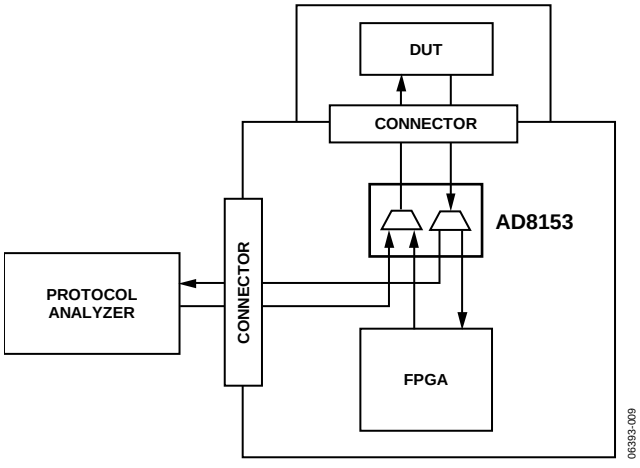


Figure 36. Test Equipment Application

PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used for optimal performance.

Power Supply Connections and Ground Planes

Use of one low impedance ground plane is recommended. The VEE pins should be soldered directly to the ground plane to reduce series inductance. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias can be used in parallel to reduce the series inductance. The exposed pad should be connected to the VEE plane using plugged vias so that solder does not leak through the vias during reflow.

Use of a 10 µF electrolytic capacitor between VCC and VEE is recommended at the location where the 3.3 V supply enters the PCB. It is recommended that 0.1 µF and 1 nF ceramic chip capacitors be placed in parallel at each supply pin for high frequency power supply decoupling. When using 0.1 µF and 1 nF ceramic chip capacitors, they should be placed between the IC power supply pins (VCC, VTTI, VTTO) and VEE, as close as possible to the supply pins.

By using adjacent power supply and GND planes, excellent high frequency decoupling can be realized by using close spacing between the planes. This capacitance is given by

$$C_{PLANE} = 0.88\varepsilon_r A/d \text{ (pF)}$$

where:

ε_r is the dielectric constant of the PCB material.
A is the area of the overlap of power and GND planes (cm^2).
d is the separation between planes (mm).

For FR4, ε_r = 4.4 and 0.25 mm spacing, C ~15 pF/cm^2.

Transmission Lines

Use of 50 Ω transmission lines is required for all high frequency input and output signals to minimize reflections. It is also necessary for the high speed pairs of differential input traces to be matched in length, as well as the high speed pairs of differential output traces, to avoid skew between the differential traces.

Soldering Guidelines for Chip Scale Package

The lands on the 32-lead LFCSP are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central exposed pad. The pad on the printed circuit board should be at least as large as this exposed pad. The user must connect the exposed pad to VEE using plugged vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

INTERFACING TO THE AD8153

TERMINATION STRUCTURES

To determine the best strategy for connecting to the high speed pins of the AD8153, the user must first be familiar with the on-chip termination structures. The AD8153 contains two types of these structures: one type for input ports and one type for output ports (see Figure 37 and Figure 38).

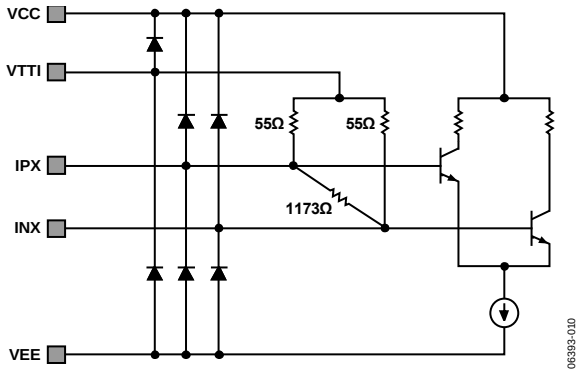


Figure 37. Receiver Simplified Diagram

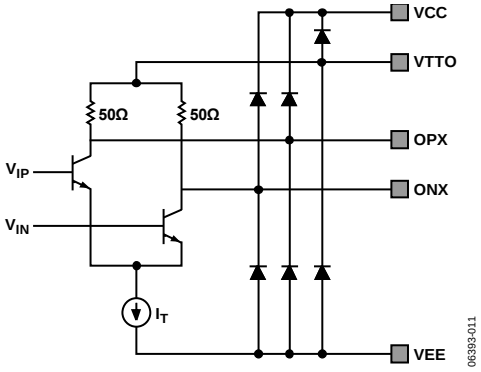


Figure 38. Transmitter Simplified Diagram

For input ports, the termination structure consists of two 55 Ω resistors connected to a termination supply and an 1173 Ω resistor connected across the differential inputs, the latter being a result of the finite differential input impedance of the equalizer.

For output ports, there are two 50 Ω resistors connected to the termination supply. Note that the differential input resistance for both structures is the same, 100 Ω.

INPUT COMPLIANCE

The range of allowable input voltages is determined by the fundamental limitations of the active input circuitry. This range of signals is normally a function of the common-mode level of the input signal, the signal swing, and the supply voltage. For a given input signal swing, there is a range of common-mode voltages that keeps the high and low voltage excursions within acceptable limits. Similarly, for a given common-mode input voltage, there is a maximum acceptable input signal swing. There is also a minimum signal swing that the active input circuitry can resolve reliably. The specifications are found in Table 1.

AC Coupling

One way to simplify the input circuit and make it compatible with a wide variety of driving devices is to use ac coupling. This has the effect of isolating the dc common-mode levels of the driver and the AD8153 input circuitry. AC coupling requires a capacitor in series with each single-ended input signal, as shown in Figure 39. This should be done in a manner that does not interfere with the high speed signal integrity of the PCB.

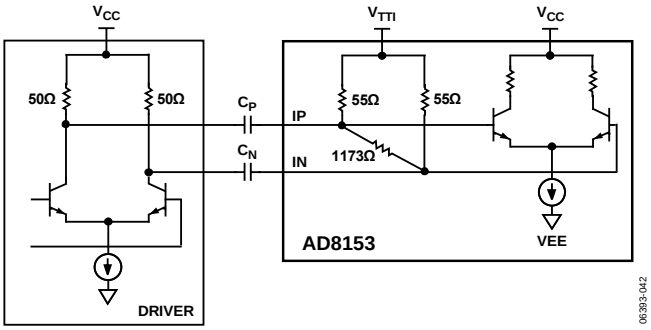


Figure 39. AC-Coupling Input Signal of AD8153

When ac coupling is used, the common-mode level at the input of the device is equal to V_{TTI}. The single-ended input signal swings above and below V_{TTI} equally. The user can then use the specifications in Table 1 to determine the input signal swing levels that satisfy the input range of the AD8153.

If dc coupling is required, determining the input common-mode level is less straightforward because the configuration of the driver must also be considered. In most cases, the user would set V_{TTI} on the AD8153 to the same level as the driver output termination voltage. This prevents a continuous dc current from flowing between the two supply nets. As a practical matter, both devices can be terminated to the same physical supply net.

Consider the following example: a driver is dc-coupled to the input of the AD8153. The AD8153 input termination voltage (V_{TTI}) and the driver output termination voltage (V_{TTOD}) are both set to the same level; that is, $V_{TTI} = V_{TTOD} = 3.3$ V. If an 800 mV differential p-p swing is desired, the total output current of the driver is 16 mA. At balance, the output current is divided evenly between the two sides of the differential signal path, 8 mA to each side. This 8 mA of current flows through the parallel combination of the 55 Ω input termination resistor on the AD8153 and the 50 Ω output termination resistor on the driver, resulting in a common-mode level of

$$V_{TTI} - 8\text{ mA} \times (50\ \Omega \parallel 55\ \Omega) = V_{TTI} - 209\text{ mV}$$

The user can then determine the allowable range of values for V_{TTI} that meets the input compliance range based on an 800 mV p-p differential swing.

OUTPUT COMPLIANCE

Figure 40 is a graphical depiction of the single-ended waveform at the output of the AD8153. The common-mode level (V_{OCM}) and the amplitude (V_{OSE}) of this waveform are a function of the output tail current (I_T), the output termination supply voltage (V_{TTO}), the topology of the far-end receiver, and whether ac- or dc-coupling is used. Keep in mind that the output tail current varies with the pre-emphasis level. The user must ensure that the high (V_H) and low (V_L) voltage excursions at the output are within the single-ended absolute voltage range limits as specified in Table 1. Failure to understand the implications of output signal levels and the choice of ac- or dc-coupling may lead to transistor saturation and poor transmitter performance.

Table 9 shows an example calculation of the output levels for the typical case, where $V_{CC} = V_{TTO} = 3.3$ V, with 50 Ω far-end terminations to a 3.3 V supply.

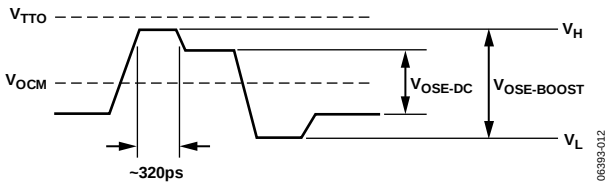


Figure 40. Single-Ended Output Waveform

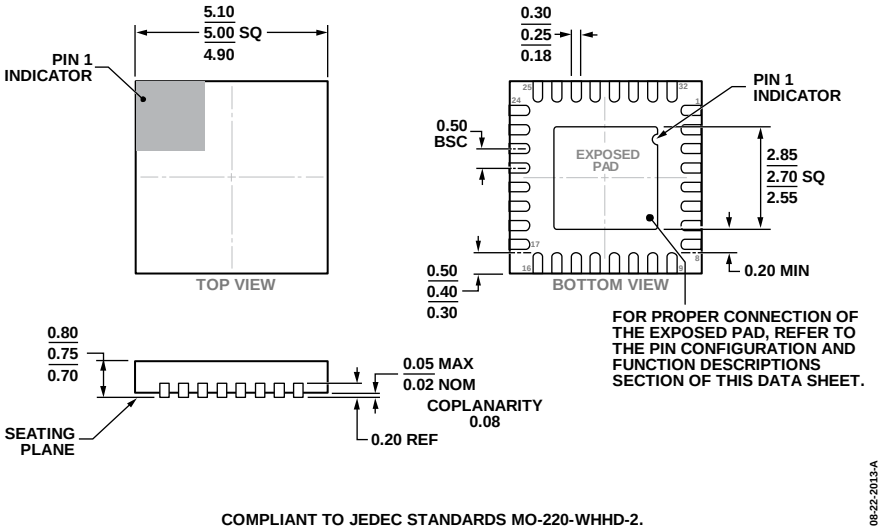
Table 9. Output Voltage Levels

				DC-Coupled			AC-Coupled		
PE Setting	**I_T (mA)**	**V_{OSE-DC} (mV p-p)**	**$V_{OSE-BOOST}$ (mV p-p)**	**V_{OCM} (V)**	**V_H (V)**	**V_L (V)**	**V_{OCM} (V)**	**V_H (V)**	**V_L (V)**
0	16	400	400	3.1	3.3	2.9	2.9	3.1	2.7
1	20	400	500	3.05	3.3	2.8	2.8	3.05	2.55
2	24	400	600	3	3.3	2.7	2.7	3	2.4
3	28	400	700	2.95	3.3	2.6	2.6	2.95	2.25

Table 10. Symbol Definitions

Symbol	Formula	Definition
V_{OSE-DC}	$I_T\|_{PE=0} \times 25\,\Omega$	Single-ended output voltage swing after settling
$V_{OSE-BOOST}$	$I_T \times 25\,\Omega$	Boosted single-ended output voltage swing
V_{OCM} (dc-coupled)	$V_{TTO} - \frac{I_T}{2} \times 25\,\Omega$	Common-mode voltage when the output is dc-coupled
V_{OCM} (ac-coupled)	$V_{TTO} - \frac{I_T}{2} \times 50\,\Omega$	Common-mode voltage when the output is ac-coupled
V_H	$V_{OCM} + V_{OSE-BOOST}/2$	High single-ended output voltage excursion
V_L	$V_{OCM} - V_{OSE-BOOST}/2$	Low single-ended output voltage excursion

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-2.

Figure 41. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-21)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8153ACPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-21
AD8153ACPZ-RL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-21
AD8153-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D06393-0-5/15(A)

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Analog Devices Inc.:

AD8153ACPZ-RL7 AD8153ACPZ