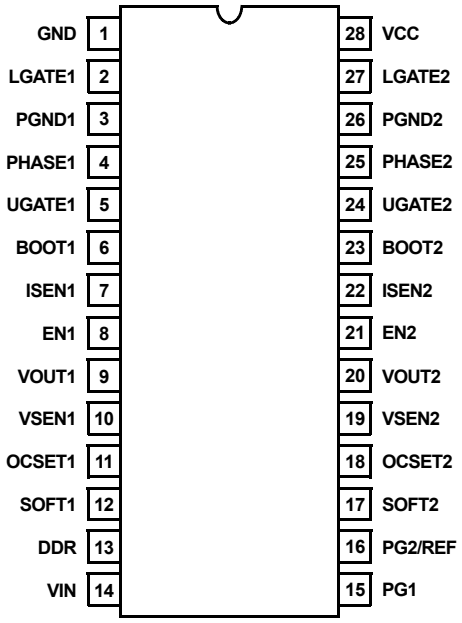
Pinout

ISL6225
SSOP-28
TOP VIEW



Absolute Maximum Ratings

Bias Voltage, V_{CC} . . . . . + 6.5V
Input Voltage, V_{IN}. . . . . +27.0V
PHASE, UGATE Voltage . . . . . GND-5V (Note 3) to 33V
BOOT, ISEN Voltage . . . . . GND-0.3V to +33.0V
BOOT with respect to PHASE . . . . . + 6.5V
All Other Pins. . . . . GND -0.3V to V_{CC} + 0.3V
ESD Classification . . . . . Class 2

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
SSOP Package	78

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SSOP - Lead Tips Only)

Recommended Operating Conditions

Bias Voltage, V_{CC} . . . . . +5.0V ±5%
Input Voltage, V_{IN} . . . . . +5.0V to +24.0V
Ambient Temperature Range. . . . . -10°C to 85°C
Junction Temperature Range. . . . . -10°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. 200ns transient.
4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY						
Bias Current	I_{CC}	LGATEx, UGATEx Open, VSENx forced above regulation point, DDR = 0, VIN > 5V	-	2.2	3.2	mA
Shut-down Current	I_{CCSN}		-	-	30	µA
V_{CC} UVLO						
Rising V_{CC} Threshold	V_{CCU}		4.3	4.65	4.75	V
Falling V_{CC} Threshold	V_{CCD}		4.1	4.35	4.45	V
V_{IN}						
Input Voltage Pin Current (Sink)	I_{VIN}		10	-	30	µA
Input Voltage Pin Current (Source)	I_{VINO}		-	-15	-30	µA
Shut-down Current	I_{VINS}		-	-	1	µA
OSCILLATOR						
PWM1 Oscillator Frequency	F_C		255	300	345	kHz
Ramp Amplitude, pk-pk	V_{R1}	V_{IN} = 16V, by design	-	2	-	V
Ramp Amplitude, pk-pk	V_{R2}	V_{IN} = 5V, by design	-	1.25	-	V
Ramp Offset	V_{ROFF}	By design	-	0.5	-	V
Ramp/V_{IN} Gain	G_{RB1}	$V_{IN} \geq 3V$, by design	-	125	-	mV/V
Ramp/V_{IN} Gain	G_{RB2}	$1 \leq V_{IN} \leq 3V$, by design	-	250	-	mV/V
REFERENCE AND SOFT-START						
Internal Reference Voltage	V_{REF}		-	0.9	-	V
Reference Voltage Accuracy			-1.0	-	+1.0	%
Soft-Start Current During Start-up	I_{SOFT}		-	-5	-	µA
Soft-Start Complete Threshold	V_{ST}	By design	-	1.5	-	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM CONVERTERS						
Load Regulation		0.0mA < I_{VOUT1} < 5.0A; 5.0V < V_{BATT} < 24.0V	-2.0	-	+2.0	%
VSEN pin bias current	I_{VSEN}	By design	50	80	120	nA
V_{OUT} pin input impedance	I_{VOUT}	V_{OUT} = 5V	40	55	65	kΩ
Undervoltage Shut-Down Level	V_{UVL}	Fraction of the set point; ~2µs noise filter	70	-	85	%
Overvoltage Shut-Down	V_{OVP1}	Fraction of the set point; ~2µs noise filter	110	-	130	%
GATE DRIVERS						
Upper Drive Pull-Up Resistance	R_{2UGPUP}	V_{CC} = 4.5V	-	8	15	Ω
Upper Drive Pull-Down Resistance	R_{2UGPDN}	V_{CC} = 4.5V	-	3.2	5	Ω
Lower Drive Pull-Up Resistance	R_{2LGPUP}	V_{CC} = 4.5V	-	8	15	Ω
Lower Drive Pull-Down Resistance	R_{2LGPDN}	V_{CC} = 4.5V	-	1.8	3	Ω
POWER GOOD AND CONTROL FUNCTIONS						
Power Good Lower Threshold	V_{PG-}	Fraction of the set point; ~3µs noise filter	-13	-	-7	%
Power Good Higher Threshold	V_{PG+}	Fraction of the set point; ~3µs noise filter. Guaranteed by design.	12	-	16	%
PGOODx Leakage Current	I_{PGLKG}	V_{PULLUP} = 5.5V	-	-	1	µA
PGOODx Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	0.5	0.85	V
EN - Low (Off)			-	-	0.8	V
EN - High (On)			2.5	-	-	V
CCM Enforced (Hysteretic Operation Inhibited)		VOUTX pulled low	-	-	0.1	V
Automatic CCM/Hysteretic Operation Enabled		VOUTX connected to the output	0.9	-	-	V
DDR - Low (Off)			-	-	0.8	V
DDR - High (On)			2.5	-	-	V
DDR REF Output Voltage	V_{DDREF}	DDR = 1, I_{REF} = 0...10mA	0.99* V_{OC2}	V_{OC2}	1.01* V_{OC2}	V
DDR REF Output Current	I_{DDREF}	DDR = 1. Guaranteed by design.	-	10	16	mA

Functional Pin Description

GND (Pin 1)

Signal ground for the IC.

LGATE1, LGATE2 (Pin 2, 27)

These are outputs of the lower MOSFET drivers.

PGND1, PGND2 (Pin 3, 26)

These pins provide the return connection for lower gate drivers. These pins are connected to sources of the lower MOSFETs of their respective converters.

PHASE1, PHASE2 (Pin 4, 25)

The PHASE1 and PHASE2 points are the junction points of the upper MOSFET sources, output filter inductors, and lower MOSFET drains. Connect these pins to the respective converter's upper MOSFET source.

UGATE1, UGATE2 (Pin 5, 24)

These pins provide the gate drive for the upper MOSFETs.

BOOT1, BOOT2 (Pin 6, 23)

These pins power the upper MOSFET drivers of the PWM converter. Connect this pin to the junction of the bootstrap capacitor with the cathode of the bootstrap diode. Anode of the bootstrap diode is connected to the VCC pin.

ISEN1, ISEN2 (Pin 7, 22)

These pins are used to monitor the voltage drop across the lower MOSFET for current feedback and overcurrent protection. For precise current detection these inputs can be connected to the optional current sense resistors placed in series with the source of the lower MOSFETs.

EN1, EN2 (Pin 8, 21)

These pins enable operation of the respective converter when high. When both pins are low, the chip is disabled and only low leakage current <1μA is taken from V_{CC} and V_{IN}. These pins are to be connected together and switched at the same time.

VOUT1, VOUT2 (Pin 9, 20)

These pins when connected to the converters' respective outputs provide the output voltage inside the chip to reduce output voltage excursion during HYS/PWM transition. When connected to ground, these pins command forced converters operate in continuous conduction mode at all load levels.

VSEN1, VSEN2 (Pin 10, 19)

These pins are connected to the resistive dividers that set the desired output voltage. The PGOOD, UVP, and OVP circuits use this signal to report output voltage status.

OCSET1 (Pin 11)

A resistor from this pin to ground sets the overcurrent threshold for the first controller.

SOFT1, SOFT2 (Pin 12, 17)

These pins provide soft-start function for their respective controllers. When the chip is enabled, the regulated 5μA pull-up current source charges the capacitor connected from the pin to ground. The output voltage of the converter follows the ramping voltage on the SOFT pin.

DDR (Pin 13)

This pin, when high, transforms dual channel chip into complete DDR memory solution. The OCSET2 pin becomes an input to provide the required tracking function. The channel synchronization is changed from out-of-phase to in-phase. The PG2/REF pin becomes the output of the VDDQ/2 buffered voltage that is used as a reference voltage by the second channel.

VIN (Pin 14)

Provides battery voltage to the oscillator for feed-forward rejection of the input voltage variation.

When connected to ground via 100kΩ resistor while the DDR pin is high, this pin commands the out-of-phase 90° channels synchronization for reduced inter-channel interference.

PG1 (Pin 15)

PGOOD1 is an open drain output used to indicate the status of the output voltage. This pin is pulled low when the first channel output is not within ±10% of the set value.

PG2/REF (Pin 16)

This pin has a double function depending on the mode the chip is operating. When the chip is used as a dual channel PWM controller (DDR = 0), the pin provides a PGOOD2 function for the second channel. The pin is pulled low when the second channel output is not within ±10% of the set value.

In DDR mode (DDR = 1), this pin serves as an output of the buffer amplifier that provides VDDQ/2 reference voltage applied to the OCSET2 pin.

OCSET2 (Pin 18)

In a dual channel application (DDR = 0), a resistor from this pin to ground sets the overcurrent threshold for the second controller.

In the DDR application (DDR = 1), this pin sets the output voltage of the buffer amplifier and the second controller and should be connected to the center point of a divider from the VDDQ output.

VCC (Pin 28)

This pin powers the controller.

Generic Application Circuits

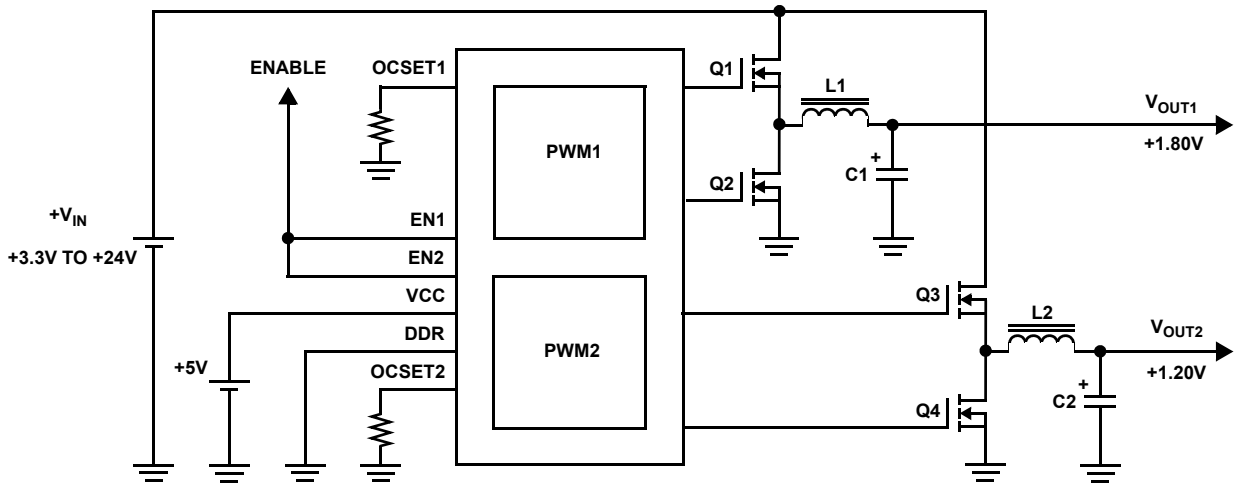


FIGURE 1. ISL6225 APPLICATION CIRCUIT FOR TWO CHANNEL POWER SUPPLY

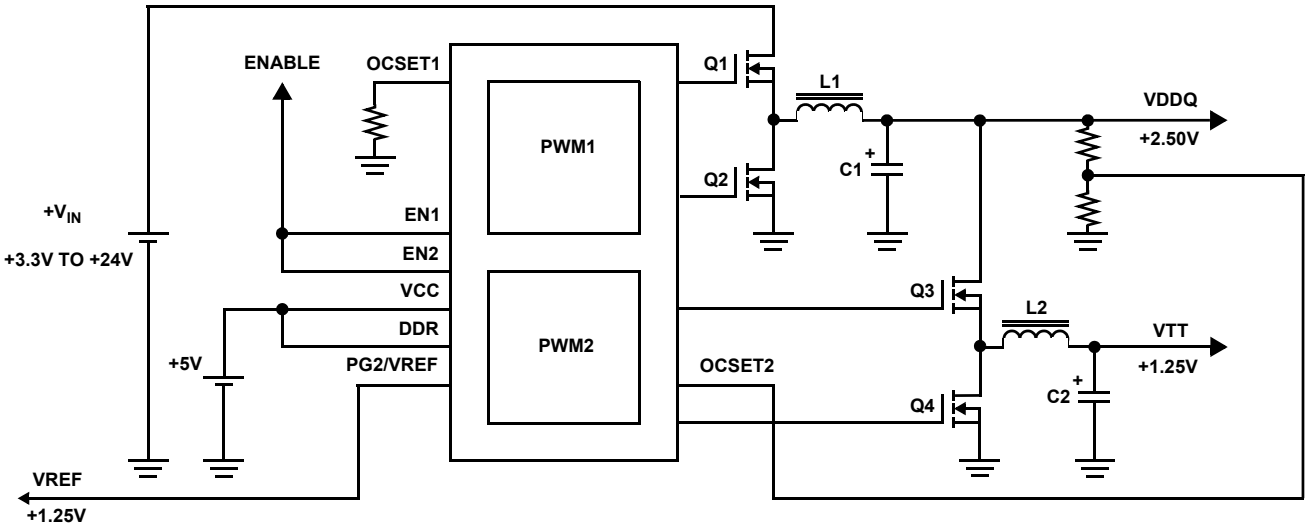
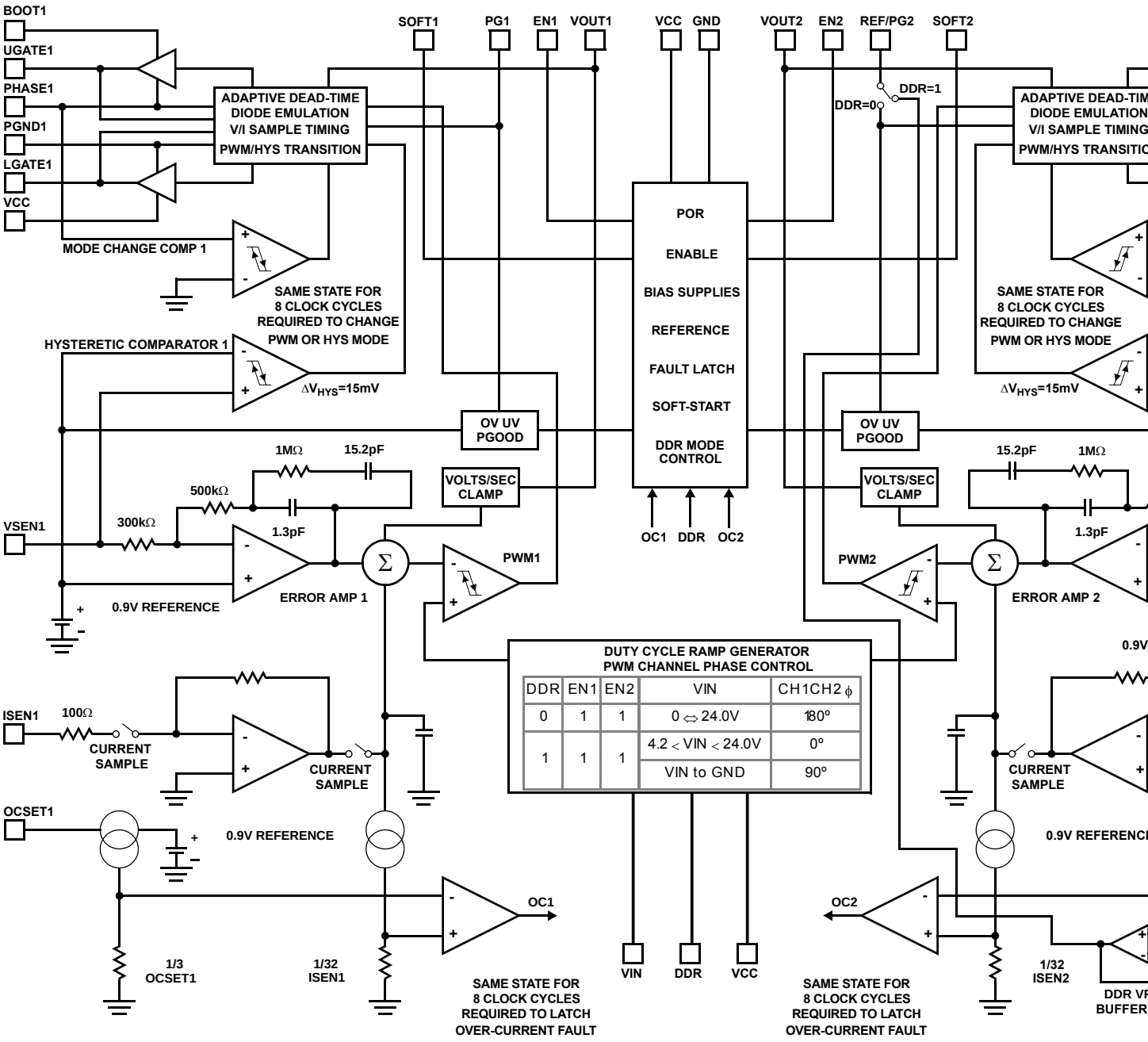


FIGURE 2. ISL6225 APPLICATION CIRCUIT FOR COMPLETE DDR MEMORY POWER SUPPLY

Block Diagram



Description

Operation

The ISL6225 is a dual channel PWM controller intended for use in power supplies for graphic chipset, SDRAM, DDR DRAM or other low voltage power applications in modern notebook and sub-notebook PCs. The IC integrates two control circuits for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistive divider. Out-of-phase operation with 180 degree phase shift reduces input current ripple.

The synchronous buck converters can operate from either an unregulated DC source such as a notebook battery with a voltage ranging from 5.0V to 24V, or from a regulated system rail of 3.3V or 5V. In either mode of operation the controller is biased from the +5V source.

The controllers operate in the current mode with input voltage feed-forward for simplified feedback loop compensation and reduced effect of the input voltage variation. An integrated feedback loop compensation dramatically reduces the number of external components.

Depending on the load level, converters can operate either in a fixed-frequency mode or in a hysteretic mode. Switch-over to the hysteretic mode operation at light loads improves the converters' efficiency and prolongs battery run time. The hysteretic mode of operation can be inhibited independently for each channel if a variable frequency operation is not desired.

The ISL6225 has a special means to rearrange its internal architecture into a complete DDR solution. When DDR input is set high, the second channel can provide the capability to track the output voltage of the first channel. The buffered reference voltage required by DDR memory chips is also provided.

Initialization

The Power-On Reset (POR) function continually monitors the bias supply voltage on the V_{CC} pin and initiates soft-start operation after the input supply voltage exceeds 4.5V. Should this voltage drop lower than 4.0V, the POR disables the chip.

Soft-Start

When soft-start is initiated, the voltage on the SOFT pin starts to ramp gradually due to the 5µA current sourced into the external soft-start capacitor. The output voltage starts to follow the soft-start voltage.

When the SOFT pin voltage reaches a level of 0.9V, the output voltage comes into regulation while the soft-start pin voltage continues to rise. When the SOFT voltage reaches 1.5V, the power good (PGOOD), the mode control, and the fault functions are enabled, as depicted in Figure 3.

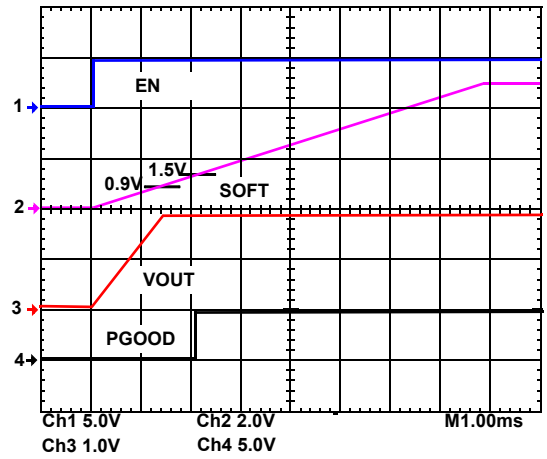


FIGURE 3. START UP

This completes the soft-start sequence. Further rise of pin voltage does not affect the output voltage. During the soft-start, the converter always operates in continuous conduction mode independently of the load level or FCCM pin potential.

The soft-start time (the time from the moment when EN becomes high to the moment when PGOOD is reported) is determined by the following equation.

$$T_{SOFT} = \frac{1.5V \times Csoft}{5\mu A}$$

The time it takes the output voltage to come into regulation can be obtained from the following equation.

$$T_{RISE} = 0.6 \times T_{SOFT}$$

Having such a spread between the time when the output voltage reaches the regulation point and the moment when PGOOD is reported allows for a fault-safe test mode by means of an external circuit that clamps the SOFT pin voltage on the level $0.9V < V_{SOFT} < 1.5V$.

Output Voltage Program

The output voltage of either channel is set by a resistive divider from the output to ground. The center point of the divider is connected to VSEN pin as shown in Figure 4. The output voltage value is determined by the following equation.

$$V_O = \frac{0.9V \bullet (R1 + R2)}{R2}$$

Where 0.9V is the value of the internal reference. The VSEN pin voltage is also used by the controller for the power good function and to detect Undervoltage and Overvoltage conditions.

Automatic Operation Mode Control

In nominal currents the synchronous buck converter operates in continuous-conduction constant-frequency mode. This mode of operation achieves higher efficiency due to the substantially lower voltage drop across the synchronous MOSFET compared to a Schottky diode.

In contrast, continuous-conduction operation with load currents lower than the inductor critical value results in lower efficiency. In this case, during a fraction of a switching cycle, the direction of the inductor current changes to the opposite, actively discharging the output filter capacitor.

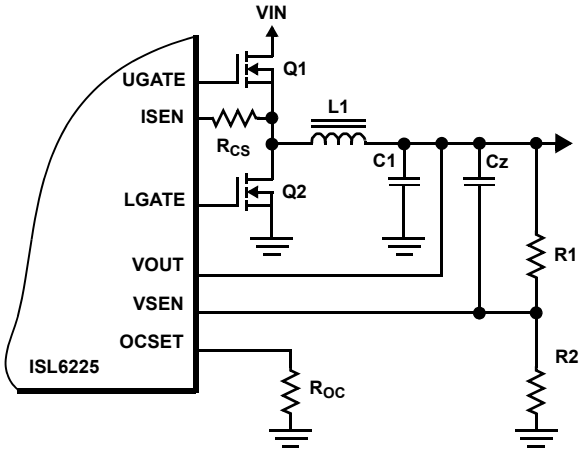


FIGURE 4. OUTPUT VOLTAGE PROGRAM

To maintain the output voltage in regulation, the discharged energy should be restored during the consequent cycle of operation by the cost of increased circulating current and losses associated with it.

The critical value of the inductor current can be estimated by the following expression:

$$I_{HYS} = \frac{(V_{IN} - V_O) \bullet V_O}{2 \bullet F_{SW} \bullet L_O \bullet V_{IN}}$$

To improve converter efficiency at loads lower than critical, the switch-over to variable frequency hysteretic operation with diode emulation is implemented into the PWM scheme. The switch-over is provided automatically by the mode control circuit that constantly monitors the inductor current and alters the way the PWM signal is generated.

The voltage across the synchronous MOSFET at the moment of time just before the upper-MOSFET turns on is monitored for purposes of mode change. When the converter operates at currents higher than critical, this voltage is always negative. In currents lower than critical, the voltage is always positive. The mode control circuit uses a sign of voltage across the synchronous devices to determine if the load current is higher or lower than the critical value.

To prevent chatter between operating modes, the circuit looks for eight contiguous signals of the same polarity before it makes the decision to perform a mode change. The same algorithm is true for both CCM-hysteretic and hysteretic-CCM transitions.

Hysteretic Operation

When the critical inductor current is detected, the converter enters hysteretic mode. The PWM comparator and the error amplifier that provided control in the CCM mode are inhibited and the hysteretic comparator is now activated. A change is also made to the gate logic. In hysteretic mode the synchronous rectifier MOSFET is controlled in diode emulation mode, hence conduction in the second quadrant is prohibited.

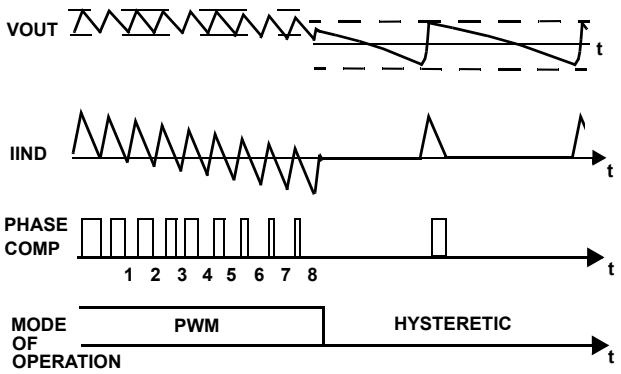


FIGURE 5. CCM - HYSTERETIC TRANSITION

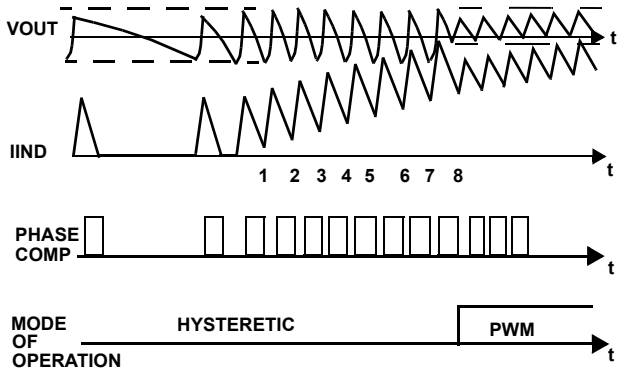


FIGURE 6. HYSTERETIC - CCM TRANSITION

The hysteretic comparator initiates the PWM signal when the output voltage gets below the lower threshold and terminates the PWM signal when the output voltage rises above the upper threshold. A spread or hysteresis between these two thresholds determines the switching frequency and the peak value of the inductor current. The transition to constant frequency CCM mode happens when the inductor current increases above the critical value:

$$I_{CCM} \approx \frac{\Delta V_{hys}}{2 \bullet ESR}$$

Where, ΔV_{hys}= 15mV, is a hysteretic comparator window, ESR is the equivalent series resistance of the output capacitor. Because of different control mechanisms, the value of the load current where transition into CCM operation takes place is usually higher compared to the load level at which transition into hysteretic mode had occurred.

V_{OUT} pin and Forced Continuous Conduction Mode (FCCM)

The controller has the flexibility to operate a converter in fixed-frequency constant conduction mode (CCM), or in hysteretic mode. Connecting the V_{OUT} pin to GND will inhibit hysteretic mode; this is called forced constant conduction mode (FCCM). Connecting the V_{OUT} pin to the converter output will allow transition between CCM mode and hysteretic mode.

When the V_{OUT} pin is connected to the converter output, a circuit is activated that smooths the transition from hysteretic mode to CCM mode. While in hysteretic mode, this circuit prepositions the PWM error amplifier output to a level close to that needed to provide the appropriate PWM duty cycle required for regulation. This is a much more desirable state for the PWM error amplifier at mode transition, as opposed to being in saturation which requires a period of time to slew to the required level.

Such dual function of the V_{OUT} pin enhances applicability of the controller and allows for lower pin count.

Feedback Loop Compensation

To reduce the number of external components and remove the burden of determining compensation components from a system designer, both PWM controllers have internally compensated error amplifiers. To make internal compensation possible several design measures where taken.

First, the ramp signal applied to the PWM comparator is proportional to the input voltage provided via the VIN pin. This keeps the modulator gain constant when the input voltage varies. Second, the load current proportional signal is derived from the voltage drop across the lower MOSFET during the $\overline{PWM}$ time interval and is added to the amplified error signal on the comparator input. This effectively creates an internal current control loop. The resistor connected to the ISEN pin sets the gain in the current feedback loop. The following expression estimates the required value of the current sense resistor depending on the maximum load current and the value of the MOSFET's $r_{DS(ON)}$.

$$R_{CS} = \frac{I_{MAX} \cdot r_{DS(ON)}}{75\mu A} - 100\Omega$$

Due to implemented current feedback, the modulator has a single pole response with -1 slope at a frequency determined by the load,

$$F_{PO} = \frac{1}{2\pi \cdot R_O \cdot C_O}$$

where: Ro is load resistance and Co is load capacitance. For this type of modulator, a Type 2 compensation circuit is usually sufficient.

Figure 7 shows a Type 2 amplifier and its response along with the responses of the current mode modulator and the converter. The Type 2 amplifier, in addition to the pole at origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole:

$$F_Z = \frac{1}{2\pi \cdot R_2 \cdot C_1} = 6kHz$$

$$F_P = \frac{1}{2\pi \cdot R_1 \cdot C_2} = 600kHz$$

This region is also associated with phase 'bump' or reduced phase shift. The amount of phase shift reduction depends on how wide the region of flat gain is and has a maximum value of 90°. To further simplify the converter compensation, the modulator gain is kept independent of the input voltage variation by providing feed-forward of V_{IN} to the oscillator ramp.

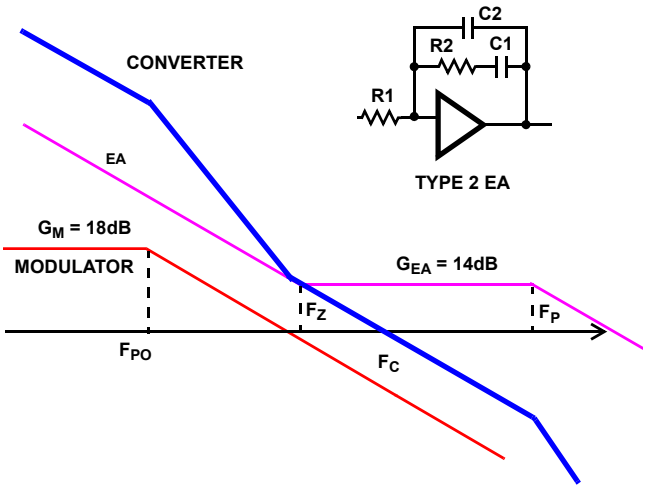


FIGURE 7. FEEDBACK LOOP COMPENSATION

The zero frequency, the amplifier high-frequency gain, and the modulator gain are chosen to satisfy most typical applications. The crossover frequency will appear at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation plenty of phase margin is easily achieved due to zero-pole pair phase 'boost'. Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within 10kHz...50kHz range gives some additional phase 'boost'. Some phase boost can also be achieved by connecting capacitor C_z in parallel with the upper resistor R1 of the divider that sets the output voltage value, as shown in Figure 4.

Gate Control Logic

The gate control logic translates generated PWM signals into gate drive signals providing necessary amplification, level shift, and shoot-trough protection. Also, it bears some functions that help to optimize the IC performance over a wide range of the operational conditions. As MOSFET switching time can very dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring real gate waveforms of both the upper and the lower MOSFETs.

Dual-Step Conversion

The ISL6225 dual channel controller can be used either in power systems with a single-stage power conversion when the battery power is converted into the desired output voltage in one step, or in the systems where some intermediate voltages are initially established. The choice of the approach may be dictated by the overall system design criteria or simply to be a matter of voltages available to the system designer, like in the case of PCI card applications.

When the power input voltage is a regulated 5V or 3.3V system bus, the feed-forward ramp may become too shallow, which creates the possibility of duty-factor jitter especially in a noisy environment. The noise susceptibility when operating from low level regulated power sources can be improved by connecting the VIN pin to ground. The feed-forward ramp generator will be internally reconnected from the VIN pin to the V_{CC} pin and the ramp slew rate will be doubled. Application circuits for dual-step power conversion are presented in Figures 11 through 15.

Protections

The converter output is monitored and protected against extreme overload, short circuit, Overvoltage, and Undervoltage conditions.

A sustained overload on the output sets the PGOOD low and latches-off the whole chip. The controller operation can be restored by cycling the VCC voltage or an enable (EN) pin.

Overcurrent Protection

Both PWM controllers use the lower MOSFET's on-resistance $\{r_{DS(ON)}\}$ to monitor the current for protection against shorted outputs. The sensed current from the ISEN pin is compared with a current set by a resistor connected from the OCSET pin to ground.

$$R_{OCSET} = \frac{9.6V \bullet (R_{CS} + 100\Omega)}{I_{OC} \bullet R_{DS(ON)}}$$

Where, I_{OC} is a desired overcurrent protection threshold and R_{CS} is the value of the current sense resistor connected to the I_{SEN} pin.

If the lower MOSFET current exceeds the overcurrent threshold, a pulse skipping circuit is activated. The upper MOSFET will not be turned on as long as the sensed current is higher then the threshold value. This limits the current supplied by the DC voltage source. This condition keeps on for eight clock cycles after the overcurrent comparator was tripped for the first time. If after these first eight clock cycles the current exceeds the overcurrent threshold again in a time interval of another eight clock cycles, the overcurrent protection latches and disables the chip. If the overcurrent condition goes away during the first eight clock cycles, normal operation is restored and the overcurrent circuit resets itself sixteen clock cycles after the overcurrent threshold was exceeded the first time, Figure 8.

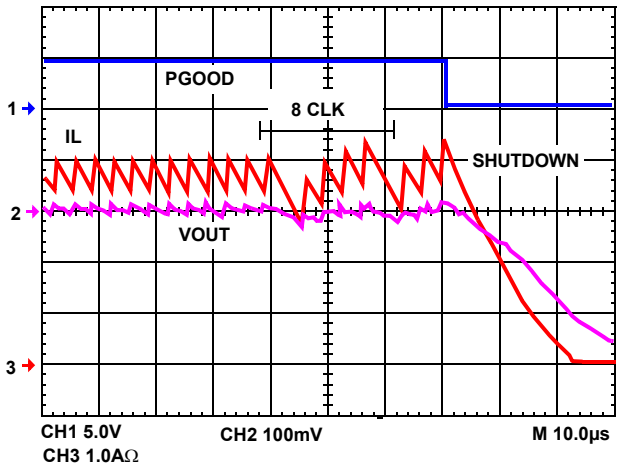


FIGURE 8. OVERCURRENT PROTECTION WAVEFORMS

If load step is strong enough to pull output voltage lower than the undervoltage threshold, the chip shuts down immediately.

Because of the nature of the used current sensing technique, and to accommodate wide range of the $r_{DS(ON)}$ variation, the value of the overcurrent threshold should represent overload current about 150%...180% of the nominal value. If more precise current protection is desired, a current sense resistor placed in series with the lower MOSFET source may be used.

Overvoltage Protection

Should the output voltage increase over 115% of the normal value due to the upper MOSFET failure, or other reasons, the overvoltage protection comparator will force the synchronous rectifier gate driver high. This action actively pulls down the output voltage and eventually attempts to blow the battery fuse. As soon as the output voltage drops below the threshold, the OVP comparator is disengaged.

This OVP scheme provides a ‘soft’ crowbar function which helps to tackle severe load transients and does not invert the output voltage when activated - a common problem for OVP schemes with a latch.

Over-Temperature Protection

The chip incorporates an over-temperature protection circuit that shuts the chip down when the die temperature of 150°C is reached. Normal operation restores at die temperatures below 125°C through the full soft-start cycle.

DDR Application

Double Data Rate (DDR) memory chips are expected to take the place of traditional memory in many newly designed computers, including high-end notebooks, due to increased throughput. A novel feature associated with this type of memory is new referencing and data bus termination techniques. These techniques employ a reference voltage, VREF, that tracks the center point of VDDQ and VSS voltages and an additional VTT power source to which all terminating resistors are connected. Despite the additional power source, the overall memory power consumption is reduced compared to traditional termination.

The added power source has a cluster of requirements that should be observed and considered. Due to reduced differential thresholds of DDR memory, the termination power supply voltage, VTT, shall closely track VDDQ/2 voltage. Another very important feature for the termination power supply is a capability to equally operate in sourcing and sinking modes. The VTT supply shall regulate the output voltage with the same degree of precision when current is floating from the supply to the load and when the current is diverted back from the load into the power supply. The last mode of operation usually conflicts with the way most PWM controllers operate.

The ISL6225 dual channel PWM controller possesses several important means that allow reconfiguration for this particular application and provide all three voltages required in DDR memory-compliant computer.

To reconfigure the ISL6225 for a complete DDR solution, the DDR pin shall be permanently set high. The simplest way to do that is to connect it to the V_{CC} rail. This activates some functions inside the chip that are specific to the DDR memory power needs.

In the DDR application presented in Figures 14 and 15, the first controller regulates the VDDQ rail to 2.5V. The output voltage is set by an external divider R3 and R5. The second controller regulates the VTT rail to VDDQ/2. The OCSET2 pin function is now different. The pin serves now as an input that brings VDDQ/2 voltage created by R4 and R6 divider inside the chip. That effectively provides a tracking function for the VTT voltage.

The PG2 pin function is also different in DDR mode. This pin becomes the output of the buffer, which input is connected via the OCSET2 pin to the center point of the R/R divider from the VDDQ output. The buffer output voltage serves as 1.25V reference for the DDR memory chips. Current capability of this pin is about 10mA.

For the VTT channel some control and protective functions can be significantly simplified as this output is derived from the VDDQ output. For example, the overcurrent and overvoltage protections for the second controller are disabled when the DDR pin is set high. The hysteretic mode of operation is also disabled on the VTT channel to allow sinking capability to be independent from the load level. As the VTT channel tracks the VDDQ/2 voltage, the soft-start function is not required and the SOFT2 pin may be left open.

Channel Synchronization in DDR Applications

Presence of two PWM controllers on the same die require channel synchronization to reduce inter channel interference that may cause the duty factor jitter and increased output ripple. The PWM controller is mostly susceptible to noise when an error signal on the input of the PWM comparator approaches the decision making point. False triggering can occur causing jitter and affecting the output regulation.

Out-of-phase operation is a common approach to synchronize dual channel converters as it reduces an input current ripple and provides a minimum interference for channels that control different voltage levels. When used in DDR application with cascaded converters (VTT generated from VDDQ), the turn-on of the upper MOSFET in the VDDQ channel happens to be just before the decision making point in the VTT channel that is running with a duty-factor close to 50%, as in Figure 10.

This makes out-of-phase channel synchronization undesirable when one of the channels is running on a duty-factor of 50%. Inversely, the in-phase channel arrangement does not have this drawback. Points of decision are far from noisy moments of time in both sourcing and sinking modes of operation for V_{IN} = 7.5V to 24V as it is shown in Figure 9.

In the case when power for VDDQ is taken from the +5V system rail, as Figure 10 shows, both in-phase and out-of-phase approaches are susceptible to noise in the sourcing mode.

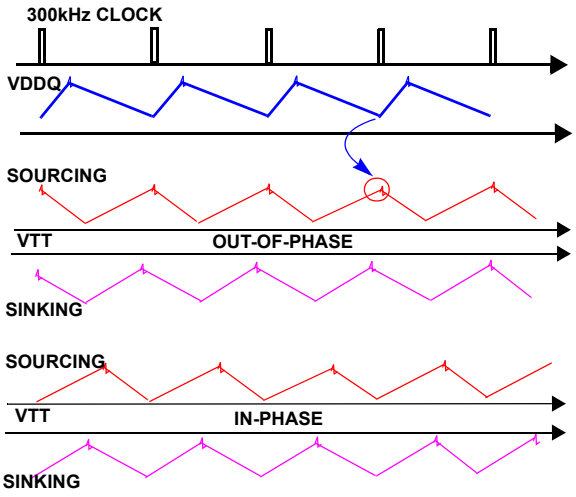


FIGURE 9. CHANNEL INTERFERENCE V_{IN} = 7.5V...24V

Noise immunity can be improved by operating the VTT converter with a 90° phase shift. As the time diagrams in Figure 10 show, the points of concern are always about a quarter of the period away from the noise emitting transitions.

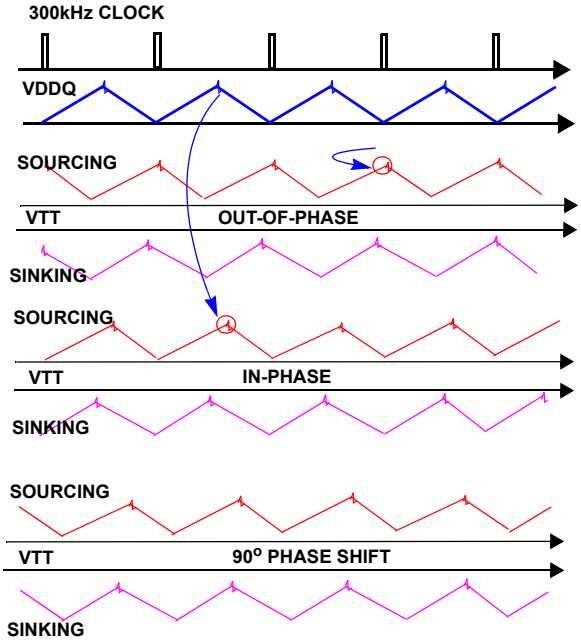


FIGURE 10. CHANNEL INTERFERENCE V_{IN} = 5V

Several ways of synchronization are implemented into the chip. When the DDR pin is connected to GND, the channels operate 180° out-of-phase. In the DDR mode when the DDR pin is connected to V_{CC}, the channels operate either in-phase when the V_{IN} pin is connected to the input voltage source, or with 90° phase shift if the VIN pin is connected to GND.

ISL6225 DC-DC Converter Application Circuits

Figures 11 and 12 show application circuits of a dual channel DC/DC converter for a notebook PC.

The power supply in Figure 11 provides +2.5V and +1.8V for memory and graphic interface chipset from +5.0V to +24V battery voltage.

Figure 12 shows the power supply that provides +2.5V and +1.8V for memory and graphic interface chipset from +5.0V system rail.

Figure 13 shows an application circuit for a single-output split input power supply with current sharing for advanced graphic card applications.

Figure 14 and 15 show application circuits of a complete power solution for DDR memory that becomes a preferred choice in modern computers. The power supply shown in Figure 14 generates +2.5V VDDQ voltage from +5.0V to +24V battery voltage. The +1.25V VTT termination voltage tracks VDDQ/2 and is derived from +2.5V VDDQ. To complete the DDR memory power requirements, the +1.25V reference voltage is also provided. The PG2 pin serves as an output for the reference voltage in this mode.

Figure 15 depicts the DDR solution in the case where the 5V system rail is used as a primary voltage source.

For detailed information on the circuit, including a Bill-of-Materials and circuit board description, see Application Note AN9995. Also see Intersil's web site (http://www.intersil.com) for the latest information.

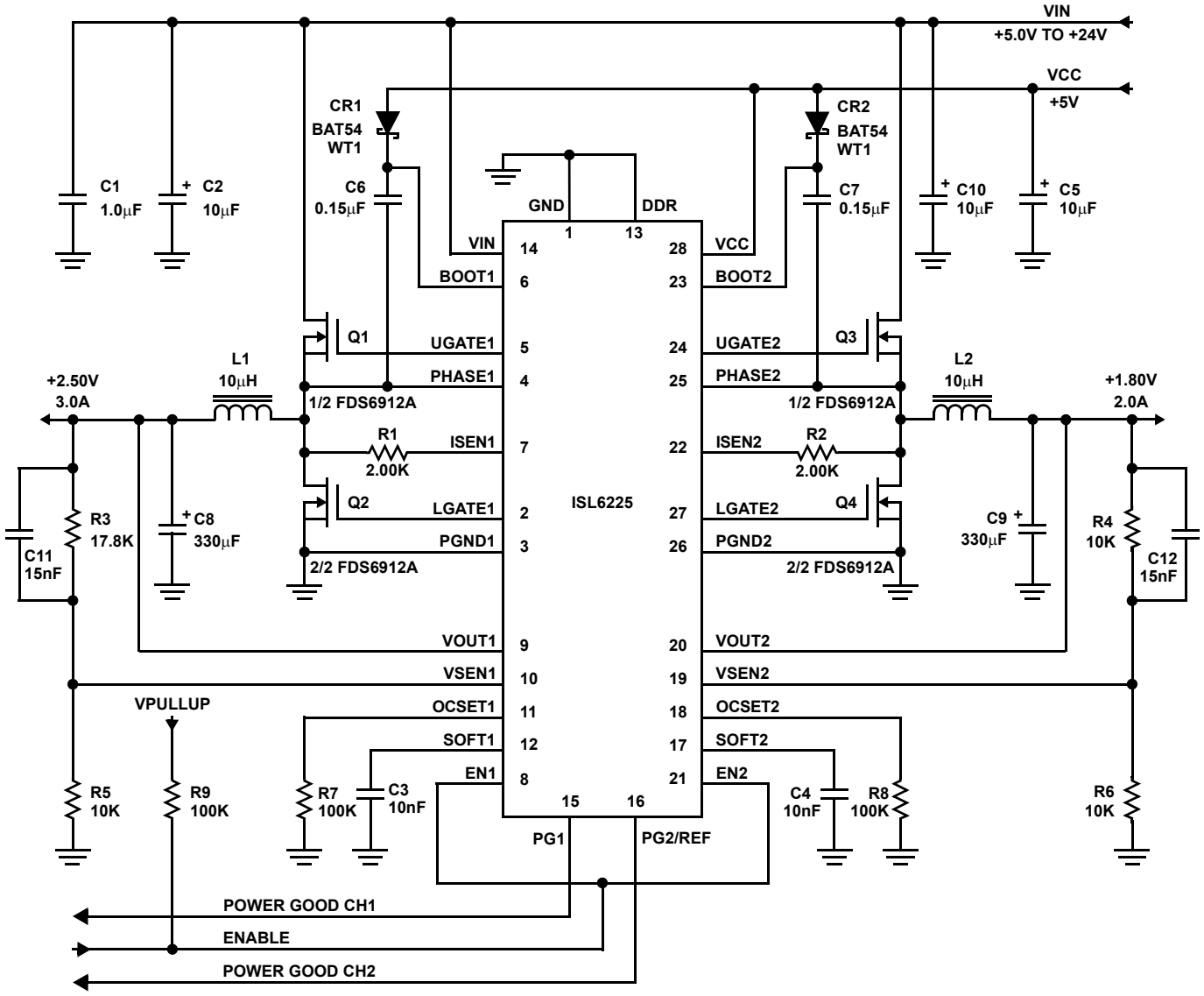


FIGURE 11. DUAL OUTPUT APPLICATION CIRCUIT FOR ONE-STEP CONVERSION

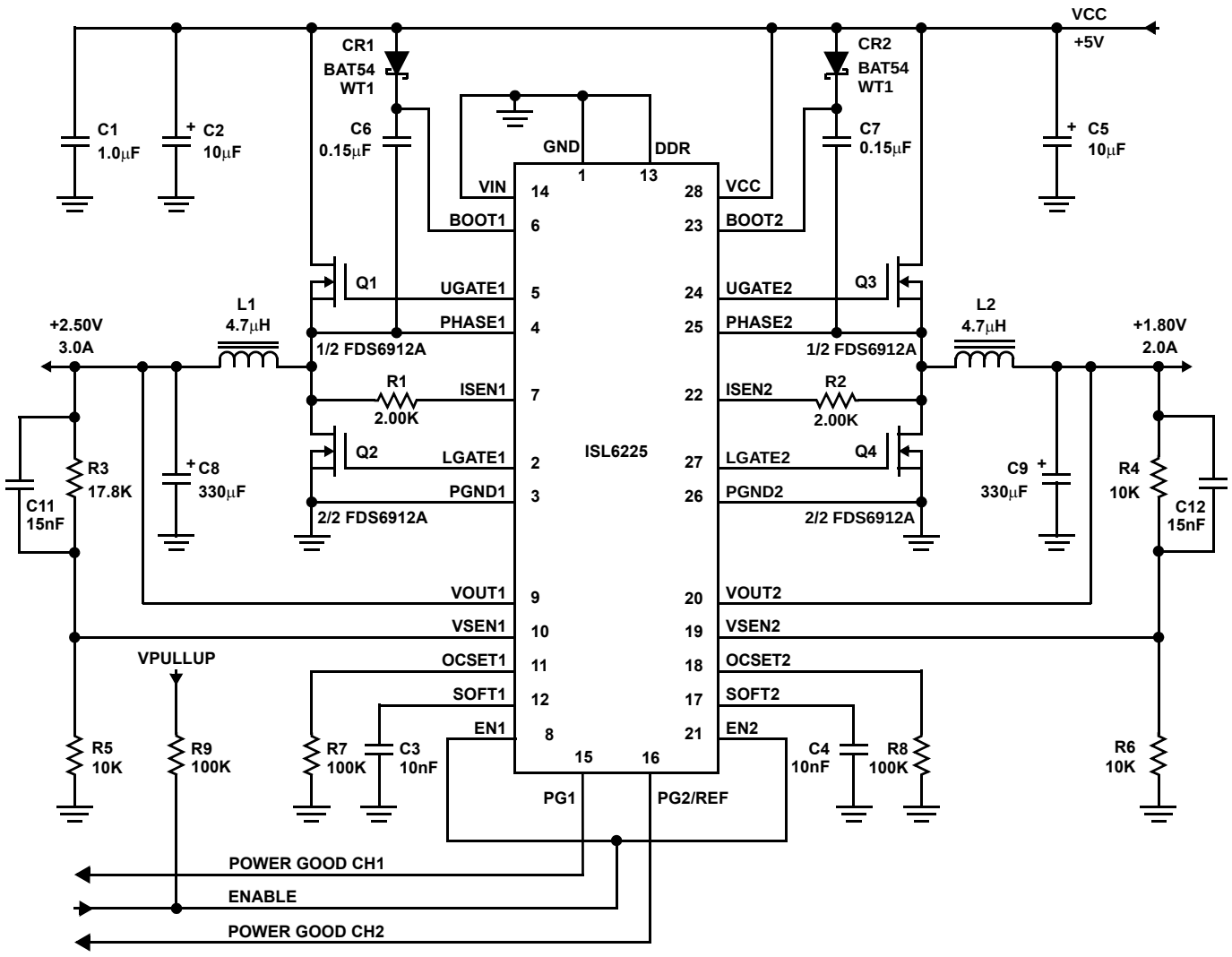


FIGURE 12. DUAL OUTPUT APPLICATION CIRCUIT FOR TWO-STEP CONVERSION

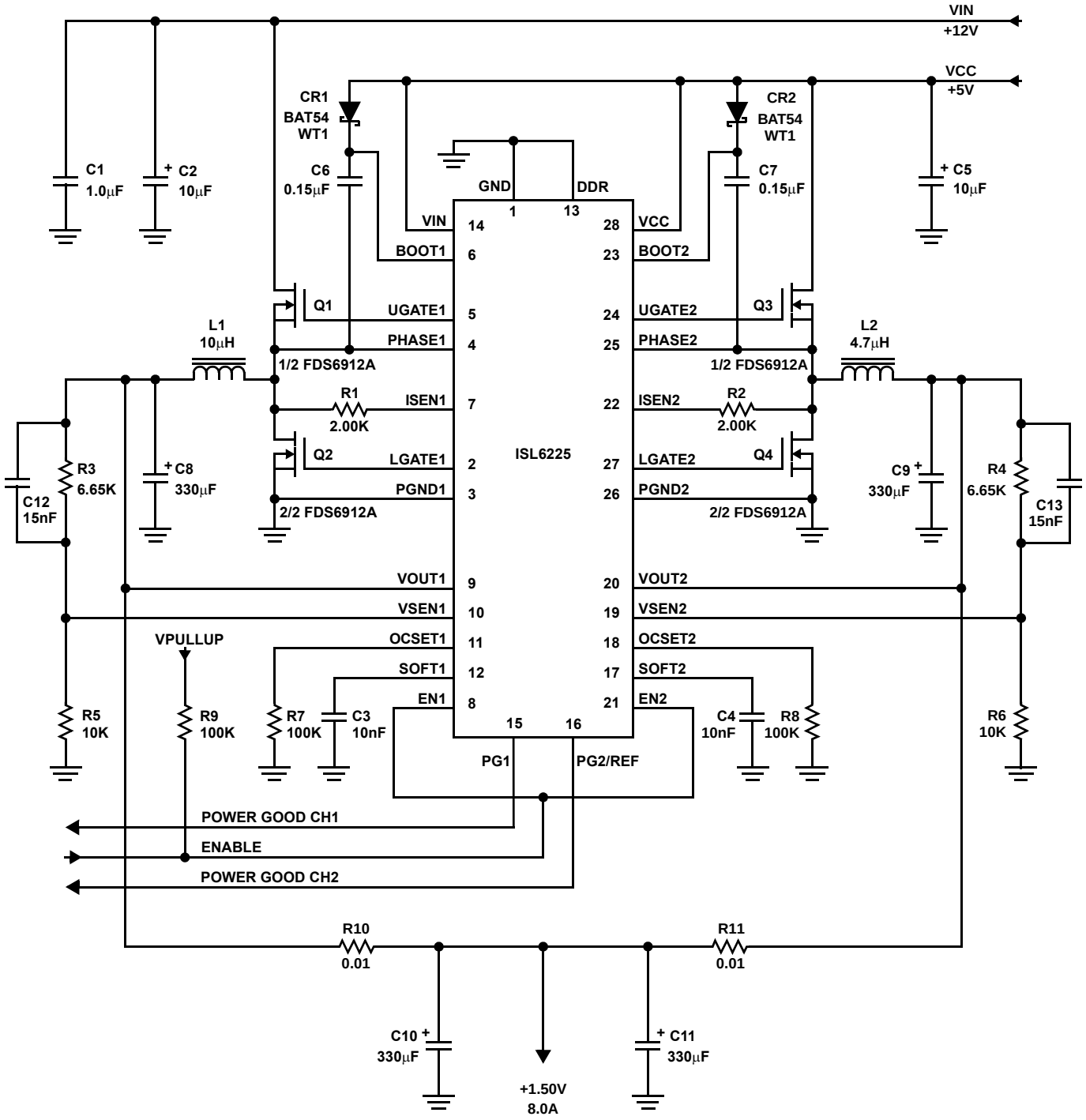


FIGURE 13. SINGLE-OUTPUT SPLIT INPUT POWER SUPPLY

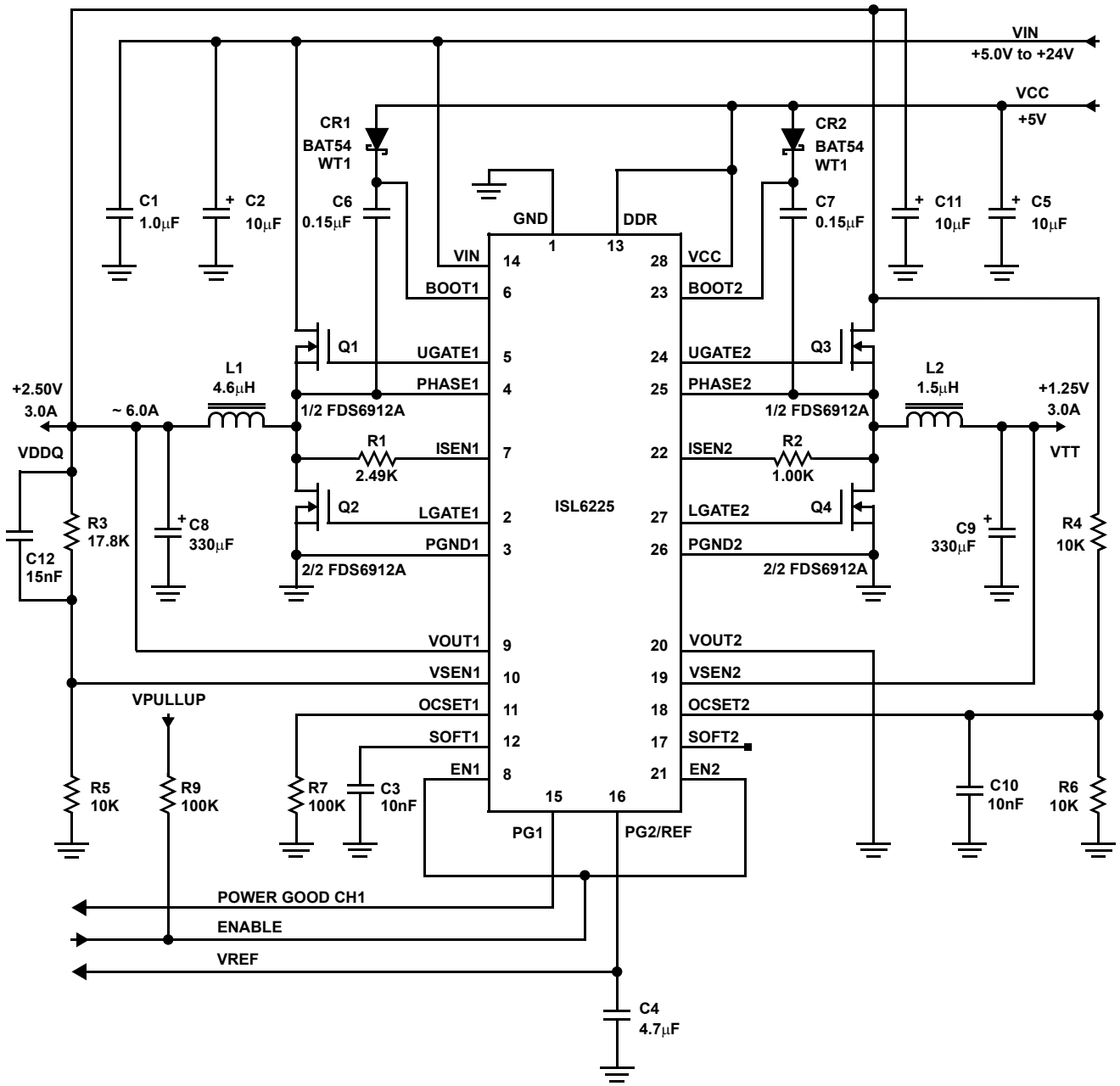


FIGURE 14. APPLICATION CIRCUIT FOR COMPLETE DDR MEMORY POWER SOLUTION WITH ONE-STEP CONVERSION

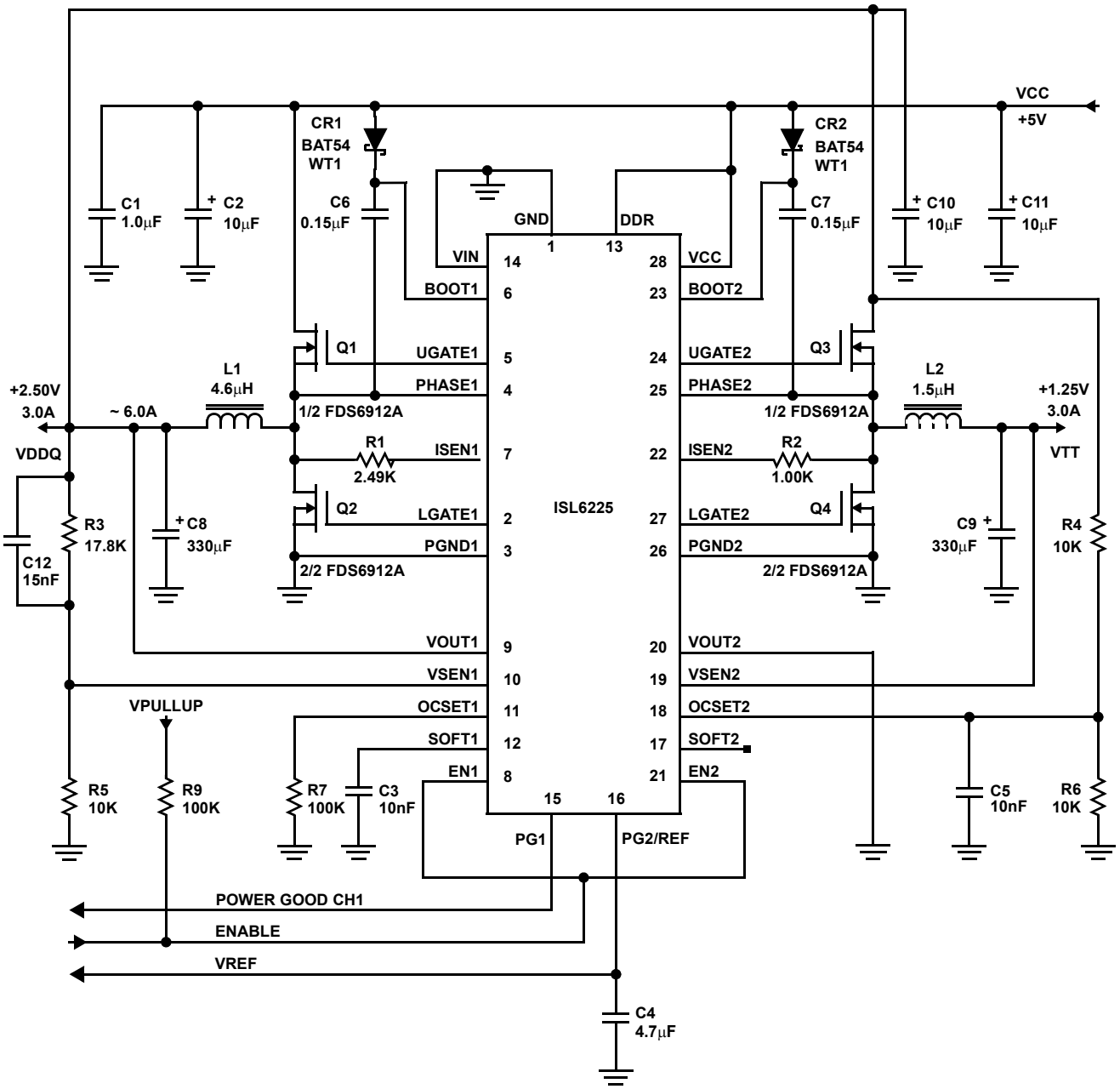
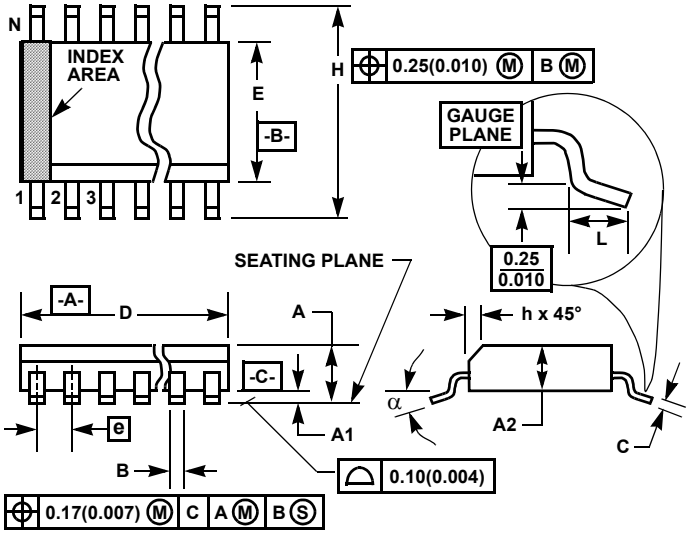


FIGURE 15. APPLICATION CIRCUIT FOR COMPLETE DDR MEMORY POWER SOLUTION WITH TWO-STEP CONVERSION

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M28.15

28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

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