Ordering Information

Product program	Output
PMR 5118UW	0.7-3.6 V, 50 A / 180 W

Product number and Packaging

PMR 5118UW n_1n_2		
Options	n_1	n_2
Mounting	o	
Delivery package information		o

Options		Description
n_1	P	Through hole
	S	Surface mount (SMD pin)
	SR	SMD pin with lead-free surface
n_2	/B	Tray
	/C	Tape and Reel

Example: a surface mounted, lead-free SMD pin surface, tray packaged product would be PMR 5118UW SR /B.

General Information

Reliability

The Mean Time Between Failure (MTBF) is calculated at full output power and an operating ambient temperature (T_A) of +40°C, which is a typical condition in Information and Communication Technology (ICT) equipment. Different methods could be used to calculate the predicted MTBF and failure rate which may give different results. Ericsson Power Modules currently uses Telcordia SR332.

Predicted MTBF for the series is:
- 1.5 million hours according to Telcordia SR332, issue 1, Black box technique.

Telcordia SR332 is a commonly used standard method intended for reliability calculations in ICT equipment. The parts count procedure used in this method was originally modelled on the methods from MIL-HDBK-217F, Reliability Predictions of Electronic Equipment. It assumes that no reliability data is available on the actual units and devices for which the predictions are to be made, i.e. all predictions are based on generic reliability parameters.

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2002/95/EC and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Ericsson Power Modules products include:
- Lead in high melting temperature type solder (used to solder the die in semiconductor packages)
- Lead in glass of electronics components and in electronic ceramic parts (e.g. fill material in chip resistors)
- Lead as an alloying element in copper alloy containing up to 4% lead by weight (used in connection pins made of Brass)

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, 6σ (sigma), and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of our products.

Warranty

Warranty period and conditions are defined in Ericsson Power Modules General Terms and Conditions of Sale.

Limitation of Liability

Ericsson Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

Safety Specification

General information

Ericsson Power Modules DC/DC converters and DC/DC regulators are designed in accordance with safety standards IEC/EN/UL60950, *Safety of Information Technology Equipment*.

IEC/EN/UL60950 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Energy hazards
- Fire
- Mechanical and heat hazards
- Radiation hazards
- Chemical hazards

On-board DC-DC converters and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any Safety requirements without “Conditions of Acceptability”. Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable Safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable Safety standards and Directives for the final product.

Component power supplies for general use should comply with the requirements in IEC60950, EN60950 and UL60950 *“Safety of information technology equipment”.*
There are other more product related standards, e.g. IEEE802.3af “Ethernet LAN/MAN Data terminal equipment power”, and ETS300132-2 “Power supply interface at the input to telecommunications equipment; part 2: DC”, but all of these standards are based on IEC/EN/UL60950 with regards to safety.

Ericsson Power Modules DC/DC converters and DC/DC regulators are UL60950 recognized and certified in accordance with EN60950.

The flammability rating for all construction parts of the products meets requirements for V-0 class material according to IEC 60695-11-10.

The products should be installed in the end-use equipment, in accordance with the requirements of the ultimate application. Normally the output of the DC/DC converter is considered as SELV (Safety Extra Low Voltage) and the input source must be isolated by minimum Double or Reinforced Insulation from the primary circuit (AC mains) in accordance with IEC/EN/UL60950.

Isolated DC/DC converters

It is recommended that a slow blow fuse with a rating twice the maximum input current per selected product be used at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter.
In the rare event of a component problem in the input filter or in the DC/DC converter that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the faulty DC/DC converter from the input power source so as not to affect the operation of other parts of the system.
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating.

The galvanic isolation is verified in an electric strength test. The test voltage (V_{iso}) between input and output is 1500 Vdc or 2250 Vdc for 60 seconds (refer to product specification).
Leakage current is less than 1 µA at nominal input voltage.

24 V DC systems

The input voltage to the DC/DC converter is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

48 and 60 V DC systems

If the input voltage to the DC/DC converter is 75 Vdc or less, then the output remains SELV (Safety Extra Low Voltage) under normal and abnormal operating conditions.

Single fault testing in the input power supply circuit should be performed with the DC/DC converter connected to demonstrate that the input voltage does not exceed 75 Vdc.

If the input power source circuit is a DC power system, the source may be treated as a TNV2 circuit and testing has demonstrated compliance with SELV limits and isolation requirements equivalent to Basic Insulation in accordance with IEC/EN/UL60950.

Non-isolated DC/DC regulators

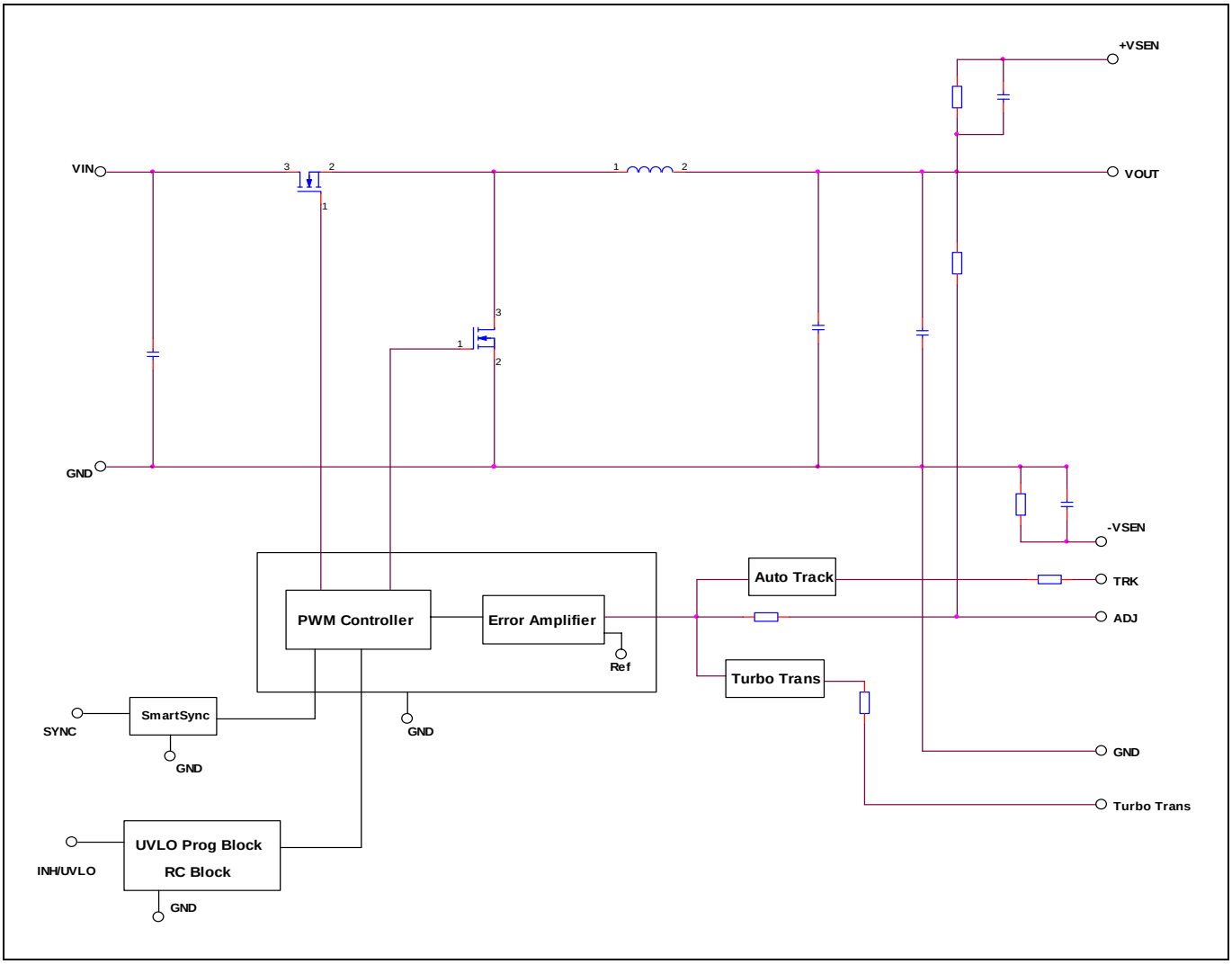
The input voltage to the DC/DC regulator is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

Absolute Maximum Ratings

Characteristics			min	typ	max	Unit
T_{ref}	Operating Temperature (see Thermal Consideration section)		–40		85	°C
T_S	Storage temperature		–40		125	°C
V_I	Input voltage		4.5	5/12	14	V
V_{RC}	Remote Control pin voltage (see Operating Information section)	Positive logic option	-0.2		Open	V
		Negative logic option	N/A		N/A	V
V_{adj}	Adjust pin voltage (see Operating Information section)		N/A		N/A	V

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits in the Electrical Specification. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

Fundamental Circuit Diagram



0.7V, 50A / 35.0W Electrical Specification — PMR 5118UW

T_{P1} = -40 to +85ºC, V_I = 4.5 to 14 V, R_{SET} = OPEN, unless otherwise specified under Conditions.
Typical values given at: T_{P1}= +25°C, V_I= 5/12 V, max I_O , unless otherwise specified under Conditions.
Additional C_{in} = 1000+22 µF and C_{out} = 660 µF. See Operating Information section for selection of capacitor types.
Connect the sense pin, where available, to the output pin.

Characteristics			Conditions	min	typ	max	Unit
V_I	Input voltage range			4.5	5/12	14	V
V_{Ioff}	Turn-off input voltage		Decreasing input voltage	4.0	4.2		V
V_{Ion}	Turn-on input voltage		Increasing input voltage		4.3	4.45	V
C_I	Internal input capacitance				44		µF
P_O	Output power			0		35	W
η	Efficiency	V_I = 5 V	V_I = 5 V, 50 % of max I_O		86.8		%
			V_I = 5 V, max I_O		80.7		
		V_I = 12 V	V_I = 12 V, 50 % of max I_O		83.4		
			V_I = 12 V, max I_O		79.4		
P_d	Power Dissipation		V_I = 5 V, max I_O		8.34	8.50	W
			V_I = 12 V, max I_O		9.05	9.50	W
P_{li}	Input idling power		V_I = 5 V, I_O= 0 A		0.45		W
			V_I = 12 V, I_O= 0 A		1.05		W
P_{RC}	Input standby power		V_I = 5 V (turned off with RC)		46.0		mW
			V_I = 12 V (turned off with RC)		102		mW
I_S	Static Input current		V_I = 5 V, max I_O		8.49		A
			V_I = 12 V, max I_O		4.86		A
f_s	Switching frequency		0-100 % of max I_O, see Note 1		600		kHz
V_{Oi}	Output voltage initial setting and accuracy		T_{P1} = +25°C, V_I = 5/12 V, max I_O	0.693	0.700	0.707	V
V_O	Output voltage tolerance band		10-100 % of max I_O	0.689		0.711	V
	Idling voltage		V_I = 5 V, I_O = 0 A		0.701		V
			V_I = 12 V, I_O = 0 A		0.701		
	Line regulation		max I_O		±5		mV
	Load regulation		V_I = 5/12 V, 0-100 % of max I_O		±5		mV
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs Without Turbo Trans C_o =660 µF Type C, see Note 2		±160		mV
t_{tr}	Load transient recovery time				100		µs
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs With Turbo Trans C_o =3300 µF Type C; R_{TT} =SHORT, see Note 2		±45		mV
t_{tr}	Load transient recovery time				100		µs
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 5 V, 100 % of max I_O		7.5		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				22.2		ms
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 12 V, 100 % of max I_O		6.9		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				13.7		ms
t_f	V_I shut-down fall time. (From V_I off to 10 % of V_O)	V_I = 5 V	Max I_O		0.07		ms
			I_O = 0.1 A		17.1		ms
		V_I = 12 V	Max I_O		1.1		ms
			I_O = 0.1 A		96.4		ms
t_{RC} t_{Inh}	RC start-up time		V_I = 5 V , Max I_O		21.9		ms
			V_I = 12 V , Max I_O		12.1		ms
	RC shut-down	V_I = 5 V	Max I_O		0.037		ms

	fall time (From RC off to 10 % of V_O)	V_I = 12 V	I_o = 0.1 A	15.4		ms
			Max I_O	0.121		ms
			I_o = 0.1 A	16.2		ms
I_O	Output current			0	50	A
I_{lim}	Current limit threshold		T_{P1} < max T_{P1}	100		A
I_{sc}	Short circuit current		T_{P1} = 25ºC, see Note 3	110		A
C_{out}	Recommended Capacitive Load		T_{P1} = 25ºC, see Note 4	1000	10000	µF
V_{Oac}	Output ripple & noise V_I = 5 V		See ripple & noise section, max I_O	5.6		mVp-p
V_{Oac}	Output ripple & noise V_I = 12 V		See ripple & noise section, max I_O	36		mVp-p

Note 1: Frequency may be adjusted with SmartSync pin. See Operating Information section

Note 2: See Operating Information section for TurboTrans technology

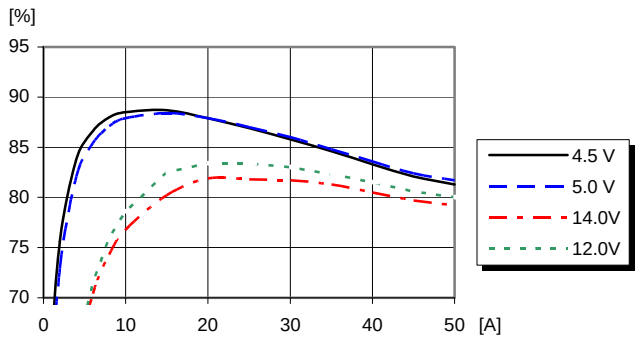
Note 3: Describe short circuit current characteristic, i.e. fold-back, hiccup or RMS, in one short sentence or type only “See Operating Information section.”)

Note 4: 1000 µF of external non-ceramic output capacitance is required for basic operation. Adding additional capacitance at the load further improves transient response. Up to 1000 µF of ceramic capacitance may be added in addition to the required non-ceramic capacitance. When not using TurboTrans technology, 8000 µF capacitance is allowed; When using TurboTrans technology, up to 10000 µF capacitance is allowed. For more information, see Operating Information Section.

0.7V, 50A / 35.0W Typical Characteristics

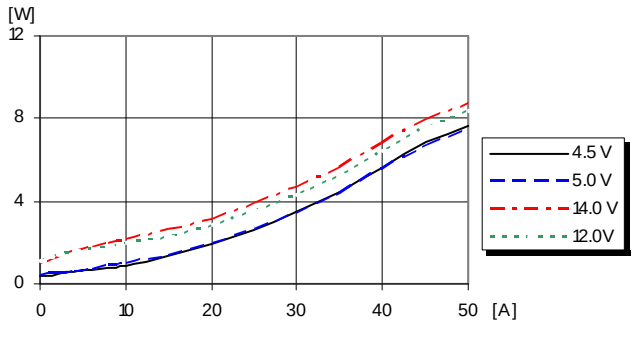
PMR 5118UW

Efficiency



Efficiency vs. load current and input voltage at T_{P1} = +25°C

Power Dissipation



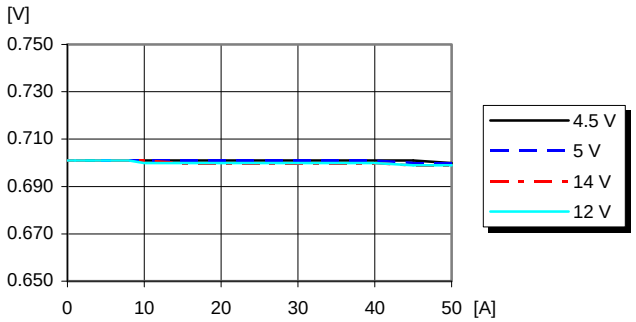
Dissipated power vs. load current and input voltage at T_{P1} = +25°C

Output Current Derating

TBD

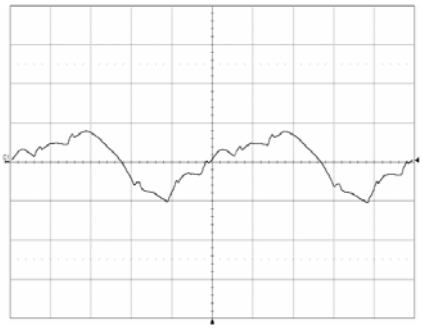
Output current derating information is available only for 1.2V and 3.3V output.

Output Characteristics



Output voltage vs. load current at T_{P1} = +25°C

Output Ripple & Noise



Output voltage ripple at:
T_{P1} = +25°C, V_I = 12 V,
I_O = 50 A resistive load.

Trace: output voltage 20mV/div.
Time scale: 2 µs/div.

Output Voltage Adjust (see operating information)

Passive adjust
The resistor value for an adjusted output voltage is calculated by using the equations in the operating information.

$$R_{SET} = 30.1\,k\Omega \times \frac{0.7}{V_O - 0.7} - 6.49\,k\Omega$$

1.0V, 50A / 50.0W Electrical Specification — PMR 5118UW

T_{P1} = -40 to +85ºC, V_I = 4.5 to 14 V, R_{SET} = 63.4 kΩ, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25°C, V_I= 5/12 V, max I_O , unless otherwise specified under Conditions.
Additional C_{in} = 1000+22 µF and C_{out} = 660 µF. See Operating Information section for selection of capacitor types.
Connect the sense pin, where available, to the output pin.

Characteristics			Conditions	min	typ	max	Unit
V_I	Input voltage range			4.5	5/12	14	V
V_{Ioff}	Turn-off input voltage		Decreasing input voltage	4.0	4.2		V
V_{Ion}	Turn-on input voltage		Increasing input voltage		4.3	4.45	V
C_I	Internal input capacitance				44		µF
P_O	Output power			0		50	W
η	Efficiency	V_I = 5 V	V_I = 5 V, 50 % of max I_O		90.1		%
			V_I = 5 V, max I_O		85.4		
		V_I = 12 V	V_I = 12 V, 50 % of max I_O		86.5		
			V_I = 12 V, max I_O		83.5		
P_d	Power Dissipation		V_I = 5 V, max I_O		8.4	8.7	W
			V_I = 12 V, max I_O		9.85	10.3	W
P_{Ii}	Input idling power		V_I = 5 V, I_O= 0 A		0.45		W
			V_I = 12 V, I_O= 0 A		1.19		W
P_{RC}	Input standby power		V_I = 5 V (turned off with RC)		45.7		mW
			V_I = 12 V (turned off with RC)		102		mW
I_S	Static Input current		V_I = 5 V, max I_O		11.68		A
			V_I = 12 V, max I_O		4.98		A
f_s	Switching frequency		0-100 % of max I_O		600		kHz
V_{Oi}	Output voltage initial setting and accuracy		T_{P1} = +25°C, V_I = 5/12 V, max I_O	0.990	1.000	1.010	V
V_O	Output voltage tolerance band		10-100 % of max I_O	0.985		1.015	V
	Idling voltage		V_I = 5 V, I_O = 0 A		1.003		V
			V_I = 12 V, I_O = 0 A		1.003		
	Line regulation		max I_O		±5		mV
	Load regulation		V_I = 5/12 V, 0-100 % of max I_O		±5		mV
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs Without Turbo Trans C_o =660 µF Type C		±160		mV
t_{tr}	Load transient recovery time				100		µs
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs With Turbo Trans C_o =3300 µF Type C; R_{TT} =SHORT		±45		mV
t_{tr}	Load transient recovery time				100		µs
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 5 V, 100 % of max I_O		8.4		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				22.1		ms
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 12 V, 100 % of max I_O		7.5		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				14.0		ms
t_f	V_I shut-down fall time. (From V_I off to 10 % of V_O)	V_I = 5 V	Max I_O		0.071		ms
			I_O = 0.1 A		23.9		ms
		V_I = 12 V	Max I_O		1.32		ms
			I_O = 0.1 A		96.6		ms
t_{RC} t_{Inh}	RC start-up time		V_I = 5 V , Max I_O		21.6		ms
			V_I = 12 V , Max I_O		12.4		ms
	RC shut-down fall time	V_I = 5 V	Max I_O		0.039		ms
			I_o = 0.1 A		26.5		ms

	(From RC off to 10 % of V_O)	V_I = 12 V	Max I_O	0.120		ms
			I_o = 0.1 A	23.1		ms
I_O	Output current			0	50	A
I_{lim}	Current limit threshold		T_{P1} < max T_{P1}	100		A
I_{sc}	Short circuit current		T_{P1} = 25ºC, see Note 3	110		A
C_{out}	Recommended Capacitive Load		T_{P1} = 25ºC, see Note 4	1000	10000	µF
V_{Oac}	Output ripple & noise V_I = 5 V		See ripple & noise section, max I_O	10		mVp-p
V_{Oac}	Output ripple & noise V_I = 12 V		See ripple & noise section, max I_O	10		mVp-p

Note 1: Frequency may be adjusted with SmartSync pin. See Operating Information section

Note 2: See Operating Information section for TurboTrans technology

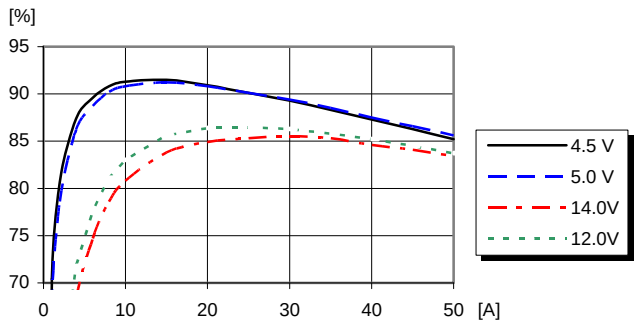
Note 3: Describe short circuit current characteristic, i.e. fold-back, hiccup or RMS, in one short sentence or type only “See Operating Information section.”)

Note 4: 1000 µF of external non-ceramic output capacitance is required for basic operation. Adding additional capacitance at the load further improves transient response. Up to 1000 µF of ceramic capacitance may be added in addition to the required non-ceramic capacitance. When not using TurboTrans technology, 8000 µF capacitance is allowed; When using TurboTrans technology, up to 10000 µF capacitance is allowed. For more information, see Operating Information Section.

1.0V, 50A / 50.0W Typical Characteristics

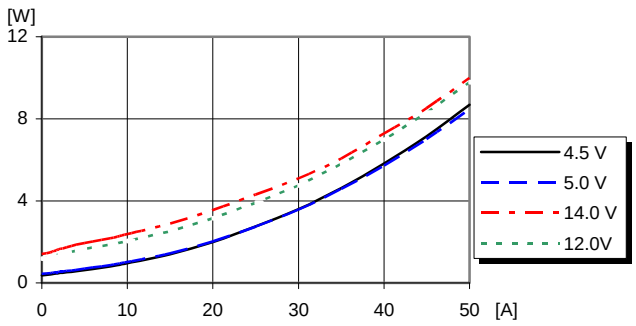
PMR 5118UW

Efficiency



Efficiency vs. load current and input voltage at T_{P1} = +25°C

Power Dissipation



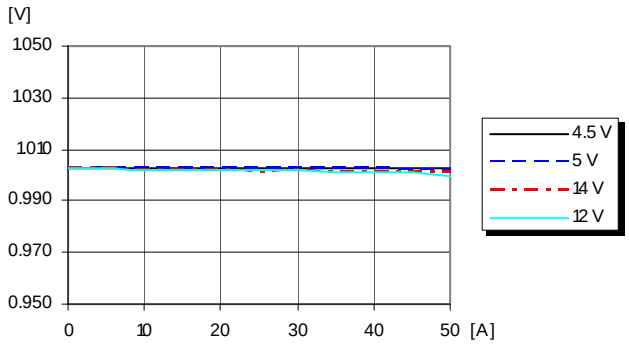
Dissipated power vs. load current and input voltage at T_{P1} = +25°C

Output Current Derating

TBD

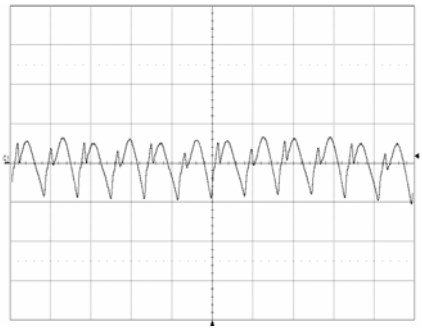
Output current derating information is available only for 1.2V and 3.3V output.

Output Characteristics



Output voltage vs. load current at T_{P1} = +25°C

Output Ripple & Noise



Output voltage ripple at:
T_{P1} = +25°C, V_I = 12 V,
I_O = 50 A resistive load.

Trace: output voltage 5 mV/div.
Time scale: 2 µs/div.

Output Voltage Adjust (see operating information)

Passive adjust
The resistor value for an adjusted output voltage is calculated by using the equations in the operating information.

$$R_{SET} = 30.1\,k\Omega \times \frac{0.7}{V_O - 0.7} - 6.49\,k\Omega$$

1.2V, 50A / 60.0W Electrical Specification — PMR 5118UW

T_{P1} = -40 to +85ºC, V_I = 4.5 to 14 V, R_{SET} = 35.7 kΩ, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25°C, V_I= 5/12 V, max I_O , unless otherwise specified under Conditions.
Additional C_{in} = 1000+22 µF and C_{out} = 660 µF. See Operating Information section for selection of capacitor types.
Connect the sense pin, where available, to the output pin.

Characteristics			Conditions	min	Typ	max	Unit
V_I	Input voltage range			4.5	5/12	14	V
V_{Ioff}	Turn-off input voltage		Decreasing input voltage	4.0	4.2		V
V_{Ion}	Turn-on input voltage		Increasing input voltage		4.3	4.45	V
C_I	Internal input capacitance				44		µF
P_O	Output power			0		50	W
η	Efficiency	V_I = 5 V	V_I = 5 V, 50 % of max I_O		91.5		%
			V_I = 5 V, max I_O		87.5		
		V_I = 12 V	V_I = 12 V, 50 % of max I_O		88.2		
			V_I = 12 V, max I_O		85.7		
P_d	Power Dissipation		V_I = 5 V, max I_O		8.6	9.0	W
			V_I = 12 V, max I_O		9.96	10.3	W
P_{Ii}	Input idling power		V_I = 5 V, I_O= 0 A		0.47		W
			V_I = 12 V, I_O= 0 A		1.21		W
P_{RC}	Input standby power		V_I = 5 V (turned off with RC)		42.4		mW
			V_I = 12 V (turned off with RC)		101.8		mW
I_S	Static Input current		V_I = 5 V, max I_O		13.71		A
			V_I = 12 V, max I_O		5.83		A
f_s	Switching frequency		0-100 % of max I_O		600		kHz
V_{Oi}	Output voltage initial setting and accuracy		T_{P1} = +25°C, V_I = 5/12 V, max I_O	1.188	1.200	1.212	V
V_O	Output voltage tolerance band		10-100 % of max I_O	1.182		1.218	V
	Idling voltage		V_I = 5 V, I_O = 0 A		1.201		V
			V_I = 12 V, I_O = 0 A		1.201		
	Line regulation		max I_O		±5		mV
	Load regulation		V_I = 5/12 V, 0-100 % of max I_O		±5		mV
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs Without Turbo Trans C_o =660 µF Type C		±160		mV
t_{tr}	Load transient recovery time				100		µs
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs With Turbo Trans C_o =3300 µF Type C; R_{TT} =SHORT		±45		mV
t_{tr}	Load transient recovery time				100		µs
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 5 V, 100 % of max I_O		8.6		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				21.3		ms
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 12 V, 100 % of max I_O		8.2		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				13.9		ms
t_f	V_I shut-down fall time. (From V_I off to 10 % of V_O)	V_I = 5 V	Max I_O		0.077		ms
			I_O = 0.1 A		29.5		ms
		V_I = 12 V	Max I_O		0.91		ms
			I_O = 0.1 A		99.4		ms
t_{RC} t_{Inh}	RC start-up time		V_I = 5 V , Max I_O		21.7		ms
			V_I = 12 V , Max I_O		12.4		ms
	RC shut-down fall time	V_I = 5 V	Max I_O		0.044		ms
			I_o = 0.1 A		28.4		ms

	(From RC off to 10 % of V_O)	V_I = 12 V	Max I_O	0.125		ms
			I_o = 0.1 A	28.1		ms
I_O	Output current			0	50	A
I_{lim}	Current limit threshold		T_{P1} < max T_{P1}	100		A
I_{sc}	Short circuit current		T_{P1} = 25ºC, see Note 3	110		A
C_{out}	Recommended Capacitive Load		T_{P1} = 25ºC, see Note 4	1000	10000	µF
V_{Oac}	Output ripple & noise V_I = 5 V		See ripple & noise section, max I_O	10		mVp-p
V_{Oac}	Output ripple & noise V_I = 12 V		See ripple & noise section, max I_O	10		mVp-p

Note 1: Frequency may be adjusted with SmartSync pin. See Operating Information section

Note 2: See Operating Information section for TurboTrans technology

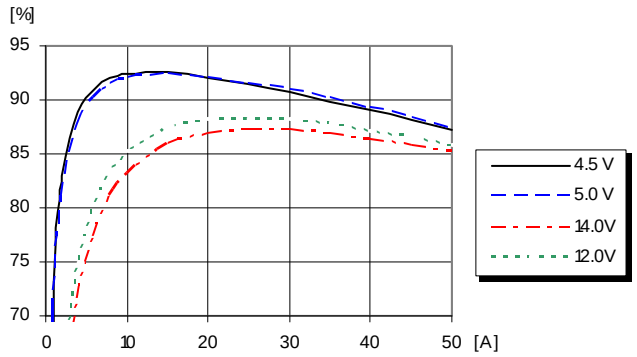
Note 3: Describe short circuit current characteristic, i.e. fold-back, hiccup or RMS, in one short sentence or type only “See Operating Information section.”)

Note 4: 1000 µF of external non-ceramic output capacitance is required for basic operation. Adding additional capacitance at the load further improves transient response. Up to 1000 µF of ceramic capacitance may be added in addition to the required non-ceramic capacitance. When not using TurboTrans technology, 8000 µF capacitance is allowed; When using TurboTrans technology, up to 10000 µF capacitance is allowed. For more information, see Operating Information Section.

1.2V, 50A / 60.0W Typical Characteristics

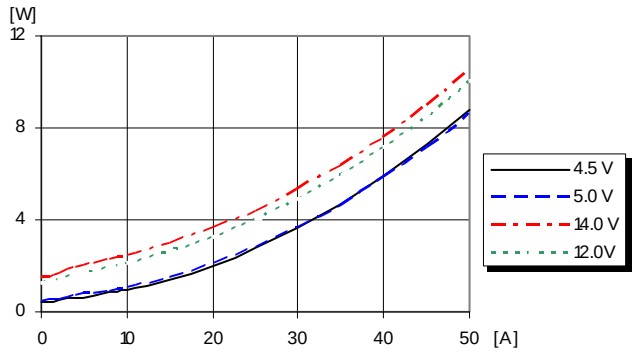
PMR 5118UW

Efficiency



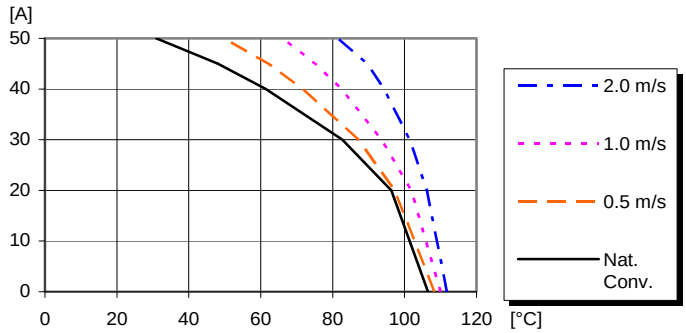
Efficiency vs. load current and input voltage at T_{P1} = +25°C

Power Dissipation



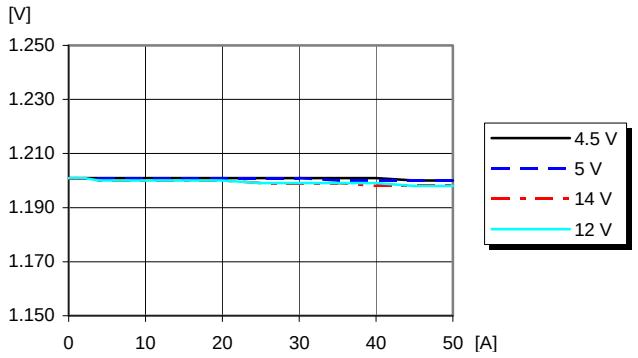
Dissipated power vs. load current and input voltage at T_{P1} = +25°C

Output Current Derating



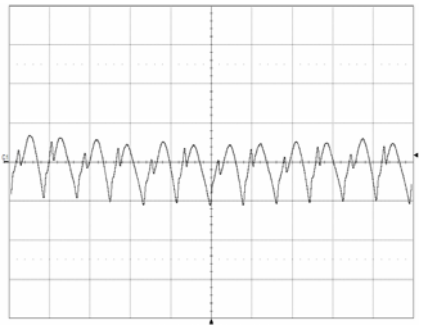
Available load current vs. ambient air temperature and airflow at V_I = 12 V. See Thermal Consideration section.

Output Characteristics



Output voltage vs. load current at T_{P1} = +25°C

Output Ripple & Noise



Output voltage ripple at:
T_{P1} = +25°C, V_I = 12 V,
I_O = 50 A resistive load.

Trace: output voltage 5 mV/div.
Time scale: 2 µs/div.

Output Voltage Adjust (see operating information)

Passive adjust
The resistor value for an adjusted output voltage is calculated by using the equations in the operating information.

$$R_{SET} = 30.1\,k\Omega \times \frac{0.7}{V_O - 0.7} - 6.49\,k\Omega$$

1.5V, 50A / 75.0W Electrical Specification — PMR 5118UW

T_{P1} = -40 to +85ºC, V_I = 4.5 to 14 V, R_{SET} = 19.6 kΩ, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25°C, V_I= 5/12 V, max I_O , unless otherwise specified under Conditions.
Additional C_{in} = 1000+22 µF and C_{out} = 660 µF. See Operating Information section for selection of capacitor types.
Connect the sense pin, where available, to the output pin.

Characteristics			Conditions	min	Typ	max	Unit
V_I	Input voltage range			4.5	5/12	14	V
V_{Ioff}	Turn-off input voltage		Decreasing input voltage	4.0	4.2		V
V_{Ion}	Turn-on input voltage		Increasing input voltage		4.3	4.45	V
C_I	Internal input capacitance				44		µF
P_O	Output power			0		50	W
η	Efficiency	V_I = 5 V	V_I = 5 V, 50 % of max I_O		92.8		%
			V_I = 5 V, max I_O		89.5		
		V_I = 12 V	V_I = 12 V, 50 % of max I_O		90.0		
			V_I = 12 V, max I_O		87.9		
P_d	Power Dissipation		V_I = 5 V, max I_O		8.81	8.95	W
			V_I = 12 V, max I_O		10.27	10.55	W
P_{Ii}	Input idling power		V_I = 5 V, I_O= 0 A		0.50		W
			V_I = 12 V, I_O= 0 A		1.26		W
P_{RC}	Input standby power		V_I = 5 V (turned off with RC)		42.4		mW
			V_I = 12 V (turned off with RC)		101.8		mW
I_S	Static Input current		V_I = 5 V, max I_O		16.76		A
			V_I = 12 V, max I_O		7.11		A
f_s	Switching frequency		0-100 % of max I_O		600		kHz
V_{Oi}	Output voltage initial setting and accuracy		T_{P1} = +25°C, V_I = 5/12 V, max I_O	1.485	1.500	1.515	V
V_O	Output voltage tolerance band		10-100 % of max I_O	1.477		1.523	V
	Idling voltage		V_I = 5 V, I_O = 0 A		1.498		V
			V_I = 12 V, I_O = 0 A		1.498		
	Line regulation		max I_O		±5		mV
	Load regulation		V_I = 5/12 V, 0-100 % of max I_O		±5		mV
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs Without Turbo Trans C_o =660 µF Type C		±160		mV
t_{tr}	Load transient recovery time				100		µs
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs With Turbo Trans C_o =3300 µF Type C; R_{TT} =SHORT		±45		mV
t_{tr}	Load transient recovery time				100		µs
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 5 V, 100 % of max I_O		8.5		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				21.0		ms
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 12 V, 100 % of max I_O		8.2		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				13.3		ms
t_f	V_I shut-down fall time. (From V_I off to 10 % of V_O)	V_I = 5 V	Max I_O		0.090		ms
			I_O = 0.1 A		37.2		ms
		V_I = 12 V	Max I_O		0.892		ms
			I_O = 0.1 A		94.3		ms
t_{RC} t_{Inh}	RC start-up time		V_I = 5 V , Max I_O		21.8		ms
			V_I = 12 V , Max I_O		12.2		ms
	RC shut-down	V_I = 5 V	Max I_O		0.063		ms

	fall time (From RC off to 10 % of V_O)	V_I = 12 V	I_o = 0.1 A		35.0	ms
			Max I_O		0.142	ms
			I_o = 0.1 A		34.7	ms
I_O	Output current			0	50	A
I_{lim}	Current limit threshold		T_{P1} < max T_{P1}		100	A
I_{sc}	Short circuit current		T_{P1} = 25ºC		110	A
C_{out}	Recommended Capacitive Load		T_{P1} = 25ºC, see Note 4	1000	10000	µF
V_{Oac}	Output ripple & noise V_I = 5 V		See ripple & noise section, max I_O		8	mVp-p
V_{Oac}	Output ripple & noise V_I = 12 V		See ripple & noise section, max I_O		10	mVp-p

Note 1: Frequency may be adjusted with SmartSync pin. See Operating Information section

Note 2: See Operating Information section for TurboTrans technology

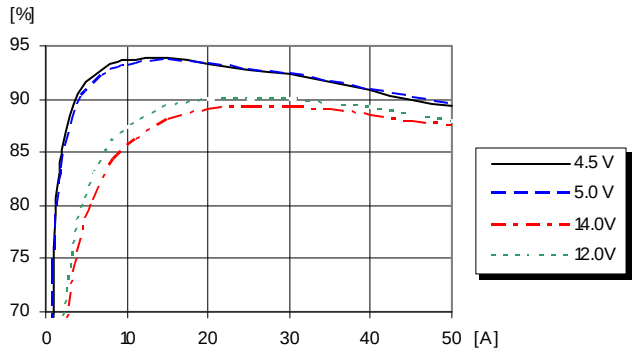
Note 3: Describe short circuit current characteristic, i.e. fold-back, hiccup or RMS, in one short sentence or type only “See Operating Information section.”)

Note 4: 1000 µF of external non-ceramic output capacitance is required for basic operation. Adding additional capacitance at the load further improves transient response. Up to 1000 µF of ceramic capacitance may be added in addition to the required non-ceramic capacitance. When not using TurboTrans technology, 8000 µF capacitance is allowed; When using TurboTrans technology, up to 10000 µF capacitance is allowed. For more information, see Operating Information Section.

1.5V, 50A / 75.0W Typical Characteristics

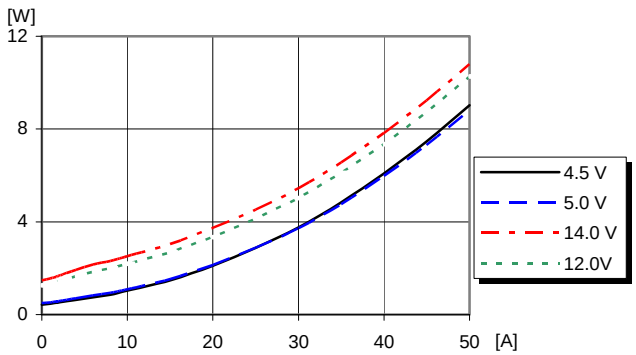
PMR 5118UW

Efficiency



Efficiency vs. load current and input voltage at T_{P1} = +25°C

Power Dissipation



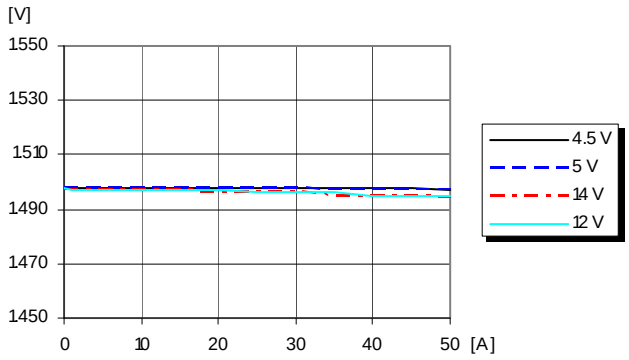
Dissipated power vs. load current and input voltage at T_{P1} = +25°C

Output Current Derating

TBD

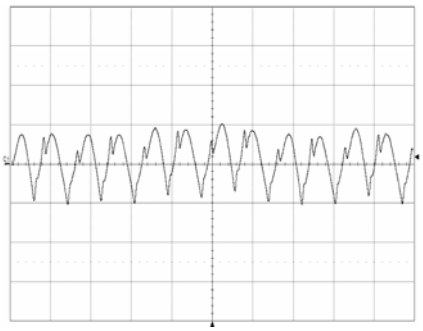
Output current derating information is available only for 1.2V and 3.3V output.

Output Characteristics



Output voltage vs. load current at T_{P1} = +25°C

Output Ripple & Noise



Output voltage ripple at:
T_{P1} = +25°C, V_I = 12 V,
I_O = 50 A resistive load.

Trace: output voltage 5 mV/div.
Time scale: 2 µs/div.

Output Voltage Adjust (see operating information)

Passive adjust
The resistor value for an adjusted output voltage is calculated by using the equations in the operating information.

$$R_{SET} = 30.1\,k\Omega \times \frac{0.7}{V_o - 0.7} - 6.49\,k\Omega$$

1.8V, 50A / 90.0W Electrical Specification — PMR 5118UW

T_{P1} = -40 to +85ºC, V_I = 4.5 to 14 V, R_{SET} = 12.7 kΩ, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25°C, V_I= 5/12 V, max I_O , unless otherwise specified under Conditions.
Additional C_{in} = 1000+22 µF and C_{out} = 660 µF. See Operating Information section for selection of capacitor types.
Connect the sense pin, where available, to the output pin.

Characteristics			Conditions	min	Typ	max	Unit
V_I	Input voltage range			4.5	5/12	14	V
V_{Ioff}	Turn-off input voltage		Decreasing input voltage	4.0	4.2		V
V_{Ion}	Turn-on input voltage		Increasing input voltage		4.3	4.45	V
C_I	Internal input capacitance				44		µF
P_O	Output power			0		50	W
η	Efficiency	V_I = 5 V	V_I = 5 V, 50 % of max I_O		93.8		%
			V_I = 5 V, max I_O		90.9		
		V_I = 12 V	V_I = 12 V, 50 % of max I_O		91.4		
			V_I = 12 V, max I_O		89.5		
P_d	Power Dissipation		V_I = 5 V, max I_O		9.00	9.25	W
			V_I = 12 V, max I_O		10.55	10.75	W
P_{li}	Input idling power		V_I = 5 V, I_O= 0 A		0.53		W
			V_I = 12 V, I_O= 0 A		1.33		W
P_{RC}	Input standby power		V_I = 5 V (turned off with RC)		42.4		mW
			V_I = 12 V (turned off with RC)		101.8		mW
I_S	Static Input current		V_I = 5 V, max I_O		19.80		A
			V_I = 12 V, max I_O		7.45		A
f_s	Switching frequency		0-100 % of max I_O		600		kHz
V_{Oi}	Output voltage initial setting and accuracy		T_{P1} = +25°C, V_I = 5/12 V, max I_O	1.782	1.800	1.818	V
V_O	Output voltage tolerance band		10-100 % of max I_O	1.773		1.827	V
	Idling voltage		V_I = 5 V, I_O = 0 A		1.802		V
			V_I = 12 V, I_O = 0 A		1.802		
	Line regulation		max I_O		±5		mV
	Load regulation		V_I = 5/12 V, 0-100 % of max I_O		±5		mV
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs Without Turbo Trans C_o =660 µF Type C		±160		mV
t_{tr}	Load transient recovery time				100		µs
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs With Turbo Trans C_o =3300 µF Type C; R_{TT} =SHORT		±45		mV
t_{tr}	Load transient recovery time				100		µs
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 5 V, 100 % of max I_O		8.5		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				21.0		ms
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 12 V, 100 % of max I_O		8.3		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				13.4		ms
t_f	V_I shut-down fall time. (From V_I off to 10 % of V_O)	V_I = 5 V	Max I_O		0.073		ms
			I_O = 0.1 A		44.1		ms
		V_I = 12 V	Max I_O		0.627		ms
			I_O = 0.1 A		95.1		ms
t_{RC} t_{Inh}	RC start-up time		V_I = 5 V , Max I_O		22.0		ms
			V_I = 12 V , Max I_O		12.3		ms
	RC shut-down fall time	V_I = 5 V	Max I_O		0.060		ms
			I_o = 0.1 A		41.8		ms

	(From RC off to 10 % of V_O)	V_I = 12 V	Max I_O	0.143		ms
			I_o = 0.1 A	42.2		ms
I_O	Output current			0	50	A
I_{lim}	Current limit threshold		T_{P1} < max T_{P1}	100		A
I_{sc}	Short circuit current		T_{P1} = 25ºC, see Note 3	110		A
C_{out}	Recommended Capacitive Load		T_{P1} = 25ºC, see Note 4	1000	10000	µF
V_{Oac}	Output ripple & noise V_I = 5 V		See ripple & noise section, max I_O	8		mVp-p
V_{Oac}	Output ripple & noise V_I = 12 V		See ripple & noise section, max I_O	12		mVp-p

Note 1: Frequency may be adjusted with SmartSync pin. See Operating Information section

Note 2: See Operating Information section for TurboTrans technology

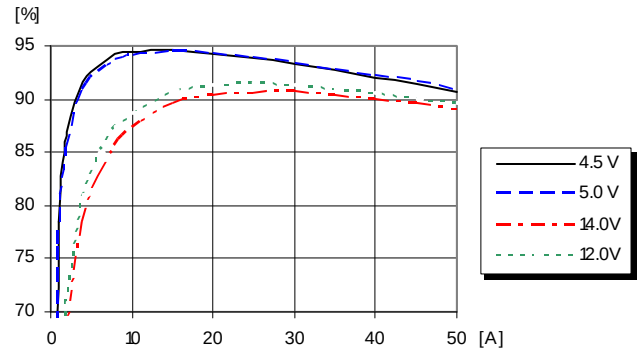
Note 3: Describe short circuit current characteristic, i.e. fold-back, hiccup or RMS, in one short sentence or type only “See Operating Information section.”)

Note 4: 1000 µF of external non-ceramic output capacitance is required for basic operation. Adding additional capacitance at the load further improves transient response. Up to 1000 µF of ceramic capacitance may be added in addition to the required non-ceramic capacitance. When not using TurboTrans technology, 8000 µF capacitance is allowed; When using TurboTrans technology, up to 10000 µF capacitance is allowed. For more information, see Operating Information Section.

1.8V, 50A / 90.0W Typical Characteristics

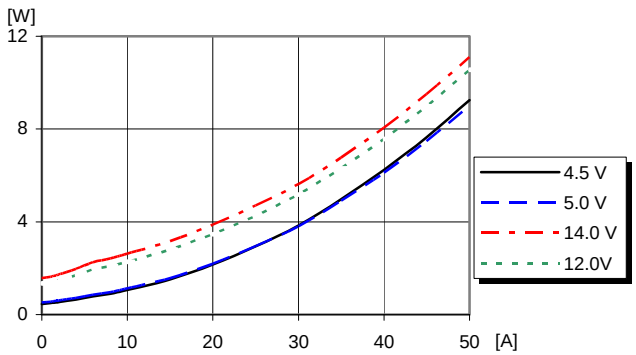
PMR 5118UW

Efficiency



Efficiency vs. load current and input voltage at T_{P1} = +25°C

Power Dissipation



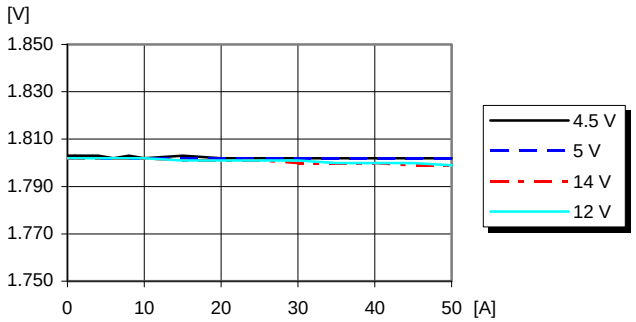
Dissipated power vs. load current and input voltage at T_{P1} = +25°C

Output Current Derating

TBD

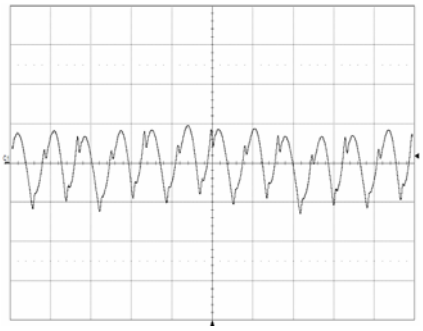
Output current derating information is available only for 1.2V and 3.3V output.

Output Characteristics



Output voltage vs. load current at T_{P1} = +25°C

Output Ripple & Noise



Output voltage ripple at:
T_{P1} = +25°C, V_I = 12 V,
I_O = 50 A resistive load.

Trace: output voltage 5 mV/div.
Time scale: 2 µs/div.

Output Voltage Adjust (see operating information)

Passive adjust
The resistor value for an adjusted output voltage is calculated by using the equations in the operating information.

$$R_{SET} = 30.1\,k\Omega \times \frac{0.7}{V_O - 0.7} - 6.49\,k\Omega$$

2.5V, 50A / 125.0W Electrical Specification — PMR 5118UW

T_{ref} = -40 to +85ºC, V_I = 4.5 to 14 V, R_{SET} = 5.23 kΩ, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25°C, V_I= 5/12 V, max I_O , unless otherwise specified under Conditions.
Additional C_{in} = 1000+22 µF and C_{out} = 660 µF. See Operating Information section for selection of capacitor types.
Connect the sense pin, where available, to the output pin.

Characteristics			Conditions	min	Typ	max	Unit
V_I	Input voltage range			4.5	5/12	14	V
V_{Ioff}	Turn-off input voltage		Decreasing input voltage	4.0	4.2		V
V_{Ion}	Turn-on input voltage		Increasing input voltage		4.3	4.45	V
C_I	Internal input capacitance				44		µF
P_O	Output power			0		50	W
η	Efficiency	V_I = 5 V	V_I = 5 V, 50 % of max I_O		95.3		%
			V_I = 5 V, max I_O		93.0		
		V_I = 12 V	V_I = 12 V, 50 % of max I_O		93.2		
			V_I = 12 V, max I_O		91.8		
P_d	Power Dissipation		V_I = 5 V, max I_O		9.46	9.75	W
			V_I = 12 V, max I_O		11.3	11.62	W
P_{Ii}	Input idling power		V_I = 5 V, I_O= 0 A		0.56		W
			V_I = 12 V, I_O= 0 A		1.57		W
P_{RC}	Input standby power		V_I = 5 V (turned off with RC)		47.1		mW
			V_I = 12 V (turned off with RC)		109.3		mW
I_S	Static Input current		V_I = 5 V, max I_O		26.88		A
			V_I = 12 V, max I_O		11.35		A
f_s	Switching frequency		0-100 % of max I_O		600		kHz
V_{Oi}	Output voltage initial setting and accuracy		T_{P1} = +25°C, V_I = 5/12 V, max I_O	2.475	2.500	2.525	V
V_O	Output voltage tolerance band		10-100 % of max I_O	2.462		2.538	V
	Idling voltage		V_I = 5 V, I_O = 0 A		2.500		V
			V_I = 12 V, I_O = 0 A		2.500		
	Line regulation		max I_O		±5		mV
	Load regulation		V_I = 5/12 V, 0-100 % of max I_O		±5		mV
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs Without Turbo Trans C_o =660 µF Type C		±160		mV
t_{tr}	Load transient recovery time				100		µs
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs With Turbo Trans C_o =3300 µF Type C; R_{TT} =SHORT		±45		mV
t_{tr}	Load transient recovery time				100		µs
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 5 V, 100 % of max I_O		8.7		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				19.2		ms
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 12 V, 100 % of max I_O		8.5		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				13.0		ms
t_f	V_I shut-down fall time. (From V_I off to 10 % of V_O)	V_I = 5 V	Max I_O		0.139		ms
			I_O = 0.1 A		70.8		ms
		V_I = 12 V	Max I_O		0.587		ms
			I_O = 0.1 A		102.4		ms
t_{RC} t_{Inh}	RC start-up time		V_I = 5 V , Max I_O		21.4		ms
			V_I = 12 V , Max I_O		12.7		ms
	RC shut-down	V_I = 5 V	Max I_O		0.115		ms

	fall time (From RC off to 10 % of V_O)	V_I = 12 V	I_o = 0.1 A		60.3	ms
			Max I_O		0.196	ms
			I_o = 0.1 A		61.6	ms
I_O	Output current			0	50	A
I_{lim}	Current limit threshold		T_{P1} < max T_{P1}		100	A
I_{sc}	Short circuit current		T_{P1} = 25ºC, see Note 3		110	A
C_{out}	Recommended Capacitive Load		T_{P1} = 25ºC, see Note 4	1000	10000	µF
V_{Oac}	Output ripple & noise V_I = 5 V		See ripple & noise section, max I_O		7	mVp-p
V_{Oac}	Output ripple & noise V_I = 12 V		See ripple & noise section, max I_O		12	mVp-p

Note 1: Frequency may be adjusted with SmartSync pin. See Operating Information section

Note 2: See Operating Information section for TurboTrans technology

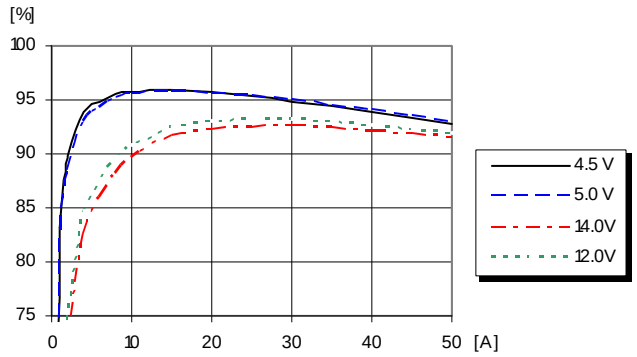
Note 3: Describe short circuit current characteristic, i.e. fold-back, hiccup or RMS, in one short sentence or type only “See Operating Information section.”)

Note 4: 1000 µF of external non-ceramic output capacitance is required for basic operation. Adding additional capacitance at the load further improves transient response. Up to 1000 µF of ceramic capacitance may be added in addition to the required non-ceramic capacitance. When not using TurboTrans technology, 8000 µF capacitance is allowed; When using TurboTrans technology, up to 10000 µF capacitance is allowed. For more information, see Operating Information Section.

2.5V, 50A / 125.0W Typical Characteristics

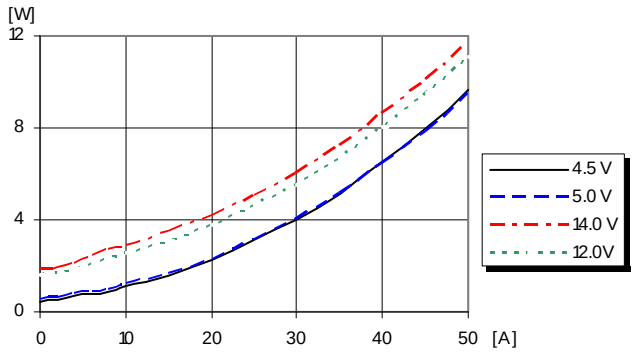
PMR 5118UW

Efficiency



Efficiency vs. load current and input voltage at T_{P1} = +25°C

Power Dissipation



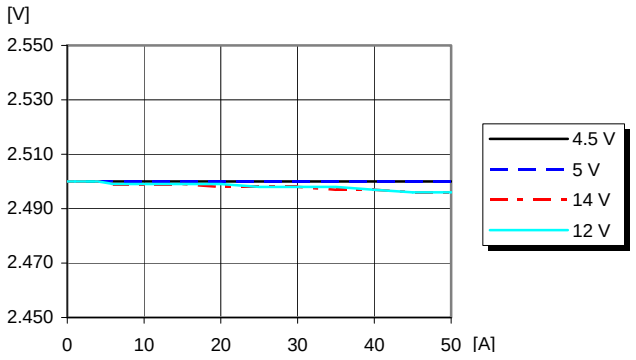
Dissipated power vs. load current and input voltage at T_{P1} = +25°C

Output Current Derating

TBD

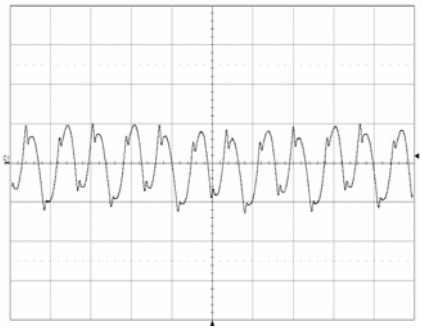
Output current derating information is available only for 1.2V and 3.3V output.

Output Characteristics



Output voltage vs. load current at T_{P1} = +25°C

Output Ripple & Noise



Output voltage ripple at:
T_{P1} = +25°C, V_I = 12 V,
I_O = 50 A resistive load.

Trace: output voltage 5 mV/div.
Time scale: 2 µs/div.

Output Voltage Adjust (see operating information)

Passive adjust
The resistor value for an adjusted output voltage is calculated by using the equations in the operating information.

$$R_{SET} = 30.1\,k\Omega \times \frac{0.7}{V_o - 0.7} - 6.49\,k\Omega$$

3.3V, 50A / 165.0W Electrical Specification — PMR 5118UW

T_{P1} = -40 to +85ºC, V_I = 4.5 to 14 V, R_{SET} = 1.62 kΩ, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25°C, V_I= 5/12 V, max I_O , unless otherwise specified under Conditions.
Additional C_{in} = 1000+22 µF and C_{out} = 660 µF. See Operating Information section for selection of capacitor types.
Connect the sense pin, where available, to the output pin.

Characteristics			Conditions	min	Typ	max	Unit
V_I	Input voltage range			4.5	5/12	14	V
V_{Ioff}	Turn-off input voltage		Decreasing input voltage	4.0	4.2		V
V_{Ion}	Turn-on input voltage		Increasing input voltage		4.3	4.45	V
C_I	Internal input capacitance				44		µF
P_O	Output power			0		50	W
η	Efficiency	V_I = 5 V	V_I = 5 V, 50 % of max I_O		96.3		%
			V_I = 5 V, max I_O		94.4		
		V_I = 12 V	V_I = 12 V, 50 % of max I_O		94.4		
			V_I = 12 V, max I_O		93.4		
P_d	Power Dissipation		V_I = 5 V, max I_O		9.80	10.2	W
			V_I = 12 V, max I_O		11.57	11.8	W
P_{Ii}	Input idling power		V_I = 5 V, I_O= 0 A		0.51		W
			V_I = 12 V, I_O= 0 A		1.86		W
P_{RC}	Input standby power		V_I = 5 V (turned off with RC)		42.4		mW
			V_I = 12 V (turned off with RC)		94.3		mW
I_S	Static Input current		V_I = 5 V, max I_O		34.96		A
			V_I = 12 V, max I_O		14.72		A
f_s	Switching frequency		0-100 % of max I_O		600		kHz
V_{Oi}	Output voltage initial setting and accuracy		T_{P1} = +25°C, V_I = 5/12 V, max I_O	3.267	3.300	3.333	V
V_O	Output voltage tolerance band		10-100 % of max I_O	3.250		3.350	V
	Idling voltage		V_I = 5 V, I_O = 0 A		3.299		V
			V_I = 12 V, I_O = 0 A		3.299		
	Line regulation		max I_O		±5		mV
	Load regulation		V_I = 5/12 V, 0-100 % of max I_O		±5		mV
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs Without Turbo Trans C_o =TBD µF Type C		±160		mV
t_{tr}	Load transient recovery time				100		µs
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2.5 A/µs With Turbo Trans C_o =TBD µF Type C; R_{TT} =TBD kΩ		±45		mV
t_{tr}	Load transient recovery time				100		µs
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 5 V, 100 % of max I_O		8.7		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				17.7		ms
t_r	Ramp-up time (from 10−90 % of V_{Oi})		V_I = 12 V, 100 % of max I_O		8.7		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})				13.1		ms
t_f	V_I shut-down fall time. (From V_I off to 10 % of V_O)	V_I = 5 V	Max I_O		0.141		ms
			I_O = 0.1 A		81.2		ms
		V_I = 12 V	Max I_O		0.414		ms
			I_O = 0.1 A		124.1		ms
t_{RC} t_{Inh}	RC start-up time		V_I = 5 V , Max I_O		21.8		ms
			V_I = 12 V , Max I_O		12.1		ms
	RC shut-down	V_I = 5 V	Max I_O		0.126		ms

	fall time (From RC off to 10 % of V_O)	V_I = 12 V	I_o = 0.1 A		81.8	ms
			Max I_O		0.206	ms
			I_o = 0.1 A		79.3	ms
I_O	Output current			0	50	A
I_{lim}	Current limit threshold		T_{P1} < max T_{P1}		100	A
I_{sc}	Short circuit current		T_{P1} = 25ºC, see Note 3		110	A
C_{out}	Recommended Capacitive Load		T_{P1} = 25ºC, see Note 4	1000	10000	µF
V_{Oac}	Output ripple & noise V_I = 5 V		See ripple & noise section, max I_O		7	mVp-p
V_{Oac}	Output ripple & noise V_I = 12 V		See ripple & noise section, max I_O		12	mVp-p

Note 1: Frequency may be adjusted with SmartSync pin. See Operating Information section

Note 2: See Operating Information section for TurboTrans technology

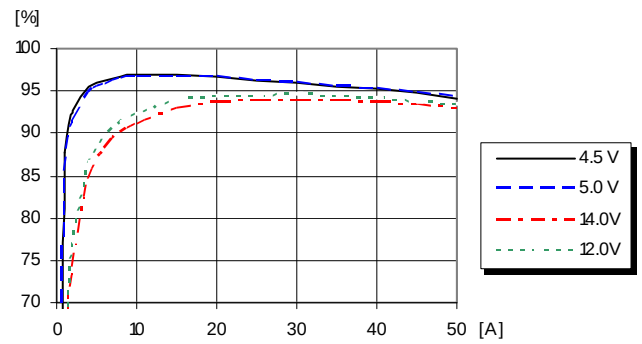
Note 3: Describe short circuit current characteristic, i.e. fold-back, hiccup or RMS, in one short sentence or type only “See Operating Information section.”)

Note 4: 1000 µF of external non-ceramic output capacitance is required for basic operation. Adding additional capacitance at the load further improves transient response. Up to 1000 µF of ceramic capacitance may be added in addition to the required non-ceramic capacitance. When not using TurboTrans technology, 8000 µF capacitance is allowed; When using TurboTrans technology, up to 10000 µF capacitance is allowed. For more information, see Operating Information Section.

3.3V, 50A / 165.0W Typical Characteristics

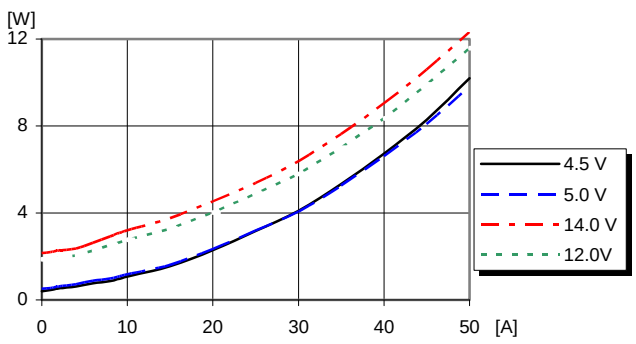
PMR 5118UW

Efficiency



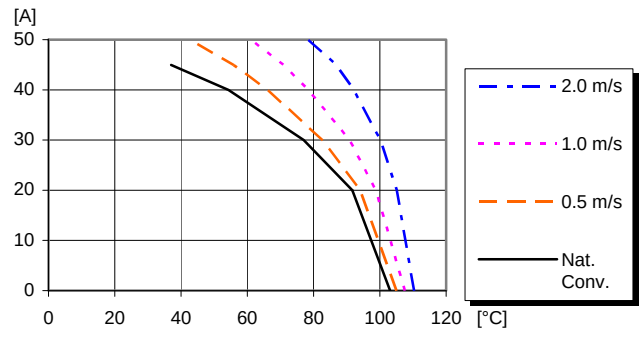
Efficiency vs. load current and input voltage at T_{P1} = +25°C

Power Dissipation



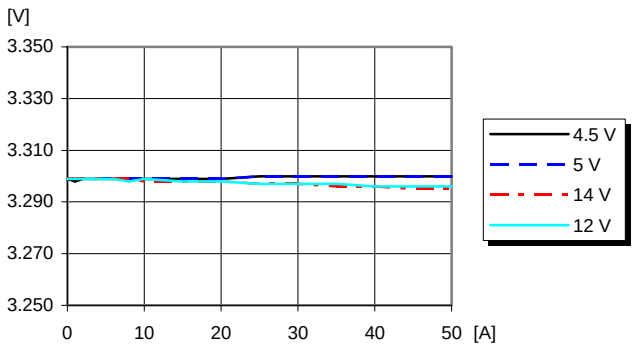
Dissipated power vs. load current and input voltage at T_{P1} = +25°C

Output Current Derating



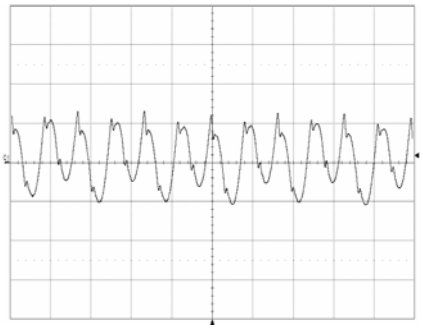
Available load current vs. ambient air temperature and airflow at V_I = 12 V. See Thermal Consideration section.

Output Characteristics



Output voltage vs. load current at T_{P1} = +25°C

Output Ripple & Noise



Output voltage ripple at:
T_{P1} = +25°C, V_I = 12 V,
I_O = 50 A resistive load.

Trace: output voltage 5 mV/div.
Time scale: 2 µs/div.

Output Voltage Adjust (see operating information)

Passive adjust
The resistor value for an adjusted output voltage is calculated by using the equations in the operating information.

$$R_{SET} = 30.1\,k\Omega \times \frac{0.7}{V_O - 0.7} - 6.49\,k\Omega$$

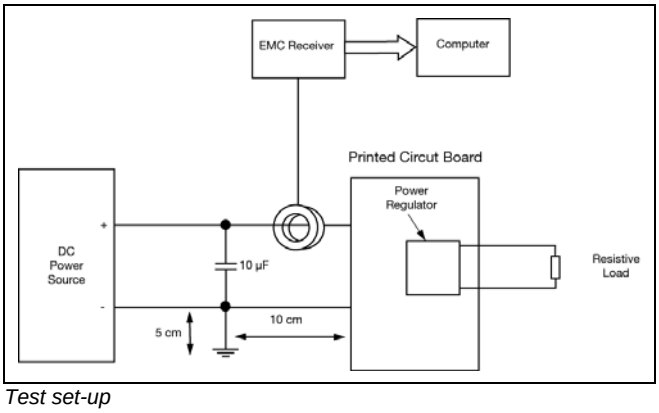
EMC Specification

Conducted EMI measured according to test set-up.
The fundamental switching frequency is 600 kHz for PMR 5118UW@ V_I = 12 V, max I_O.

Conducted EMI Input terminal value (typ)

TBD

EMI without filter



Test set-up

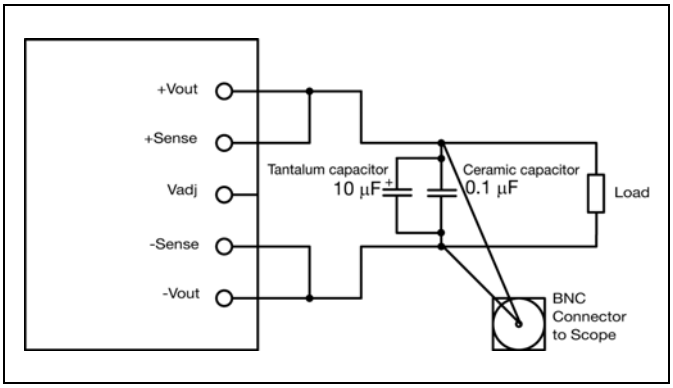
Layout recommendations

The radiated EMI performance of the product will depend on the PCB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.

A ground layer will increase the stray capacitance in the PCB and improve the high frequency EMC performance.

Output ripple and noise

Output ripple and noise measured according to figure below. See Design Note 022 for detailed information.



Output ripple and noise test setup

Operating information

Extended information for POLA products is found in Application Note 205.

Input Voltage

The input voltage range 4.5 to 14 Vdc makes the product easy to use in intermediate bus applications when powered by a non-regulated bus converter or a regulated bus converter.

Turn-off Input Voltage

The products monitor the input voltage and will turn on and turn off at predetermined levels.

The typical hysteresis between turn on and turn off input voltage is 0.1V.

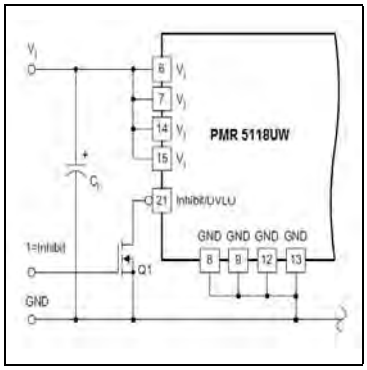
Turn on/off voltage can be adjusted by using UVLO (Undervoltage lockout) function. The UVLO character is defined by the ON threshold (V_{THD}) voltage. Below the ON threshold, the Inhibit control is overridden, and the module does not produce an output.

The UVLO feature allows for limited adjustment of the ON threshold voltage. It is made by using a single resistor between the Inhibit/UVLO pin (pin 21) and ground pins (pin 8,9,12,13). The V_{THD} value can be adjusted from 5.5V to 11V. Default value of V_{THD} is 4.3V.

Below equation determines the value of resistor required to adjust V_{THD} to a new value.

$$R_{UVLO} = \frac{230}{V_{THD} - 4.6} (k\Omega)$$

Inhibit Control



The products are fitted with a remote control function by using the Inhibit/UVLO pin. The Inhibit control function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch. The RC pin has an internal pull up. An external pull-up resistor should never be used with the inhibit pin.

When the Inhibit pin is left open, the regulator will turn on when the input voltage is applied. Turn off is achieved by connecting the Inhibit pin to the GND.

The reference figure above shows the typical application of the inhibit function. The input is not compatible with TTL logic device. An open-collector (or open-drain) discrete transistor is recommended for control. Turning the discrete transistor on applies a low voltage to the Inhibit control pin and disables the output of the module. If this device is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 20 ms.

External Decoupling Capacitors

Input capacitors:

The PMR 5118UW requires a minimum input capacitance of e 1000 µF. The ripple current rating of the input capacitor must be at least 600 mA rms. An optional 22 µF X5R/X7R ceramic capacitor is recommended to reduce RMS ripple current.

The size and value of the input capacitor is determined by the converter's transient performance capability. This minimum value assumes that the converter is supplied with a responsive, low inductance input source. This source should have ample capacitive decoupling, and be distributed to the converter via PCB power and ground planes.

Ceramic capacitors should be located as close as possible to the module's input pins, within 0.5 inch (1,3 cm). Adding ceramic capacitance is necessary to reduce the high-frequency ripple voltage at the module's input. This reduces the magnitude of the ripple current through the electrolytic capacitor, as well as the amount of ripple current reflected back to the input source. Additional ceramic capacitors can be added to further reduce the RMS ripple current requirement for the electrolytic capacitor.

The main considerations when selecting input capacitors are the RMS ripple current rating, temperature stability, and less than 100 mΩ of equivalent series resistance (ESR).

Regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of 2× (maximum dc voltage + ac ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with a sufficient voltage rating to meet this requirement.

Output capacitors:

The PMR 5118UW module requires a minimum output capacitance of 660µF of polymer-aluminum, tantulum, or polymer-tantalum type.

The required capacitance above the minimum is determined by actual transient deviation requirements. See "TurboTrans Technology" information below.

For both input and output capacitors, when the operating temperature is below 0°C, the ESR of aluminium electrolytic capacitors increases. For these applications, OS-CON, poly-aluminium, and polymer-tantalum types should be considered.

If the TurboTrans feature is not used, minimum ESR and maximum capacitor limits must be followed. System stability may be effected and increased output capacitance may be required without TurboTrans.

When using the PMR 5118UW, observe the minimum ESR of the entire output capacitor bank. The minimum ESR limit of the output capacitor bank is 7mΩ.

When using PMR 5118UW without the TurboTrans feature, the maximum amount of capacitance is 1000 µF of ceramic type. Large amounts of capacitance may reduce system stability.

Utilizing the TurboTrans feature improves system stability, improves transient response, and reduces the amount of output capacitance required to meet system transient design requirements. For detaile information, see "TurboTrans Technology" information below.

Output Voltage Adjust (V_{adj})

The product has an Output Voltage Adjust function. The function can be used to adjust the output voltage in the range from 0.7V to 3.6V.

The Vo Adjust control sets the output voltage of the PMR 5118UW. The adjustment method requires the addition of a single external resistor, RSET, that must be connected directly between pins Vo Adjust (pin 18) and AGND (pin 4). The value of the required resistor can be calculated using the following formula.

$$R_{SET} = 30.1(k\Omega) \times \frac{0.7}{V_O - 0.7} - 6.49(k\Omega)$$

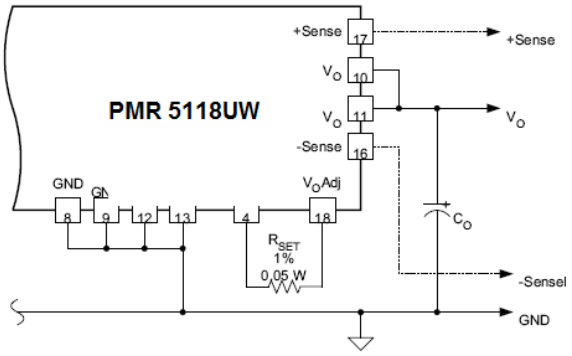
Note:

(1) R_{SET} : Use a 0.05 W resistor with a tolerance of 1% and temperature stability of 100 ppm/°C (or better). Connect the

resistor directly between pins 18 and 4, as close to the regulator as possible, using dedicated PCB traces.

(2) Never connect capacitors from Vo Adjust to either + Sense, GND, or Vo. Any capacitance added to the Vo Adjust pin affects the stability of the regulator.

(3) For output voltages less than 1.2 V, the output ripple may increase (up to 2×) when operating at input voltages greater than (Vo×12). Adjusting the switching frequency using the SmartSync feature may increase or decrease this ratio.

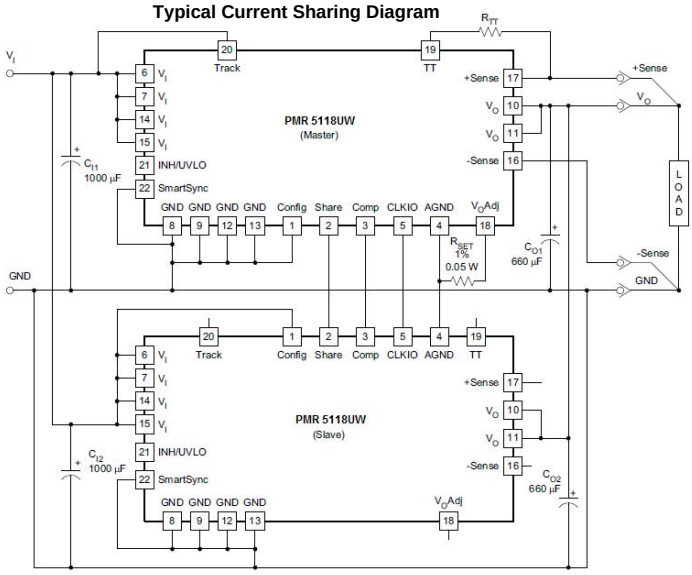


Parallel Operation

The PMR 5818UW module is capable of being configured in parallel with another PMR 5118UW module to share load current. To parallel the two modules, it is necessary to configure one module as the Master and one module as the Slave. To configure a module as the Master, connect the CONFIG pin (pin 1) to GND. The CONFIG pin of the Slave must be connected to V_I. In order to share current, pins 2 through 5 of both the Master and Slave must be connected between the two modules. The module that is configured as the MASTER is used to control all of the functions of the two modules including Inhibit, ON/OFF control, AutoTrack sequencing, TurboTrans, SmartSync, +/- Remote Sense, and Output Voltage Adjust. The MASTER and the SLAVE must be powered from the same input voltage supply.

When using TurboTrans while paralleling two modules, the TurboTrans resistor, R_{TT}, must be connected from the TurboTrans pin (pin 19) of the Master module to the +Sense pin (pin 17) of the Master module. When paralleling modules the procedure to calculate the proper value of output capacitance and R_{TT} is similar to that explained in the TurboTrans Selection section, however the values must be calculated for a single module. Therefore, the total output current load step must be halved before determining the required output capacitance and the R_{TT} value as explained in the TurboTrans Selection section. The value of output capacitance calculated is the minimum required output capacitance per module and the value of RTT must be calculated using this value of output capacitance. The TurboTrans pin of the Slave module must be left open.

Typical Current Sharing Diagram

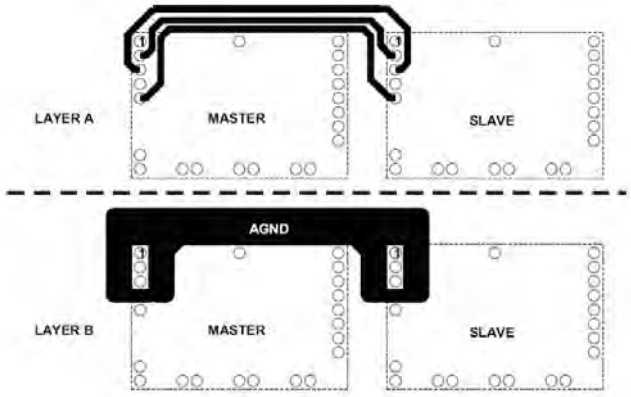


Required Connections for Current Sharing

TERMINAL		MASTER	SLAVE
NAME	NO.		
V_I	6,7,14,15	Connect to the Input Bus.	Connect to the Input Bus.
V_O	10,11	Connect to the Output Bus.	Connect to the Output Bus.
GND	8,9,12,13	Connect to Common Power GND.	Connect to Common Power GND.
Inhibit and UVLO	21	Use for Inhibit control & UVLO adjustments. If unused leave open-circuit.	No Connection. Leave open-circuit.
V_o Adjust	18	Use to set the output voltage. Connect R_{SET} resistor between this pin and AGND (pin 4).	No Connection. Leave open-circuit.
+Sense	17	Connect to the output voltage either at the load or at the module (pin 11).	No Connection. Leave open-circuit.
–Sense	16	Connect to the output GND either at the load or at the module (pin 13).	No Connection. Leave open-circuit.
Track	20	Connect to Track control or to V_I (pin 15).	No Connection. Leave open-circuit.
TurboTrans™	19	Connect TurboTrans resistor, R_{TT}, between this pin and +Sense (pin 17).	No Connection. Leave open-circuit.
SmartSync	22	Connect to an external clock. If unused connect to GND.	Connect to Common Power GND.
CONFIG	1	Connect to GND.	Connect to the Input Bus.
Share	2	Connect to pin 2 of Slave.	Connect to pin 2 of Master.
Comp	3	Connect to pin 3 of Slave.	Connect to pin 3 of Master.
AGND	4	Connect to pin 4 of Slave.	Connect to pin 4 of Master.
CLKIO	5	Connect to pin 5 of Slave.	Connect to pin 5 of Master.

Current sharing layout

In current sharing applications the V_I pins of both modules must be connected to the same input bus. The V_O pins of both modules are connected together to power the load. The GND pins of both modules are connected via the GND plane. Four other inter-connection pins are connected between the modules. Below figure shows the required layout of the inter-connection pins for two modules configured to share current. Notice that the Share (pin 2) connection is routed between the Comp (pin 3) and CLKIO (pin 5) connections. AGND (pin 4) should be connected as a thicker trace on an adjacent layer, running parallel to pins 2, 3 and 5. AGND must not be connected to the GND plane.



Remote Sense

The products have remote sense that can be used to compensate for voltage drops between the output and the point of load. The sense traces should be located close to the PCB ground layer to reduce noise susceptibility. The remote sense circuitry will compensate for up to 0.3 voltage drop between output pins and the point of load.
If the remote sense is not needed +Sense should be connected to +Out and -Sense should be connected to -Out.

Over Temperature Protection (OTP)

The regulators are protected from thermal overload by an internal over temperature shutdown circuit. If the internal temperature exceeds the OTP threshold, the module's inhibit control is internally pulled low. This turns the output off. The voltage drops as the external output capacitors are discharged by the load circuit. The product will make continuous attempts to start up (non-latching mode) and resume normal operation automatically when the temperature has dropped >10°C below the temperature threshold.

Over Current Protection (OCP)

The regulators include current limiting circuitry for protection at continuous overload. The output voltage will decrease towards zero for output currents in excess of max output current (max I_O). The regulator will resume normal operation after removal of the overload. The load distribution should be designed for the maximum output short circuit current specified.

Soft-start Power Up

From the moment a valid input voltage is applied, the soft-start control introduces a short time-delay (typically 5-15 ms) before allowing the output voltage to rise. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors.

Auto-Track™ Function

Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each unit power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, micro-processors and ASICs.

Notes on Use of Auto-Track™

1. The Track pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the Track pin is the input voltage V_I.
4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 20 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the Track pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the Track pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises according to its softstart rate after input power has been applied.
6. The Auto-Track pin should never be used to regulate the module's output voltage for long-term, steady-state operation.

Smart Sync

Smart Sync is a feature that allows multiple power modules to be synchronized to a common frequency. When not used, this pin must be connect to GND. Driving the Smart Sync pins with an external oscillator set to the desired frequency, synchronizes all connected modules to the selected requency. The synchronization frequency can be higher or lower than the nominal switching frequency of the modules within the range of 240 kHz to 400 kHz.

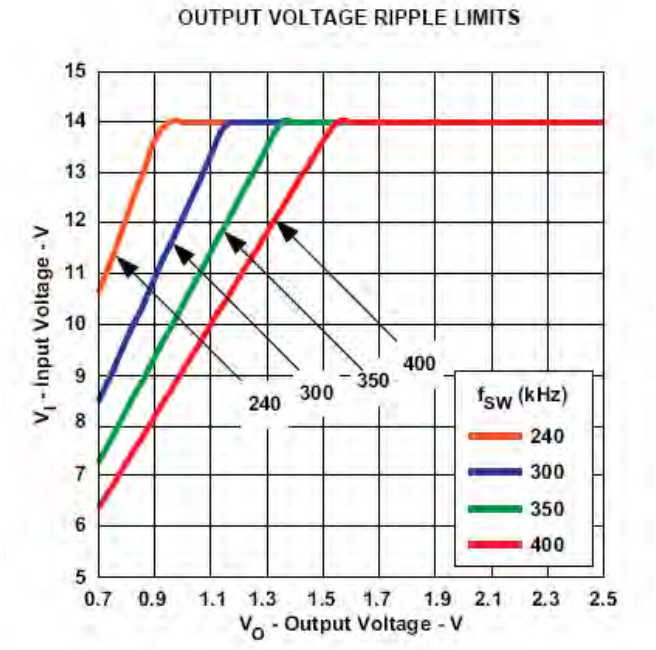
Synchronizing modules powered from the same bus eliminates beat frequencies reflected back to the input supply, and also reduces EMI filtering requirements. Eliminating the low beat frequencies (usually<10kHz) allows the EMI filter to be designed to attenuate only the synchronization frequency. Power modules can also be synchronized out of phase to minimize ripple current and reduce input capacitance requirements.

The PMR 5118UW requires that the external synchronization frequency be present before a valid input voltage is present or before release of the inhibit control.

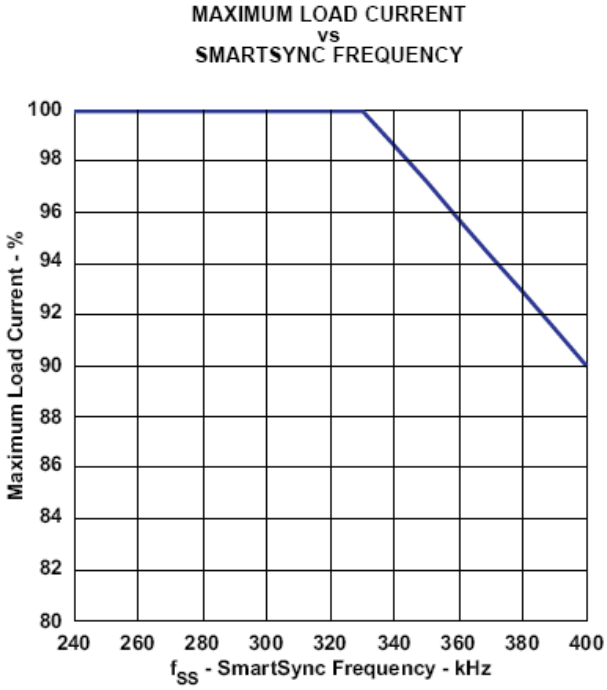
Operating the PMR 5118UW with a low duty cycle may increase the output voltage ripple. When operating at the nominal switching frequency, input voltages greater than (V_O ×12) may cause the output voltage ripple to increase (up to 2×).

When using Smart Sync, the minimum duty cycle varies as a function of output voltage and switching frequency. Synchronizing to a higher frequency causes greater restrictions on the duty cycle range. For a given switching frequency, below figure shows the operating region where the output voltage ripple meets the electrical specifications.

Operation above a given curve may cause the output voltage ripple to increase (up to 2×).



The maximum output current that a single module can deliver may also be affected by the sychronization frequency. See Figure below for load current derating when sychronizing at frequencies greater than 330 kHz. First consult the temperature derating graphs in the Typical Characteristics section to determine the maximum output current based on operating conditions. Any derating due to the SmartSync frequency is in addition to the temperature derating.



Pre-Bias Startup Capability

A prebias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active.This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as FPGA or ASIC.

The PMR family of regulators incorporate synchronous rectifiers, but will not sink current during startup, or whenever the Inhibit pin is held low. However, to ensure satisfactory operation of this function, certain conditions must be maintained.

For more inforamtion, please refer to Application Note 205.

Turbo Trans™ Technology

Turbo Trans™ optimizes the transient response of the regulator with added external capacitance using a single external resistor. The benefits of this technology include: reduced output capacitance, minimized output voltage deviation following a load transient, and enhanced stability when using ultra-low ESR output capacitors. The amout of output capacitance required to meet a target output voltage deviation, is reduded with Turbo Trans™ activated. Likewise, for a given amout of output capacitance, with Turbo Trans™ engaged, the amplitude of the voltage deviation following a load transient is reduced. Applications requiring tight transient voltage tolerances and minimized capacitor footprint area benefit from this technology.

Utilizing Turbo Trans™ requires connecting a resistor, R_{TT} ,

between the +Sense pin (pin 17) and the Turbo Trans™ pin (pin 19), The value of the resistor directly corresponds to the amount of output capacitance required. For the PMR 5118UW, the minimum required capacitance is 1000µF. When using Turbo Trans™, capacitors with a capacitance×ESR product below 10,000 µF×mΩ are required.

To have a better understanding of the required capacitors with Turbo Trans™, three types of capacitors are defined as below.

a. TypeA = (100 < capacitance × ESR ≤ 1,000)

b. TypeB = (1,000 < capacitance × ESR ≤ 5,000)

c. TypeC = (5,000 < capacitance × ESR ≤ 10,000)

As an example, let's look at a 12-V application requiring a 60 mv deviation during an 15A load transient. A majority of 470µF, 10mΩ output capacitors are used. Use the 12 V, Type B capacitor chart. Dividing 60mV by 15A gives 4mV/A transient voltage deviation per amp of transient load setp. Select 4mV/A on the Y-axis and read across to the "With TurboTrans" plot. Following this point down to the X-axis gives us a minimum required output capacitance of approximately 1500µF. The required R_{TT} resistor value for 1500µF can then be calculated or selected from the below table. The required R_{TT} resistor is approximately 17.4KΩ.

To see the benefit of Turbo Trans™, follow the 4mV/A marking across to the "Without TurboTrans" plot. Following that point down shows that you would need a minimum of 7500µF of output capacitance to meet the same transient deviation limit. This is the benefit of Turbo Trans™ .

A typical Turbo Trans™ application schematic is also shown.

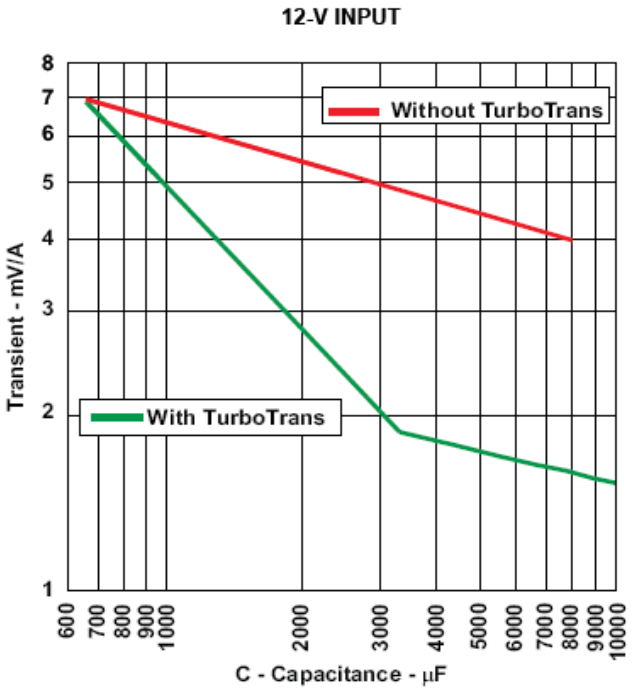


Figure 12. Capacitor Type B,
1000 < C(µF)×ESR(mΩ) ≤ 5000 (e.g. Polymer-Tantalum)

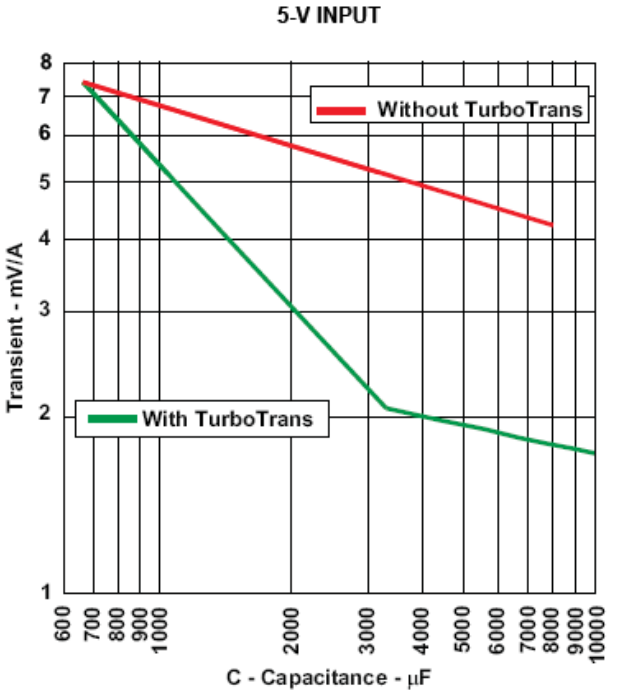


Figure 13. Capacitor Type B,
1000 < C(µF)×ESR(mΩ) ≤ 5000 (e.g. Polymer-Tantalum)

Table: Type B TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			12 Volt Input		5 Volt Input	
25% load step (12.5 A)	50% load step (25 A)	75% load step (37.5 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
100	200	300	660	open	660	open
85	170	255	660	open	750	226
75	150	225	800	143	870	93.1
60	120	180	1050	46.4	1150	34.8
50	100	150	1300	24.9	1450	18.7
40	70	105	1750	11.3	1950	8.45
30	60	90	2500	3.48	2800	1.87
25	50	75	3100	0.649	4000	short

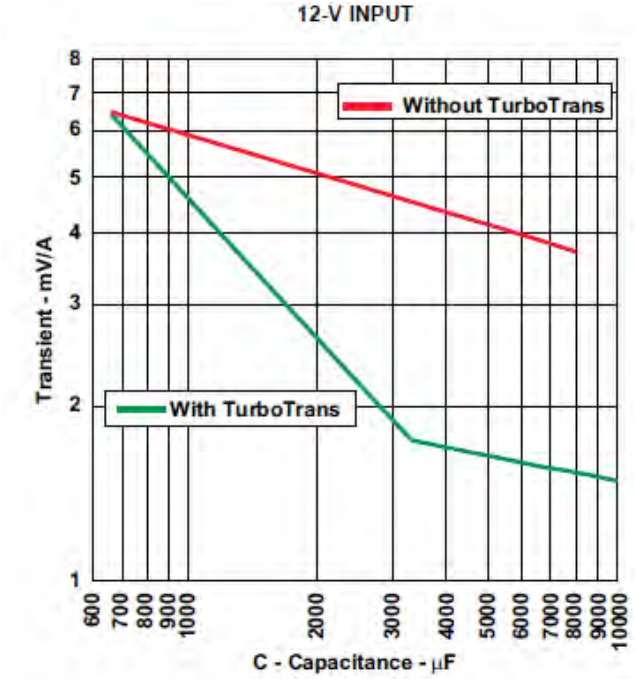


Figure 14. Capacitor Type C, 5000 < C(µF)×ESR(mΩ) ≤ 10,000(e.g. OS-CON)

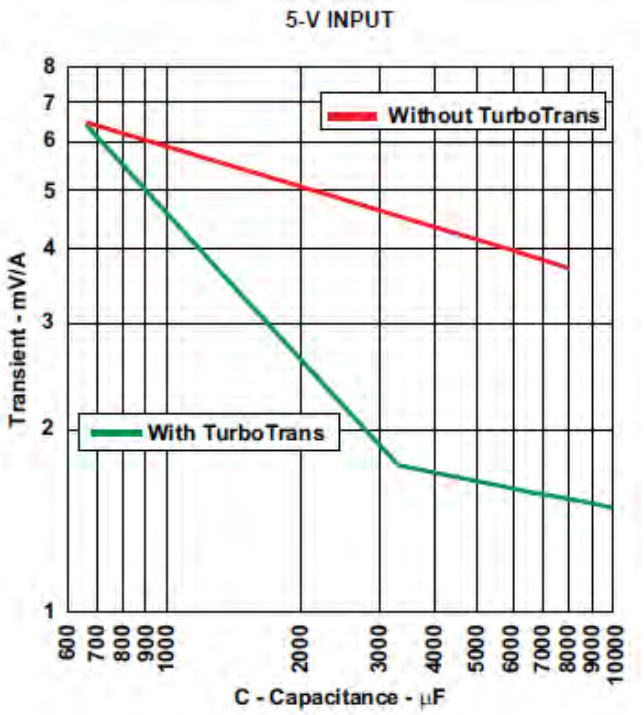


Figure 15. Capacitor Type C, 5000 < C(µF)×ESR(mΩ) ≤ 10,000(e.g. OS-CON)

Table: Type B TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			12 Volt Input		5 Volt Input	
25% load step (12.5 A)	50% load step (25 A)	75% load step (37.5 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
100	200	300	660	open	660	open
85	170	255	660	open	750	226
75	150	225	800	143	870	93.1
60	120	180	1050	46.4	1150	34.8
50	100	150	1300	24.9	1450	18.7
40	70	105	1750	11.3	1950	8.45
30	60	90	2500	3.48	2800	1.87
25	50	75	3100	0.649	4000	short

R_{TT} Resistor Selection

The Turbo Trans™ resistor value, R_{TT} can be determined from the Turbo Trans™ programming equation, see the equation below.

$$R_{TT} = 40 \times \frac{1 - (\frac{C_o}{3300})}{5 \times (\frac{C_o}{3300}) - 1} (k\Omega)$$

Where C_o is the total output capacitance in µF. C_o values greater than or equal to 3300 µF require R_{TT} to be a short,

0Ω. (The above equation results in a negative value for R_{TT} when $C_o \geq 3300$ µF)

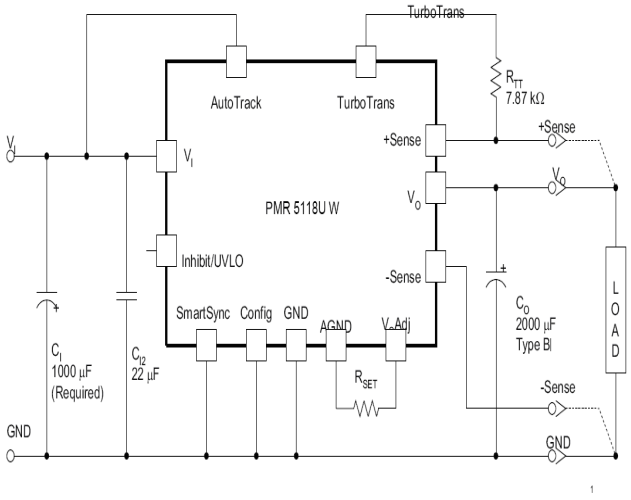


Figure: Typical TurboTrans™ Application

Thermal Consideration

General

The regulators are designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation.
Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependant on the airflow across the regulator. Increased airflow enhances the cooling of the regulator.

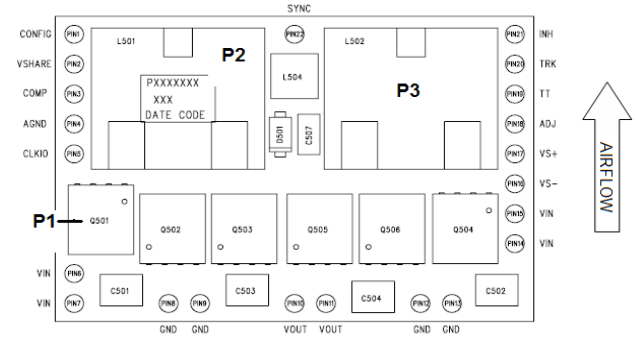
The typical Output Current Derating graph can be found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at V_I = 12 V.

The product is tested on a 100 x 100 mm double-sided PCB with 2 oz. copper and the direction of airfow fro pin 10 to pin 22. For surface mount packages, multiple vias must be utilized.

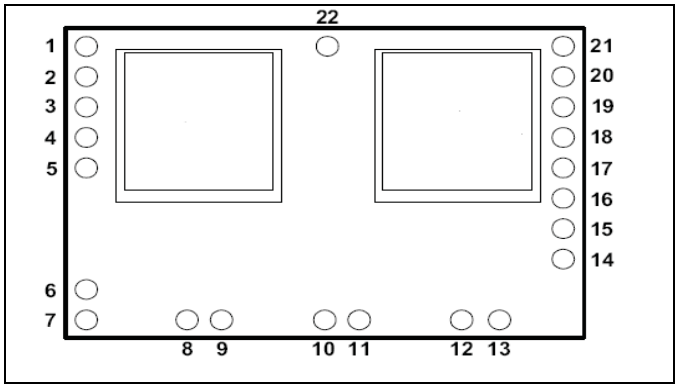
Definition of product operating temperature

The product operating temperatures is used to monitor the temperature of the product, and proper thermal conditions can be verified by measuring the temperature at positions P1, P2, and P3. The temperature at these positions (T_{P1}, T_{P2}, T_{P3},) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above maximum T_{P1}, measured at the reference point P1 are not allowed and may cause permanent damage.

Position	Description	Max Temp.
P1	Reference point (Q501)	T_{P1}=130º C
P2	Inductor (L501)	T_{P2}=130º C
P3	Inductor (L502)	T_{P3}=130º C



Connections

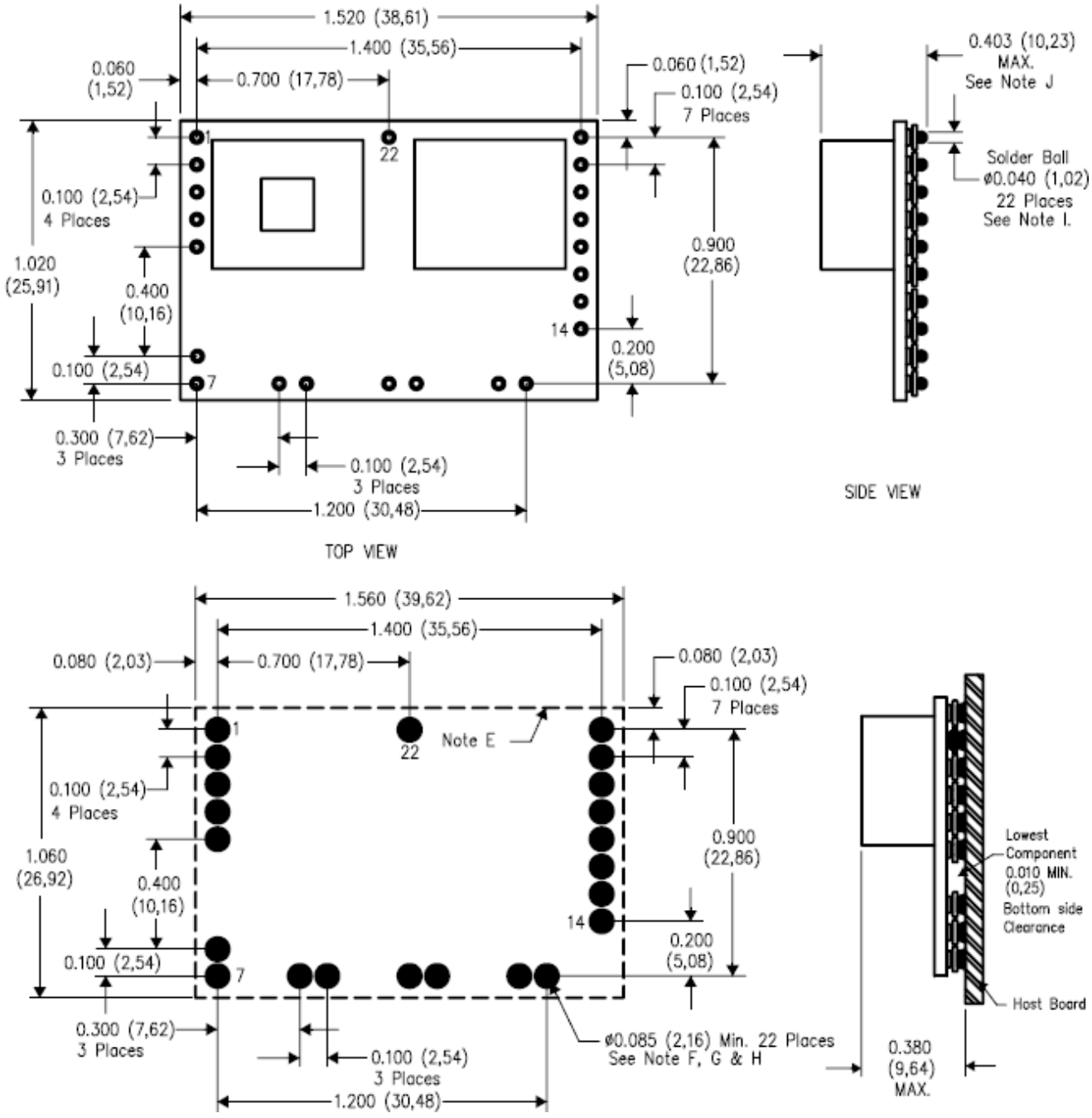


Pin	Designation	Function
1	CONFIG	When two modules are connected together to share load current one must be configured as the MASTER and the other as the SLAVE. This pin is used to configure the module as either MASTER or SLAVE. To configure the module as the MASTER, connect this pin to GND. To condigure the module as the SLAVE, connect this pin to V_I (pin 6). When not sharing current, this pin should be connected to GND.
2	Share	This pin is used when connecting two modules together to share load current. When two modules are sharing the current the Share pin of both modules must be connected together. When not sharing current, this pin MUST be left open (floating).
3	Comp	This pin is used when connecting two modules together to share load current. When two modules are sharing current the Comp pin of bothe modules must be connected together. When not sharing current, this pin MUST be left open (floating).

4	AGND	This pin is the internal analog ground of the module. This pin provides the return path for the V_oAdjust resistor (R_{SET}). When two modules are sharing current the AGND pin of both modules must be connected together. Also, when two modules are connected, R_{SET} must be connected only on the MASTER module.
5	CLKIO	This pin is used when connecting two modules together to share load current. When two modules are sharing current the CLKO pin of both modules must be connected togethe. When not sharing current, this pin MUST be left open (floating).
6	V_I	The positive input voltage power node to the module, which is referenced to common GND.
7	V_I	See pin 6
8	GND	This is the common ground connection for the V_I and V_o power connections. It is also the 0 V_{dc} reference for the control inputs.
9	GND	See pin 8
10	V_O	This regulated positive power output with respect to GND.
11	V_O	See pin 10
12	GND	See pin 8
13	GND	See pin 8
14	V_I	See pin 6
15	V_I	See pin 6
16	-Sense	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. The –Sense pin should always be connected to GND, either at the load for optimal voltage accuracy, or at the module (pin 13).
17	+Sense	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. The +Sense pin should always be connected to V_O, either at the load for optimal voltage accuracy, or at the module (pin 11).
18	V_o Adjust	A 0.05 W 1% resistor must be directly connected between this pin and pin4 (AGND) to set the output voltage to a value higher than 0.7 V. The temperature stability of the resistor should be 100 ppm/℃ (or better). The setpoint range for the output voltage is from 0.7V to 3.6V. If left open circuit, the output voltage defaults to its lowest value. For further information, refer to the information for each output voltage sector.
19	Turbo Trans™	This input pin adjusts the transient response of the regulator. To activate the Turbo Trans™ feature, a 1%, 50mW resistor must be connected between this pin and pin 17 (+Sense) very close to the module. For a given value of output capacitance, a reduction in peak output voltage deviation is achieved by using this feature. If unused, this pin must be left open-circuit. External capacitance must never be connected to this pin. The resistance requirement can be selected from the Turbo Trans™ resistor table which is shown above.

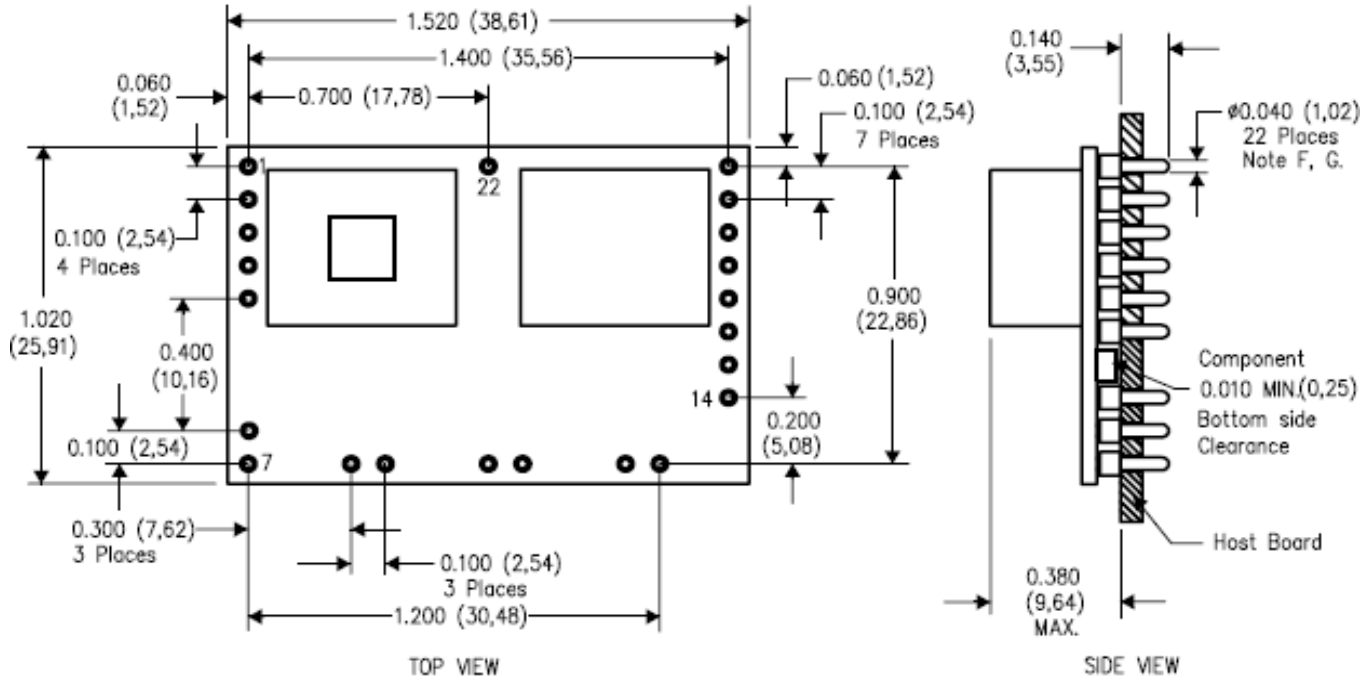
20	Track	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 25 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the module's output voltage follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The features allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V_I . NOTE: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, see the related application note.
21	Inhibit and UVLO	The Inhibit pin is an open-collector/drain, negative logic input that is referenced to GND. Applying a low level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied. This pin is also used for input undervoltage lockout(UVLO) programming. Connecting a resistor from this pin to GND (pin 13) allows the ON threshold of the UVLO to be adjusted higher than the default value. For more information, see related application information.
22	SmartSync	This input pin sychronizes the switching frequency of the module to an external clock frequency. The SmartSync feature can be used to sychronize the switching frequency of multiple modules, aiding EMI noise suppression efforts. The external synchronization frequency must be present before a valid input voltage is present, or before the release of inhibit control. If unused, this pin MUST be connected to GND. For more information, please see the related application note.

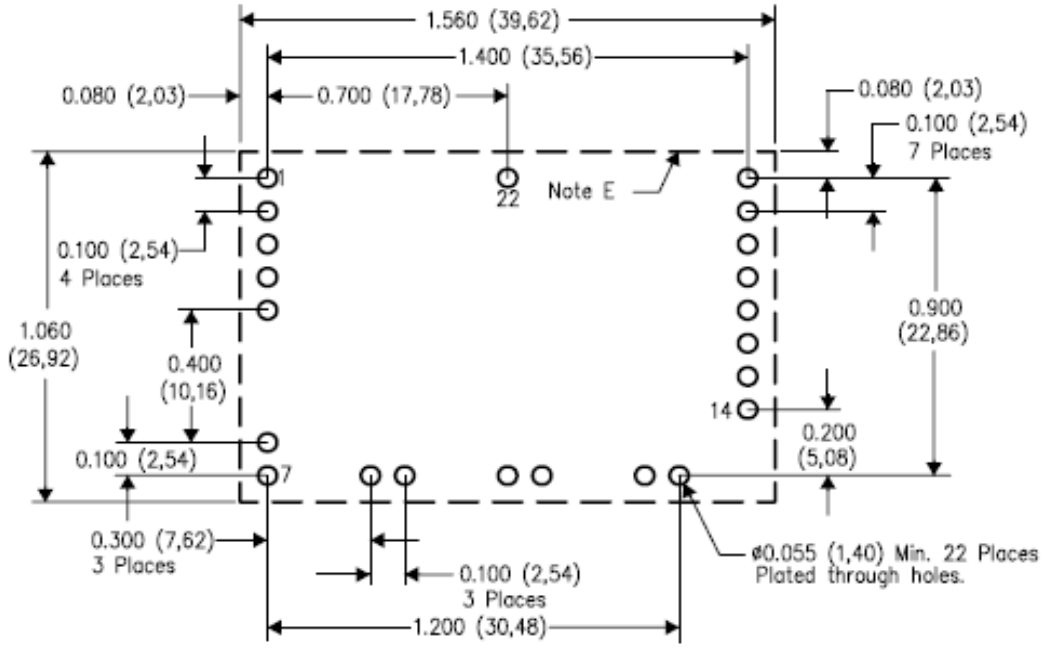
Mechanical Information - Surface mount version



NOTES: A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm)
D. 3 place deciamls are ±0.010 (±0,25mm)
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the elctrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16)
Paste screen thickness: 0.006 (0,15)
H. Pad type: Solder mask defined.
I. This is a lead-free solder ball design.
Finish: Tin (100%) over Nickel plating
Solder ball: 96.5 Sn/3.0 Ag/0.5 Cu
J. Dimension prior to reflow solder.

Mechanical Information- Through hole mount version





NOTES: A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material - Copper Alloy
Finish - Tin (100%) over Nickel Plating.

Soldering Information - Hole Mounting

The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

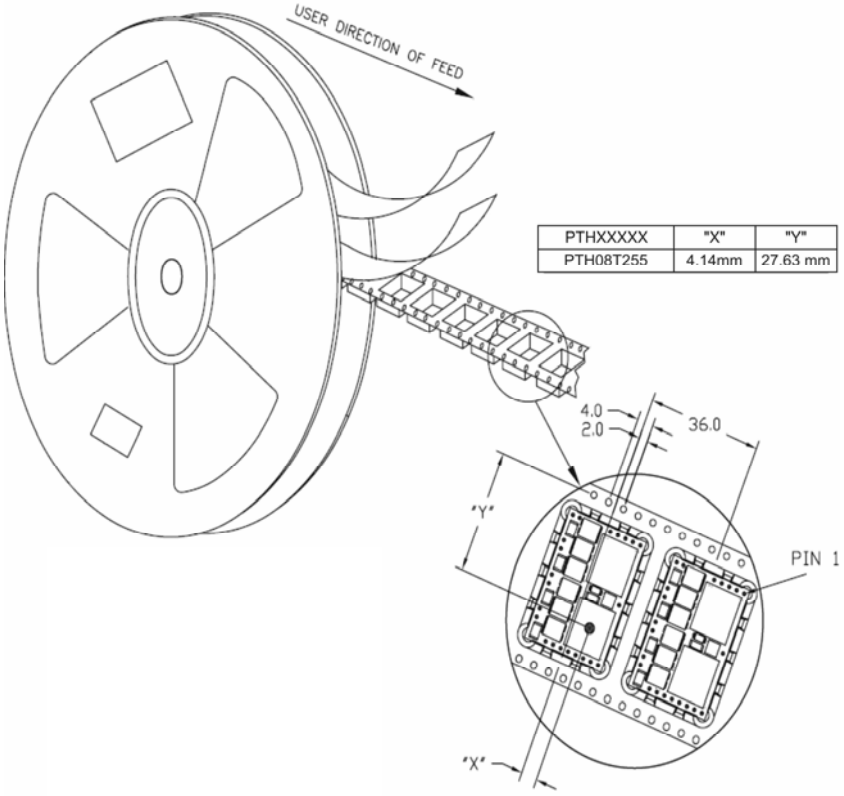
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

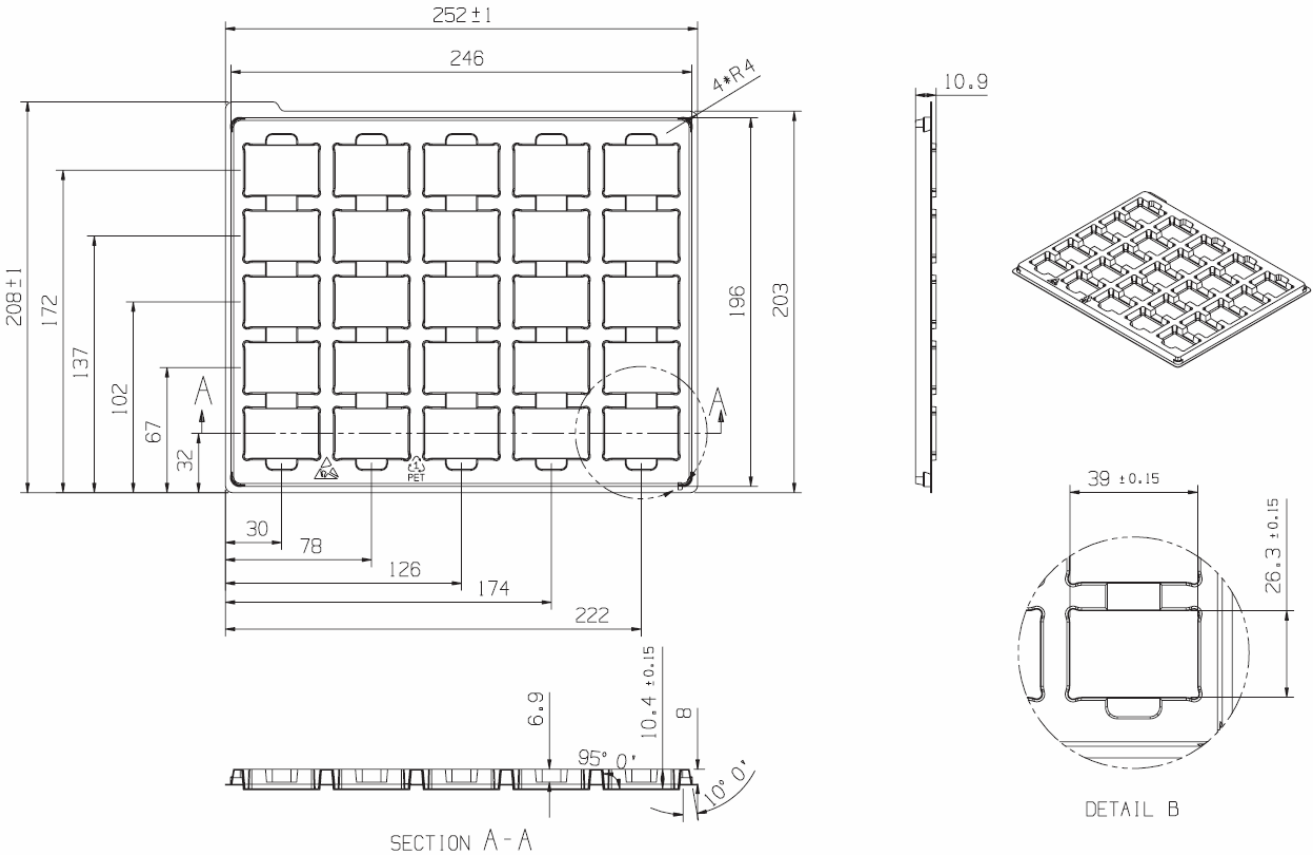
Delivery Package Information

The products are delivered in tape and reel (SMD) or antistatic trays (TH & SMD)

Reel Specifications	
Material	Antistatic PS
Surface resistance	10^8 < Ohm/square < 10^{12}
Bakeability	The reels cannot be baked
Tape width, W	56 mm [2.205 inch]
Pocket pitch, P_1	36 mm [1.417 inch]
Pocket depth, K_0	10.4 mm [0.41 inch]
Reel diameter	330 mm [13 inch]
Reel capacity	150 products /reel
Reel weight	150 g empty, 2550 g/full reel
Carrier thickness	0.05 mm [0.002 inch]
Box capacity	300 products [2 reel/box)



Tray Specifications	
Material	Antistatic PET
Surface resistance	10^8 < Ohm/square < 10^{12}
Bakability	The trays cannot be baked
Tray thickness	0.8 mm [0.03 inch]
Box capacity	125 products (5 full trays/box)
Tray weight	40 g empty, 440 g/full tray
Tray capacity	25 products/tray



Dry pack information

The products are delivered in trays or tape on reel. These inner shipment containers are dry packed in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033A (Handling, packing, shipping, and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to the referred IPC/JEDEC standard.

Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T_A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether Isopropyl alcohol	55°C 35°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity [1]	J-STD-020C	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 260°C
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Resistance to soldering heat [2]	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td [1] IEC 60068-2-20 test Ta [2]	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C Steam ageing 235°C 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g^2/Hz 10 min in each direction

Notes
[1] Only for products intended for reflow soldering (surface mount products)
[2] Only for products intended for wave soldering (plated through hole products)

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Flex:

PMR5118UWP