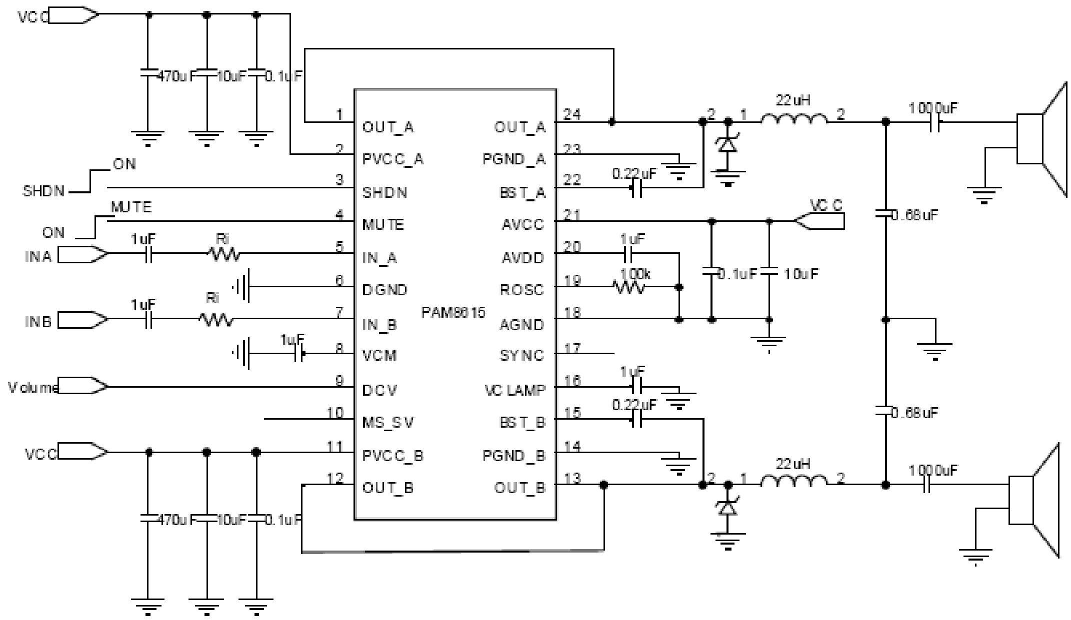
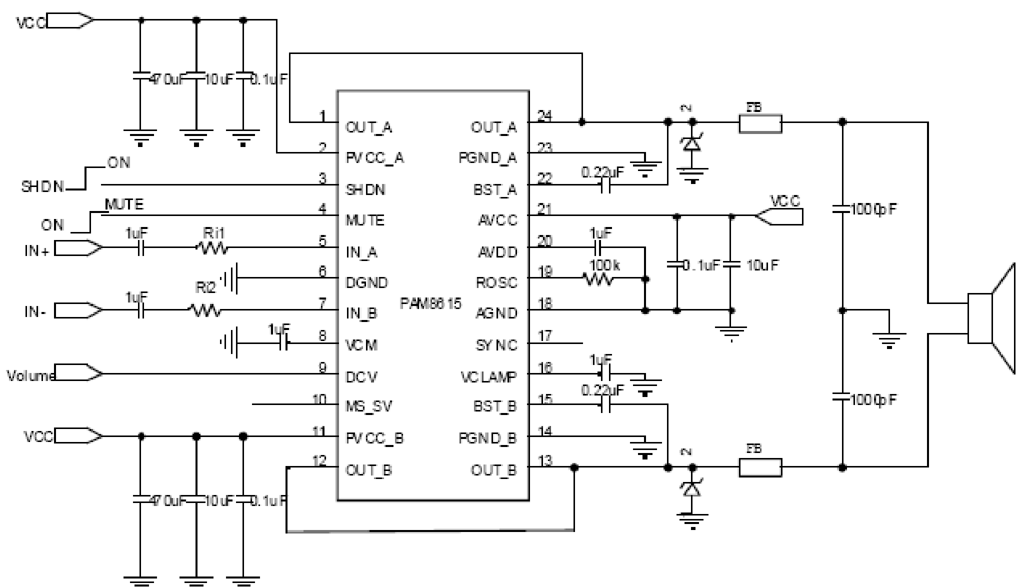
Typical Applications Circuit



Single-Ended Configuration

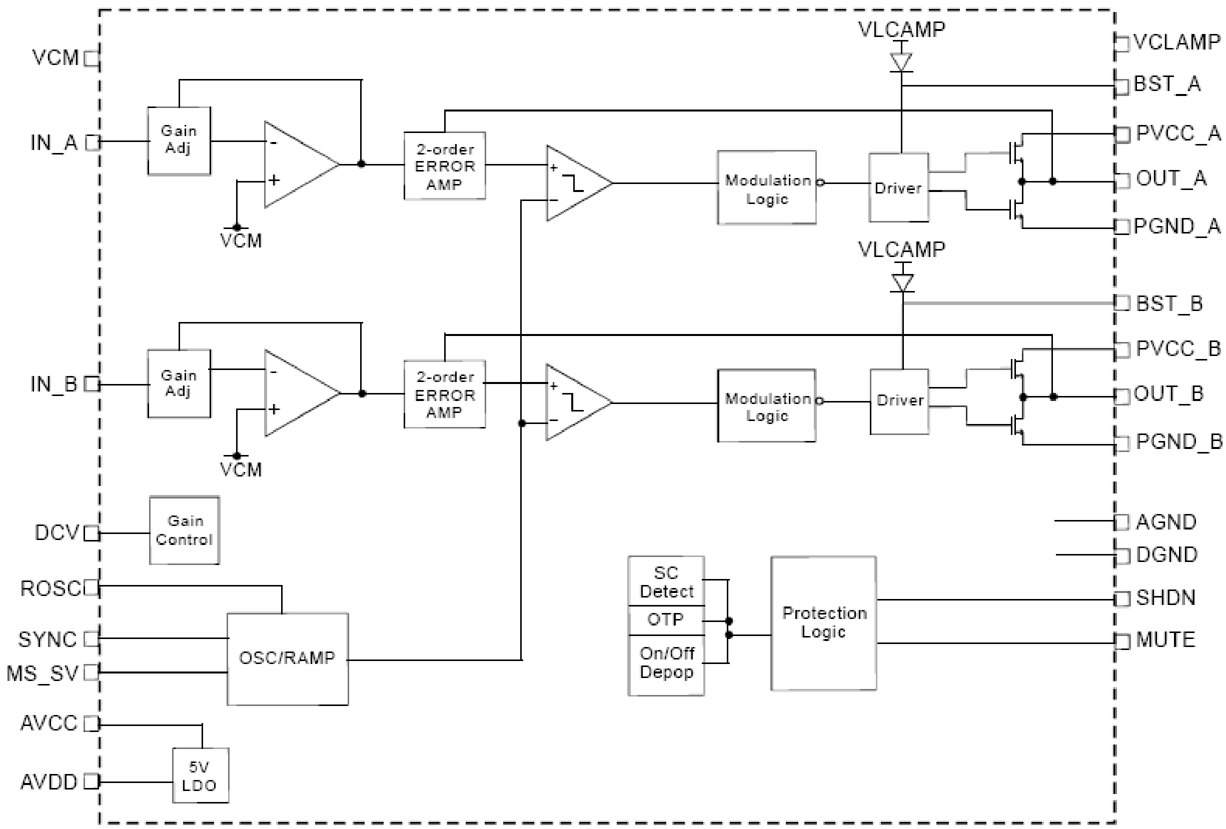


BTL Configuration

Pin Descriptions

Pin Number	Pin Name	I/O/P	Function
1	OUT_A	O	H-bridge A output.
2	PVCC_A	P	Power supply for H-bridge A not connected to PVCC_B or AVCC.
3	SHDN	I	Shutdown signal for IC (low = shutdown, high = operat ional). TTL logic levels with compliance to AVCC.
4	MUTE	I	Alogic high on this pin disables the outputs. A low on this pin enables the outputs. TTL logic levels with compliance to AVCC.
5	IN_A	I	Audio input for channel A.
6	DGND	P	Digital GND
7	IN_B	I	Audio input for channel B.
8	VCM	O	Reference for analog cells.
9	DCV	I	DC voltage setting the gain of the amplifier.
10	MS_SV	I	Master/Slave select for determining direction of SYNC terminal. High = Master mode, SYNC terminal is an output; Low = Slave mode, SYNC terminal accept s a clock input.
11	PVCC_B	P	Power supply for H-bridge B, not connected to PVCC_A or AVCC
12, 13	OUT_B	O	H-bridge B output
14	PGND_B	P	Power ground for H-bridge B
15	BST_B	I/O	Bootstrap I /O for H-bridge B high-side FET
16	VCLAMP	P	Internally generated voltage supply for bootst rap. Not to be used as a supply or connected to any component other than the decoupling capacitor.
17	STNC	I/O	Clock i nput/output for synchroni zing multiple class-D devices. Direction determined by MS_SV terminal.
18	AGND	P	Analog GND.
19	ROSC	I/O	Current s etting resis tor for ramp generator.
20	AVDD	P	Analog 5V Regulated output.
21	AVCC	P	High-voltage analog power supply.
22	BST_A	I/O	Bootstrap I /O for H-bridge A high-side FET.
23	PGND_A	P	Power ground for H-bridge A.

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Parameter	Rating	Unit
Supply Voltage AVCC, PVCC	-0.3 to +30	V
Logic Input Voltage:		
SHDN, MUTE	-0.3 to AVCC +0.3	V
DCV, MS_SV, SYNC	0 to +5.5	
Analog Input Voltage:		
IN-A, IN-B	0 to +5.5	V
Storage Temperature	-65 to +150	°C
Soldering Temperature	300, 5sec	

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage (V_{CC})	10 to 26	V
DCV Volume Control Pin	0 to 5	
f_{OSC} Oscillator Frequency (R_{OSC} = 100kΩ)	250 to 350	kHz
T_A – Operating Free-Air Temperature	-40 to +85	°C
Ambient Operating Temperature	-20 to +85	
Ambient Temperature Range	-40 to +160	
Junction Temperature Range	-40 to +85	

Thermal Information

Parameter	Package	Symbol	Max	Unit
Thermal Resistance (Junction to Ambient)	TSSOP-24	θ_{JA}	30	°C/W

Electrical Characteristics (@T_A = +25°C, V_{CC} = 24V, Gain = 20dB, R_L = 4Ω, unless otherwise specified.)

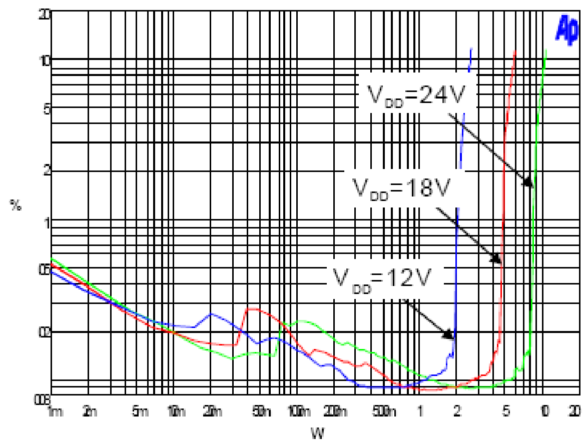
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Class-D Output Offset Voltage (measured differently)	|VOS|	V_I = 0V, AV = 36dB		10	65	mV
Quiescent Supply Current	I_{CC}	SHDN = 2V, MUTE = 0V, Input AC_GND, No load		25	40	mA
Quiescent Supply Current in Mute Mode	$I_{CC(MUTE)}$	MUTE = 2V, No load		25	40	mA
Quiescent Supply Current in Shutdown Mode	$I_{CC(SD)}$	SHDN = 0.5V, No load		5	20	μA
Oscillator Frequency	f_{OSC}	R_{OSC} = 100kΩ		323		kHz
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{CC} = 24V,IO = 1A, TA = 27°C		220		mΩ
Power Supply Rejection Ratio	PSRR	V_{CC} = 23.5V to 24.5V		-60		dB
Output Power at 1% THD+N	P_O(SE)	V_{CC} = 24V, R_L = 4Ω, f = 1kHz		14		W
		V_{CC} = 24V, R_L = 8Ω, f = 1kHz		8.2		
Output Power at 10% THD+N		V_{CC} = 24V, R_L = 4Ω, f = 1kHz		17.3		
		V_{CC} = 24V, R_L = 8Ω, f = 1kHz		9.8		
Output Power at 1% THD+N	P_O(BTL)	V_{CC} = 24V, R_L = 8Ω, f = 1kHz		27		W
		V_{CC} = 12V, R_L=8Ω, f = 1kHz		7		
Output Power at 10% THD+N		V_{CC} = 24V, R_L = 8Ω, f = 1kHz		35		
		V_{CC} = 12V, R_L = 8Ω, f = 1kHz		9		
Total Harmonic Distortion + Noise	THD+N	R_L = 4Ω, f = 1kHz, P_o = 10W		0.25%		
		R_L = 8Ω, f = 1kHz, P_o = 5W		0.15%		
Output Integrated Noise Floor	V_N	20Hz to 22kHz, A-weighted filter, Gain = 20dB		-67		dBV
Crosstalk	C_S	P_O = 1W, f = 1kHz, Gain = 20dB		-60		dB
Signal-to-Noise Ratio	SNR	Max output at THD+N<1%, f = 1kHz, Gain = 20dB		86		dB
Thermal Trip Point				160		°C
Thermal Hystersis				40		°C

DC Volume Control

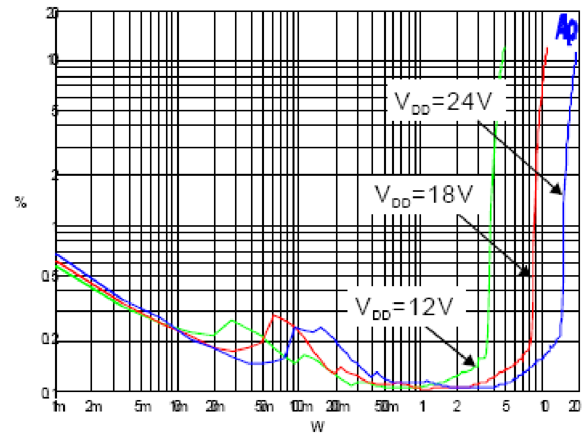
STEP	VOLTAGE OF THE VOLUME	TOTAL_GAIN	STEP	VOLTAGE OF THE VOLUME	TOTAL_GAIN
	(V)	(dB)		(V)	(dB)
1	0.10	-60	33	2.34	17.4
2	0.17	-40	34	2.41	18.0
3	0.24	-30	35	2.48	18.6
4	0.31	-20	36	2.55	19.2
5	0.38	-10	37	2.62	19.8
6	0.45	-5	38	2.69	20.4
7	0.52	-2.5	39	2.76	21.0
8	0.59	0	40	2.83	21.6
9	0.66	2	41	2.90	22.2
10	0.73	3	42	2.97	22.8
11	0.80	4	43	3.04	23.4
12	0.87	4.8	44	3.11	24.0
13	0.94	5.4	45	3.18	24.6
14	1.01	6.0	46	3.25	25.2
15	1.08	6.6	47	3.32	25.8
16	1.15	7.2	48	3.39	26.4
17	1.22	7.8	49	3.46	27.0
18	1.29	8.4	50	3.53	27.6
19	1.36	9.0	51	3.60	28.2
20	1.43	9.6	52	3.67	28.8
21	1.50	10.2	53	3.74	29.4
22	1.57	10.8	54	3.81	30.0
23	1.64	11.4	55	3.88	30.6
24	1.71	12.0	56	3.95	31.2
25	1.78	12.6	57	4.02	31.8
26	1.85	13.2	58	4.09	32.4
27	1.92	13.8	59	4.16	33.0
28	1.99	14.4	60	4.23	33.6
29	2.06	15.0	61	4.30	34.2
30	2.13	15.6	62	4.37	34.8
31	2.20	16.2	63	4.44	35.4
32	2.27	16.8	64	4.51	36.0

Typical Performance Characteristics (@T_A = +25°C, V_{DD} = 24V, R_L = 8Ω, unless otherwise specified.)

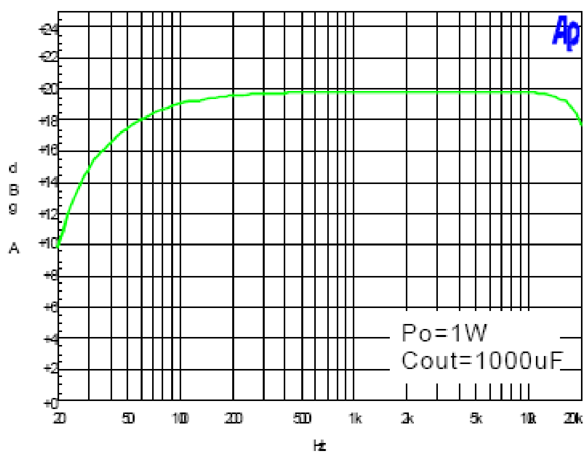
1. THD Power —Single-Ended(Load=8Ω)



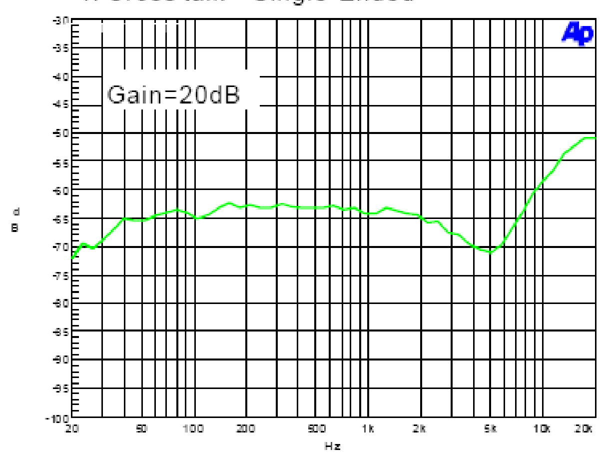
2. THD Power —Single-Ended(load=4Ω)



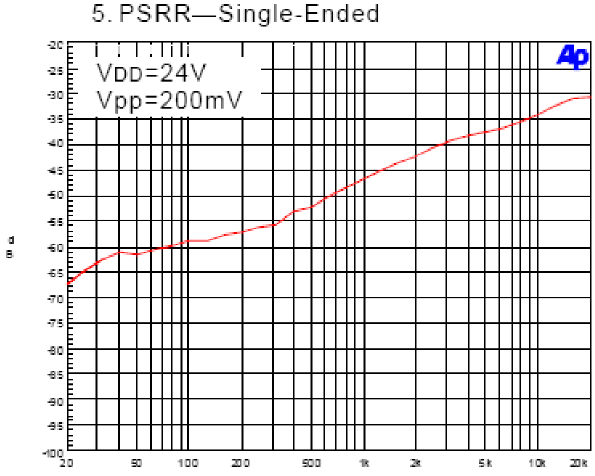
3. Frequency response—Single-Ended



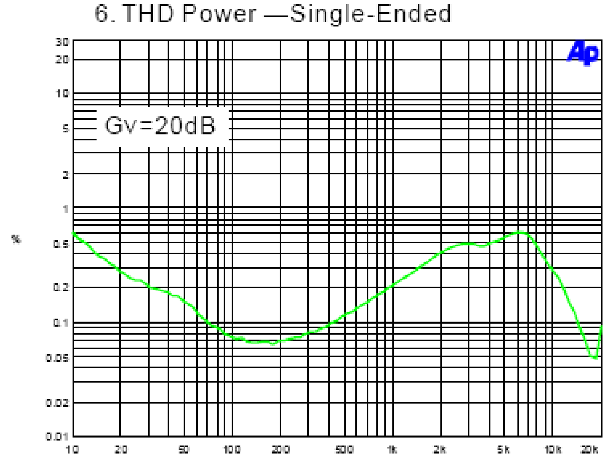
4. Cross talk—Single-Ended



5. PSRR—Single-Ended

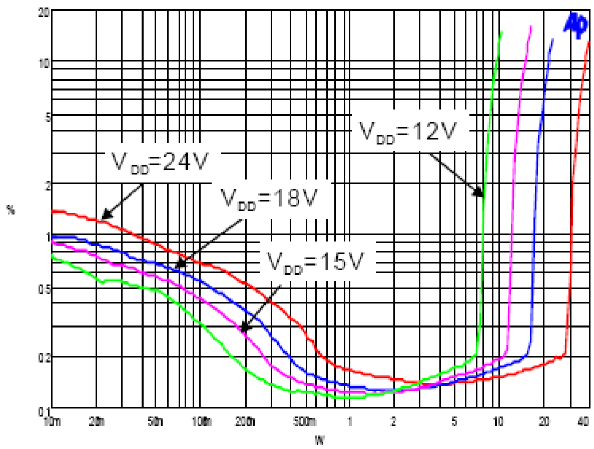


6. THD Power —Single-Ended

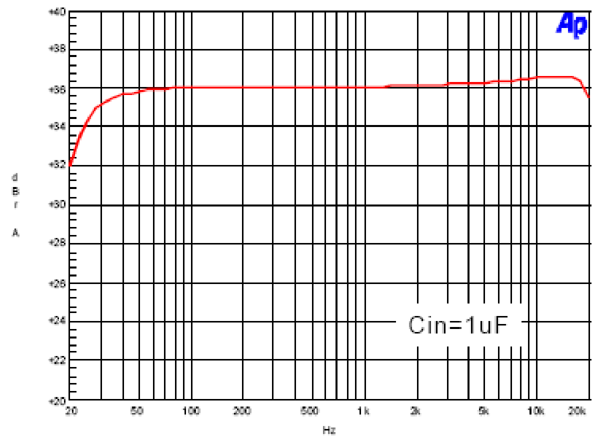


Typical Performance Characteristics (cont.) (@T_A = +25°C, V_{DD} = 24V, R_L = 8Ω, unless otherwise specified.)

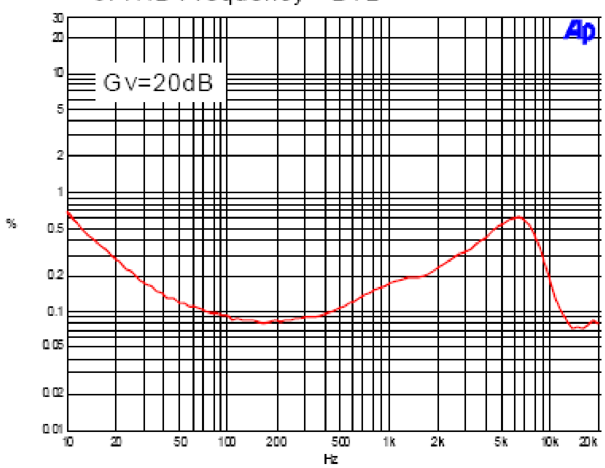
7. THD Power—BTL



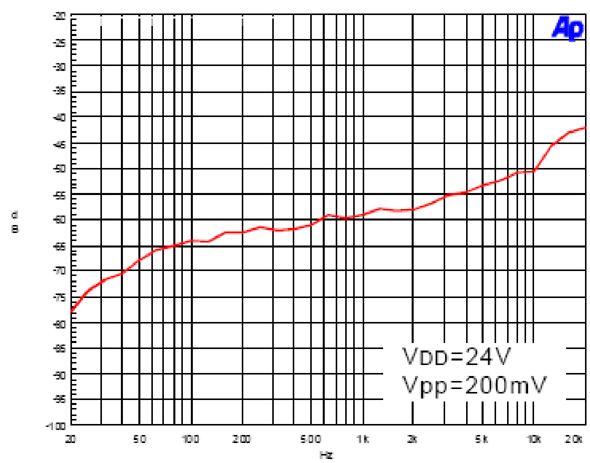
8. Frequency response—BTL



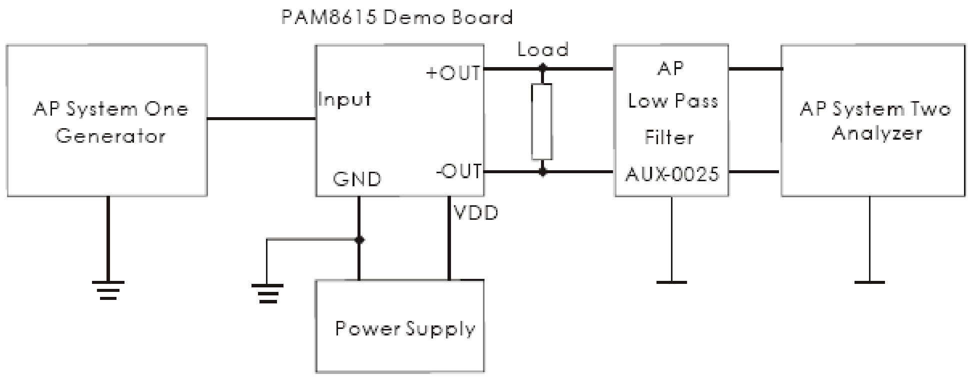
9. THD Frequency—BTL



10. PSRR—BTL



Test Setup for Performance Testing



Notes: 1. The AP AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
2. Two 22µH inductors are used in series with load resistor to emulate the small speaker for effic iency measurement.

Application Information

Power and Heat Dissipation

Choose speakers that are able to stand large output power from the PAM8615. Otherwise, speaker may suffer damage.

Heat dissipation is very important when the device works in full power operation. Two factors affect the heat dissipation, the efficiency of the device that determines the dissipation power, and the thermal resistance of the package that determines the heat dissipation capability.

Generally, Class–D amplifiers are high efficiency and need no heat sink. For high power ones that has high dissipation power, the heat sink may also not necessary if the PCB is carefully designed to achieve good heat dissipation by the PCB itself.

Dual-Side PCB

To achieve good heat dissipation, the PCB's copper plate should be thicker than 35µm and the copper plate on both sides of the PCB should be utilized for heat sink.

The thermal pad on the bottom of the device should be soldered to the plate of the PCB, and via holes, usually 9 to 16 should be drilled in the PCB area under the device and deposited copper on the vias should be thick enough so that the heat can be dissipated to the other side of the plate. There should be no insulation mask on the other side of the copper plate. It is better to drill more vias on the PCB around the device if possible.

Volume Control

A DC volume control section is integrated in PAM8615, controll ing via DCV and DGND terminals. The voltage on DCV pin, determines internal amplifier gain as listed in Page 6.

If a resistor divider is used to fix gain of the amplifier, the DCV terminal can be directly connected to the resistor divider connected across AVDD and DGND. For fixed gain, the resistor divider values are calculated to center the voltage given in Page 6.

MUTE Operation

The MUTE pin is an input for controlling the output state of the PAM8615. A logic high on this pin disables the outputs and low enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade.

Application Information (cont.)

Shutdown Operation

The PAM8615 employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The SD input terminal should be pull high during normal operation when the amplifier is in use. Pulling SD low causes the outputs to mute and the amplifier to enter a low-current state. SD should never be left unconnected to prevent the amplifier from unpredictable operation.

For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Internal Bias Generator Capacitor Selection

The internal bias generator (VCM) provides the internal bias for the preamplifier stage. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the VCM terminal is critical for achieving the best device performance. During startup or recovery from shutdown state, the VCM capacitor determines the rate at which the amplifier starts up. The startup time is not critical for the best de-pop performance since any heard pop sound is the result of the class-D output switching-on other than that of the startup time. However, at least a 0.47μF capacitor is recommended for the VCM capacitor.

Another function of the VCM capacitor is to bypass high frequency noise on the internal bias generator.

Power Supply Decoupling, CS

The PAM8615 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents oscillations caused by long lead between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-seriesresistance (ESR) ceramic capacitor, typically 0.1μF, is recommended, placing as close as possible to the device's PVCC lead. To filter lower-frequency noises, a large aluminum electrolytic capacitor of 470μF or greater is recommended, placing near the audio power amplifier. The 10μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

Selection of ROSC

The switching frequency is determined by the values of components connected to ROSC (pin 19) and calculated with the following equation:

$$f_{OSC} = \frac{0.68}{R_{OSC} \times 21pF}$$

The recommended values is R_{OSC} = 100KΩ for a switching frequency of 323kHz.

BST_A and BST_B Capacitors

The half H-bridge output stages use NMOS transistors only. They therefore require bootstrap capacitors for the high side of each output to turn on correctly. An at least 220nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from OUT_A to BST_A, and another 220nF capacitor from OUT_B to BST_B. It is recommended to use 1μF BST capacitor to replace 220nF for lower than 100Hz applications.

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors not exceeded, two internal regulators are used to clamp the gate voltage. A 1μF capacitors must be connected from VCLAMP to ground and must be rated for at least 25V. The voltages at the VCLAMP terminals vary with VCC and may not be used to power any other circuitry.

Internal Regulated 5-V Supply (AVDD)

The AVDD terminal is the output of an internallygenerated 5V supply, used for the oscillator, preamplifier, and volume control circuitry. It requires a 0.1μF to 1μF capacitor, placed very close to the pin to Ground to keep the regulator stable. The regulator may not be used to power any external circuitry.

Application Information (cont.)

Using low-ESR Capacitors

Low - ESR capacitors are recommended throughout this application section. A real (with respect to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves as an ideal capacitor.

Short-Circuit Protection

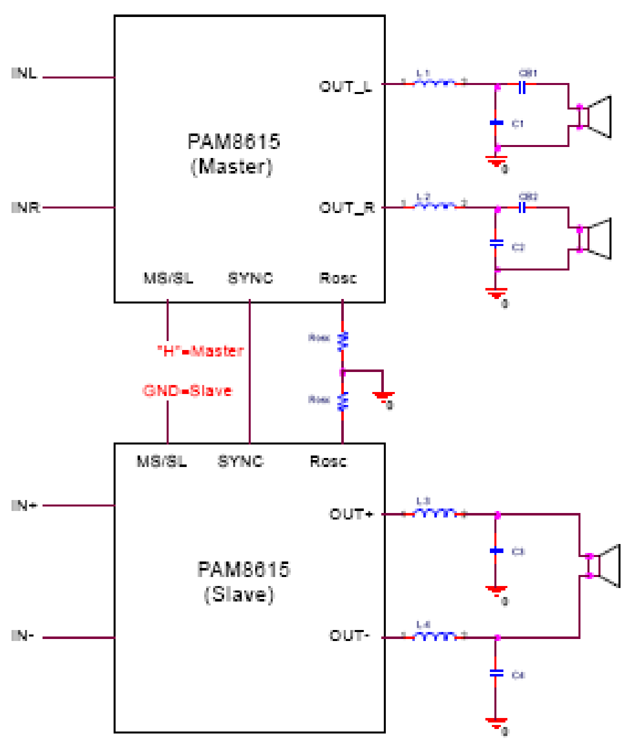
The PAM8615 has short circuit protection circuitry on the outputs to prevent damage to the device when output-to-output shorts (BTL mode), output-to- GND shorts, or output-to-VCC shorts occur. Once a short-circuit is detected on the outputs, the output drive is immediately disabled. This is a latched fault and must be reset by cycling the voltage on the SD pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

Thermal Protection

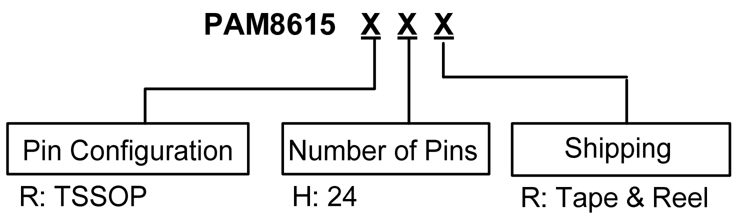
Thermal protection on the PAM8615 prevents damage to the device when the internal die temperature exceeds +160°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the set thermal point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by +40°C. The device begins normal operation at this point without external system intervention.

Master-Slave and SYNC Operation

The MS/SL and SYNC terminals can be used to synchronize the frequency of the class-D output switching. When the MS/SL is high or left floating due to the internal pull up resistor, the switching frequency is determined by the ROSC. The SYNC becomes an output whose source/sink current is about 0.5mA, and the frequency of this output is also determined by the ROSC. And this output can be connected to another PAM8615 who is configured in the slave mode. The output switching is synchronized to avoid any beat frequencies that occur in the audio band when two Class-D amplifiers in the same system are switching at the slight different frequencies. When the MS/SL is low, the switching frequency is determined by the incoming square wave on the SYNC input. The SNYC becomes an input in this mode and accept a square wave from another PAM8615 configured in the master mode or from an external GPIO.
(Key: MS/SL = "H", Master Mode, MS/SL = "L", Slave Mode)

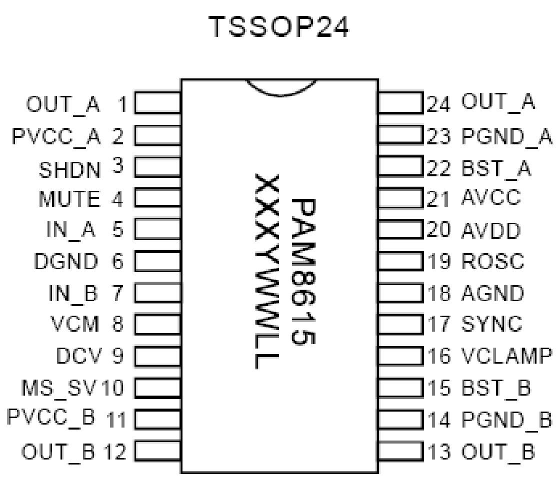


Ordering Information



Part Number	Package Type	Standard Package
PAM8615RHR	TSSOP-24	3000 Units/Tape & Reel

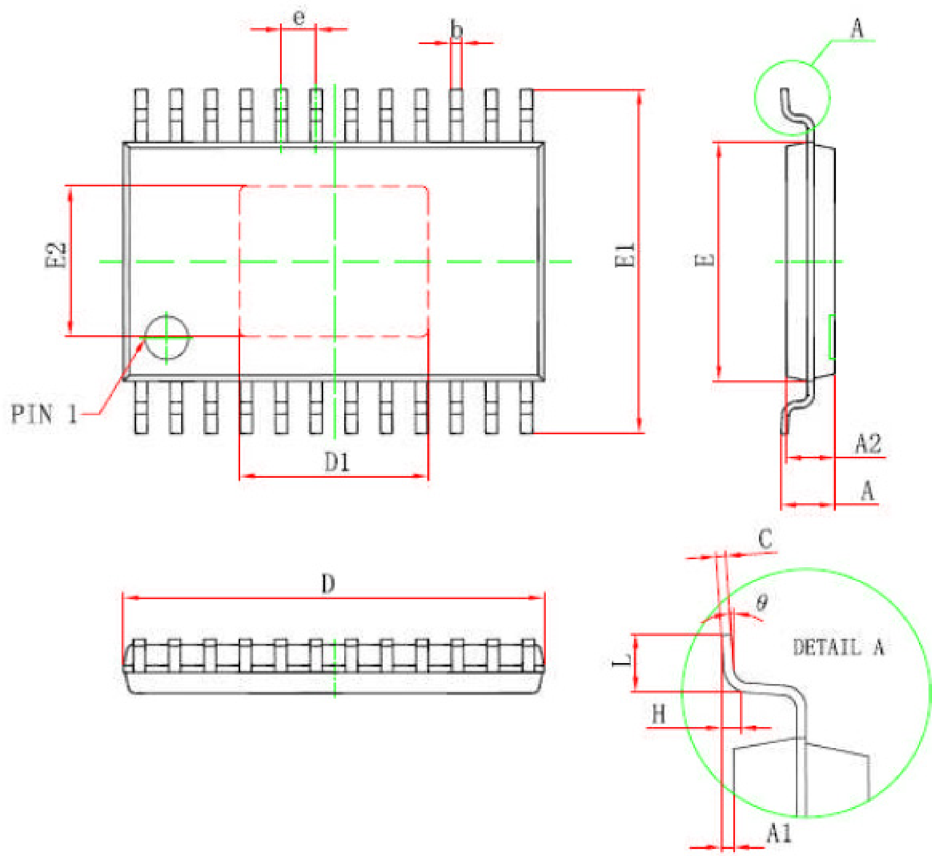
Marking Information



X: Internal Code
Y: Year
WW: Week
LL: Internal Code

Package Outline Dimensions (All dimensions in mm.)

TSSOP-24



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	7. 700	7. 900	0. 303	0. 311
D1	3. 400	3. 600	0. 134	0. 138
E	4. 300	4. 500	0. 169	0. 177
b	0. 190	0. 300	0. 007	0. 012
c	0. 090	0. 200	0. 004	0. 008
E1	6. 250	6. 550	0. 246	0. 258
E2	2. 700	2. 900	0. 106	0. 122
A		1. 100		0. 043
A2	0. 800	1. 000	0. 031	0. 039
A1	0. 020	0. 150	0. 001	0. 006
e	0. 65 (BSC)		0. 026 (BSC)	
L	0. 500	0. 700	0. 02	0. 028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°