Ball Assignments

27 bit 1:1 Register

	1	2	3	4	5	6
A	DCKE0	D0	V_{REF}	V_{DD}	QCKE0	QCKE1
B	DCKE1	D1	GND	GND	Q0	Q1
C	D2	DODT1	V_{DD}	V_{DD}	Q2	DNU
D	DODT0	$\overline{\text{PTYERR}}$	GND	GND	QODT0	QODT1
E	D3	D4	V_{DD}	V_{DD}	Q3	Q4
F	D5	D6	GND	GND	Q5	Q6
G	PAR_IN	$\overline{\text{RESET}}$	V_{DD}	V_{DD}	NC	NC
H	CK	$\overline{\text{DCS0}}$	GND	GND	$\overline{\text{QCS0}}$	$\overline{\text{QCS1}}$
J	$\overline{\text{CK}}$	$\overline{\text{DCS1}}$	V_{DD}	V_{DD}	NC	NC
K	D7	D8	GND	GND	Q7	Q8
L	D9	D10	V_{DD}	V_{DD}	Q9	Q10
M	D11	D12	GND	GND	Q11	Q12
N	D13	D14	V_{DD}	V_{DD}	Q13	Q14
P	D15	D16	GND	GND	Q15	Q16
R	D17	D18	V_{DD}	V_{DD}	Q17	Q18
T	D19	D20	CSGateEN	V_{DD}	Q19	Q20

General Description

This 27-bit 1:1 registered buffer with parity is designed for 1.7V to 1.9V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load. The **ICSSSTUB32871A** operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going high, and $\overline{CK}$ going low.

The device supports low-power standby operation. When the reset input ($\overline{RESET}$) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when $\overline{RESET}$ is low all registers are reset, and all outputs except $\overline{PTYERR}$ are forced low. The LVCMOS $\overline{RESET}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{RESET}$ until the input receivers are fully enabled, the design of the **ICSSSTUB32871A** must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The device monitors both $\overline{DCS0}$ and $\overline{DCS1}$ inputs and will gate the Qn outputs from changing states when both $\overline{DCS0}$ and $\overline{DCS1}$ are high. If either $\overline{DCS0}$ or $\overline{DCS1}$ input is low, the Qn outputs will function normally. The $\overline{RESET}$ input has priority over the $\overline{DCS0}$ and $\overline{DCS1}$ control and will force the Qn outputs low and the $\overline{PTYERR}$ output high. If the DCS-control functionality is not desired, then the CSGateEnable input can be hardwired to ground, in which case, the setup-time requirement for DCS would be the same as for the other D data inputs.

The **ICSSSTU32871A** includes a parity checking function. The **ICSSSTUB32871A** accepts a parity bit from the memory controller at its input pin PARIN, compares it with the data received on the D-inputs and indicates whether a parity error has occurred on its open-drain $\overline{PTYERR}$ pin (active LOW).
Package options include 96-ball Thin Profile Fine Pitch BGA (TFBGA, MO-TBD).

Inputs							Output
$\overline{RESET}$	$\overline{DCS0}$	$\overline{DCS1}$	CK	$\overline{CK}$	# of inputs = H (D0-D21)	PARIN*	$\overline{PTYERR}$**
H	L	H	↑	↓	Even	L	H
H	L	H	↑	↓	Odd	L	L
H	L	H	↑	↓	Even	H	L
H	L	H	↑	↓	Odd	H	H
H	H	L	↑	↓	Even	L	H
H	H	L	↑	↓	Odd	L	L
H	H	L	↑	↓	Even	H	L
H	H	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	$\overline{PTYERR}_0$
H	X	X	L or H	L or H	X	X	$\overline{PTYERR}_0$
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	H

* PARIN arrives one clock cycle after the data to which it applies.

** This transition assumes $\overline{PTYERR}$ is high at the crossing of CK going high and $\overline{CK}$ going low. If $\overline{PTYERR}$ is low, it stays latched low for two clock cycles or until $\overline{RESET}$ is driven low.

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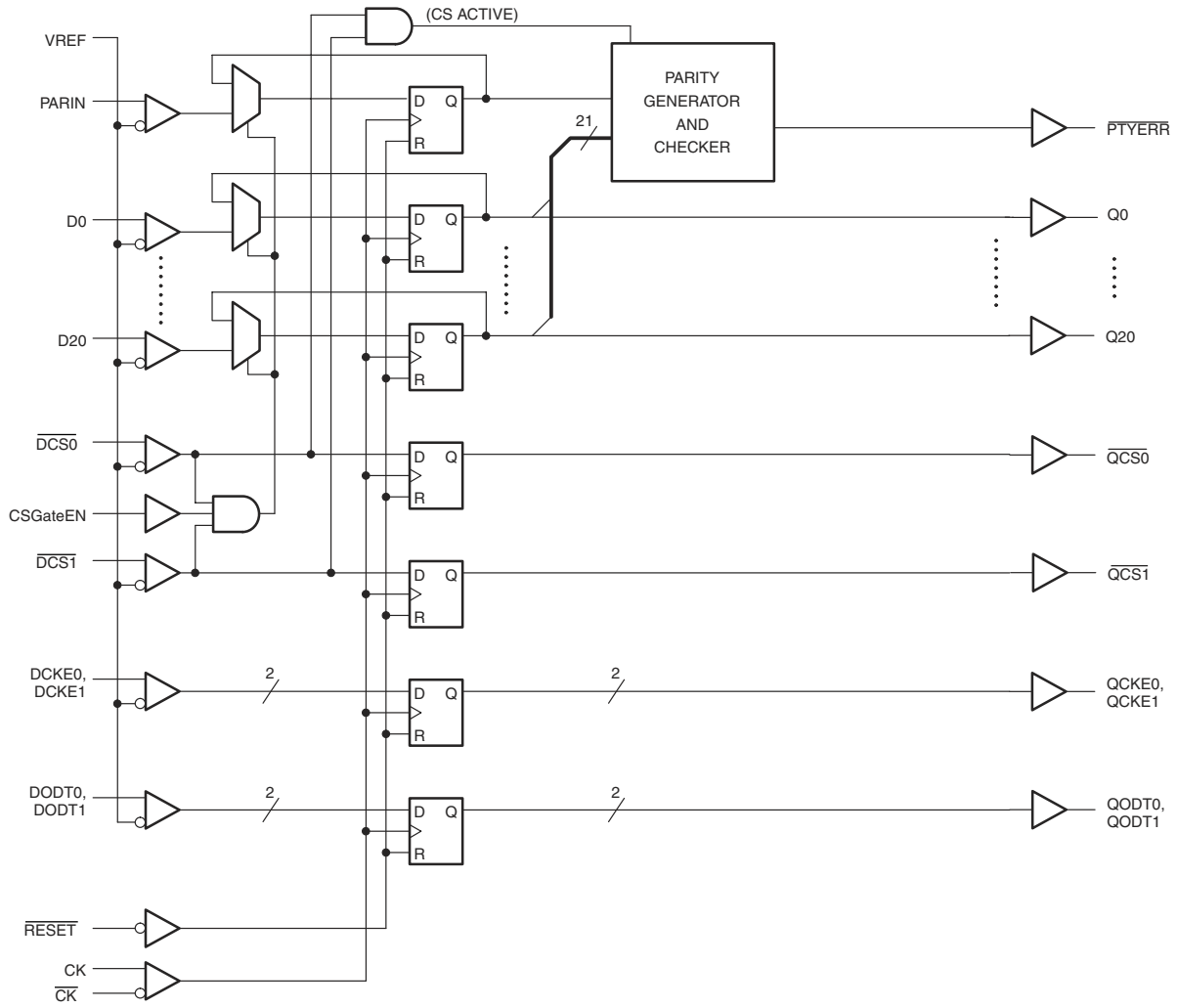
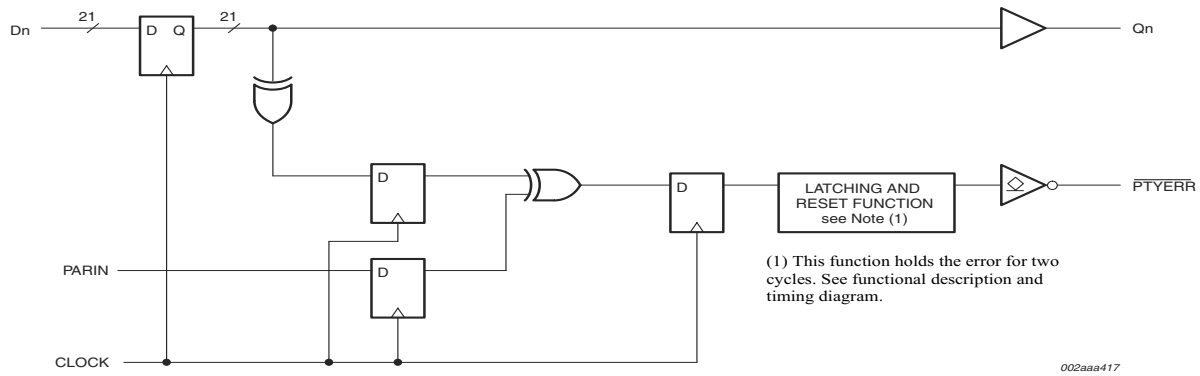
Ball Assignment

Signal Group	Signal Name	Type	Description
Ungated inputs	DCKE0, DCKE1, DODT0, DODT1	SSTL_18	DRAM function pins not associated with Chip Select.
Chip Select gated inputs	D0 ... D20	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW.
Chip Select inputs	$\overline{DCS0}$, $\overline{DCS1}$	SSTL_18	DRAM Chip Select signals. These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The register can be programmed to re-drive all D-inputs only (CSGateEN high) when at least one Chip Select input is LOW.
Re-driven outputs	Q0...Q20, $\overline{QCS0}$-1, QCKE0-1, QODT0-1	SSTL_18	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Parity input	PARIN	SSTL_18	Input parity is received on pin PARIN and should maintain odd parity across the D0...D20 inputs, at the rising edge of the clock.
Parity error output	$\overline{PTYERR}$	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. $\overline{PTYERR}$ will be active for two clock cycles, and delayed by an additional clock cycle for compatibility with final parity out timing on the industry-standard DDR-II register with parity (in JEDEC definition).
Program inputs	CSGateEN	1.8 V LVCMOS	Chip Select Gate Enable. When HIGH, the D0..D20 inputs will be latched only when at least one Chip Select input is LOW during the rising edge of the clock. When LOW, the D0...D20 inputs will be latched and redriven on every rising edge of the clock.
Clock inputs	CK, $\overline{CK}$	SSTL_18	Differential master clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CK).
Miscellaneous inputs	$\overline{RESET}$	1.8 V LVCMOS	Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. $\overline{RESET}$ also resets the $\overline{PTYERR}$ signal.
	VREF	0.9 V nominal	Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.

Block Diagram



Parity Functionality Block Diagram



Register Timing

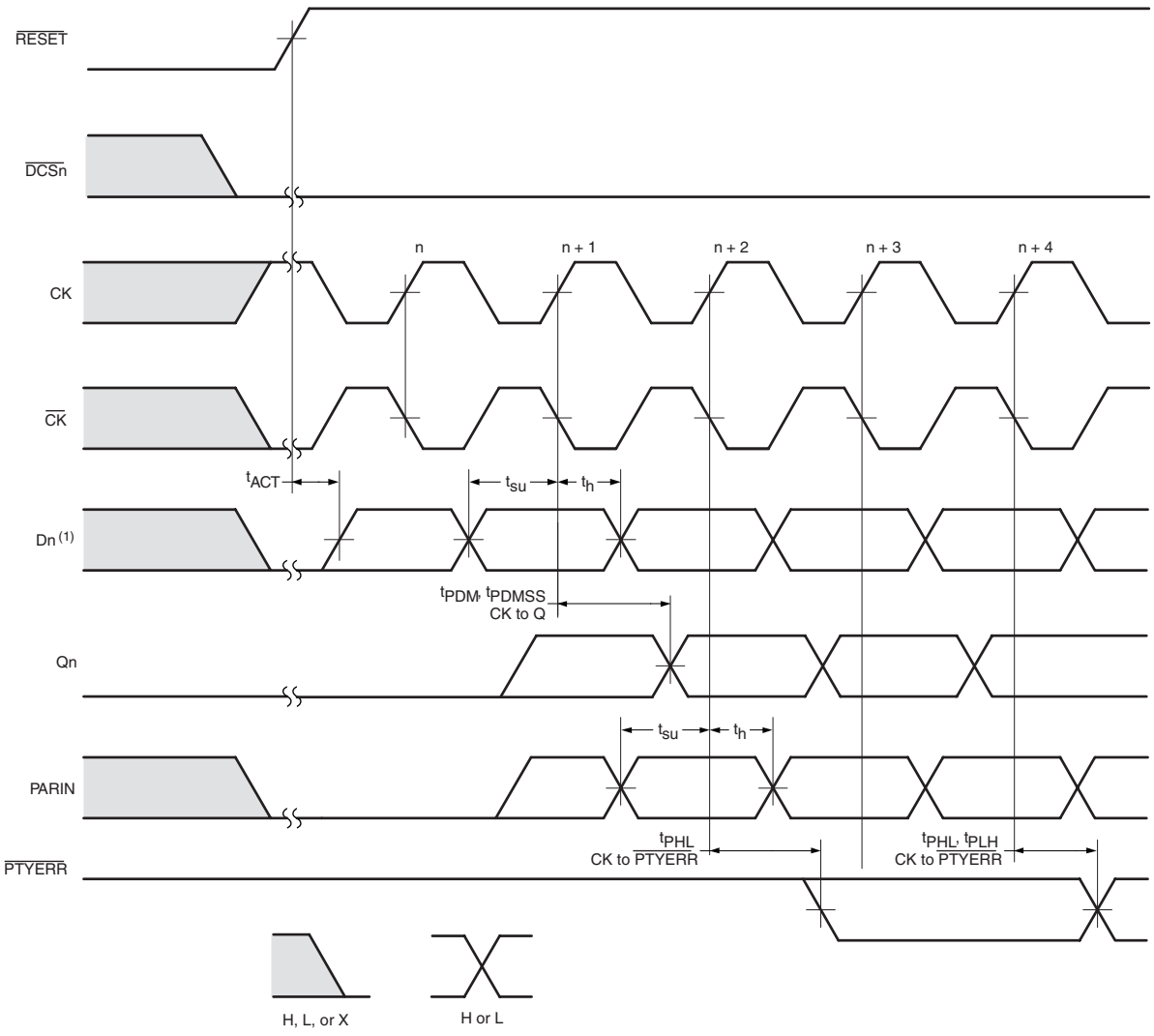


Figure 4 —RESET switches from L to H

(1) After RESET is switched from LOW to HIGH, all data and PARIN input signals must be set and held LOW for a minimum time of t_{ACT} (max) to avoid false error.

Register Timing

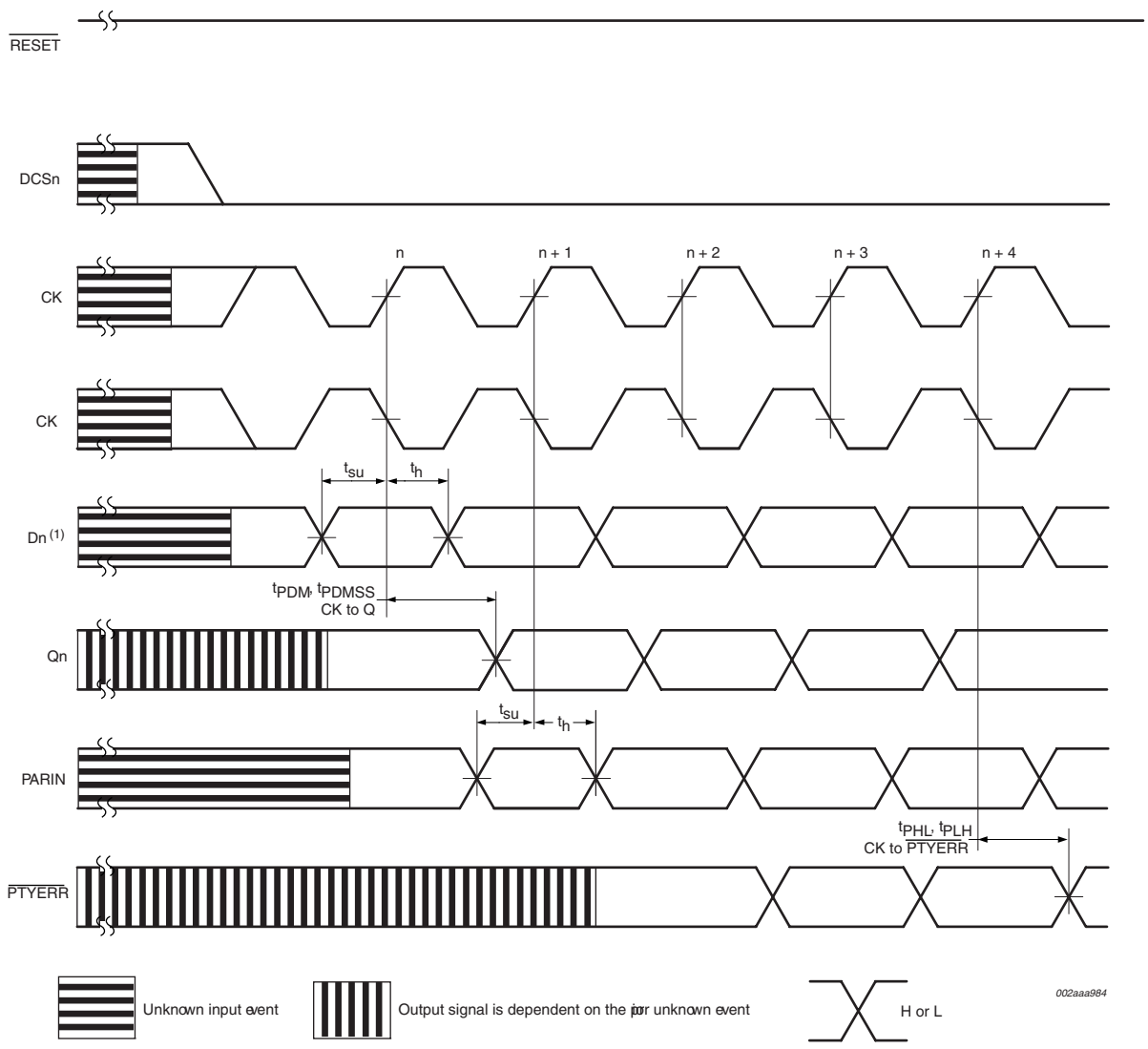


Figure 5 — $\overline{\text{RESET}}$ being held HIGH

Register Timing

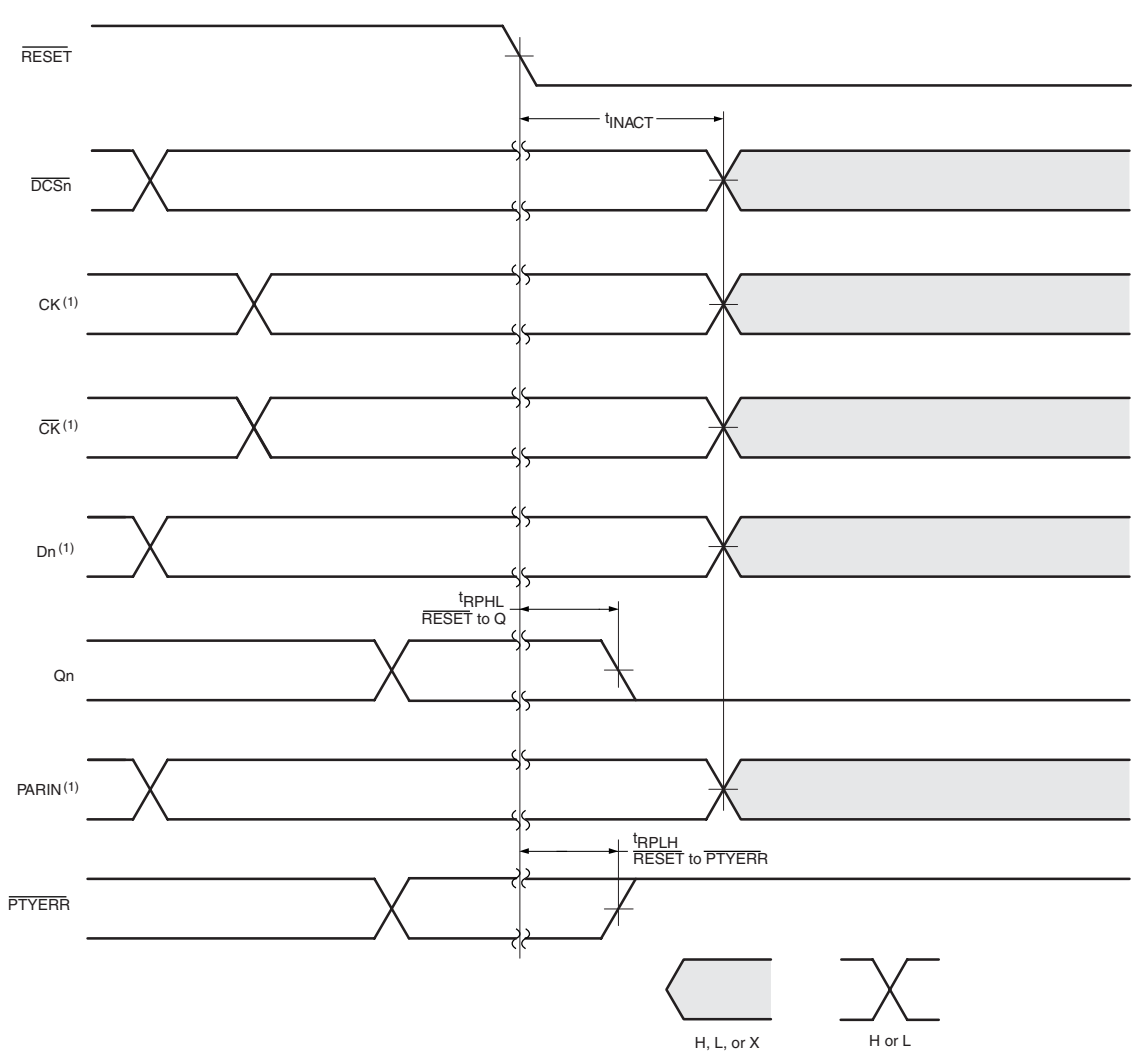


Figure 6 — RESET switches from H to L

(1) After Reset is switched from HIGH to LOW, all data and clock input signals must be set and held at valid logic levels (not floating) for a minimum time of t_{INACT} (max)

Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Supply Voltage	-0.5V to 2.5V
Input Voltage[1,]	-0.5V to VDD +2.5V
Output Voltage[1,2]	-0.5V to VDDQ + 0.5V
Input Clamp Current	±50 mA
Output Clamp Current	±50mA
Continuous Output Current	±50mA
VDD or GND Current/Pin	±100mA
Package Thermal Impedance[3]	36°C

Notes:
1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This value is limited to 2.5V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
V_{DDQ}	I/O Supply Voltage		1.7	1.8	1.9	V
V_{REF}	Reference Voltage		0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	
V_{TT}	Termination Voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	
V_I	Input Voltage		0		V_{DDQ}	
$V_{IH\ (DC)}$	DC Input High Voltage	Data Inputs	V_{REF} + 0.125			
$V_{IH\ (AC)}$	AC Input High Voltage		V_{REF} + 0.250			
$V_{IL\ (DC)}$	DC Input Low Voltage				V_{REF} - 0.125	
$V_{IL\ (AC)}$	AC Input Low Voltage				V_{REF} - 0.250	
V_{IH}	Input High Voltage Level	$\overline{\text{RESET}}$	0.65 x V_{DDQ}			
V_{IL}	Input Low Voltage Level				0.35 x V_{DDQ}	
V_{ICR}	Common mode Input Range	CK, $\overline{\text{CK}}$	0.675		1.125	
V_{ID}	Differential Input Voltage		0.600			
I_{OH}	High-Level Output Current				-8	mA
I_{OL}	Low-Level Output Current				8	
T_A	Operating Free-Air Temperature		0		70	°C

[1]Guaranteed by design, not 100% tested in production.

Note: $\overline{\text{Rst}}$ and Cn inputs must be helf at valid logic levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{\text{Rst}}$ is low.

Electrical Characteristics - DC

T_A = 0 - 70°C; V_{DD} = 2.5 +/-0.2V, V_{DDQ}=2.5 +/-0.2V; (unless otherwise stated)

SYMBOL	PARAMETERS	CONDITIONS		V_{DDQ}	MIN	TYP	MAX	UNITS
V_{OH}		I_{OH} = -8mA		1.7V	1.2			V
V_{OL}		I_{OL} = 8mA		1.7V			0.5	
I_I	All Inputs	$V_I = V_{DD}$ or GND		1.9V			±5	µA
I_{DD}	Standby (Static)	$\overline{RESET}$ = GND	I_O = 0	1.9V			200	µA
	Operating (Static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, $\overline{RESET} = V_{DD}$					150	mA
I_{DDD}	Dynamic operating (clock only)	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLK switching 50% duty cycle.		1.8V		TBD		µA/clock MHz
	Dynamic Operating (per each data input)	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLK switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle				TBD		µA/ clock MHz/data
C_i	Data Inputs	$V_I = V_{REF}$ ±350mV			2.5		5	pF
	CLK and $\overline{CLK}$	V_{ICR} = 1.25V, $V_{I(PP)}$ = 360mV			2		3.8	
	$\overline{RESET}$	$V_I = V_{DDQ}$ or GND				4.5		pF

Notes:
1 - Guaranteed by design, not 100% tested in production.

Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range (See figure 7)

PARAMETER	V_{DD} = 1.8V ± 0.1V		UNIT
	MIN	MAX	
dV/dt_r	1	4	V/ns
dV/dt_f	1	4	V/ns
dV/dt_Δ[1]		1	V/ns

1. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

Timing Requirements

(over recommended operating free-air temperature range, unless otherwise noted)

SYMBOL	PARAMETERS		V_{DD} = 1.8V ±0.1V		UNITS
			MIN	MAX	
f_{clock}	Clock frequency			410	MHz
t_W	Pulse duration		1		ns
t_{ACT}	Differential inputs active time			10	ns
t_{INACT}	Differential inputs inactive time			15	ns
t_S	Setup time	Data before CLK↑, $\overline{CLK}$↓	0.6		ns
		$\overline{DCS0}$, $\overline{DSC1}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ HIGH	0.7		
t_H	Hold time	$\overline{DCS}$, DODT, DCKE and Dn after CLK↑, $\overline{CLK}$↓	0.6		ns
	Hold time	PAR_IN after CLK↑, $\overline{CLK}$↓	0.5		ns

Notes: 1 - Guaranteed by design, not 100% tested in production.
2 - For data signal input slew rate of 1V/ns.
3 - For data signal input slew rate of 0.5V/ns and < 1V/ns.
4 - CLK/$\overline{CLK}$ signal input slew rate of 1V/ns.

Switching Characteristics

(over recommended operating free-air temperature range, unless otherwise noted)

Symbol	Parameter	Measurement Conditions	MIN	MAX	Units
fmax	Max input clock frequency		410		MHz
t_{PDM}	Propagation delay, single bit switching	CLK↑ and $\overline{CLK}$↓ to Qn	1.25	1.9	ns
t_{LH}	Low to High propagation delay	CLK↑ and $\overline{CLK}$↓ to $\overline{PTYERR}$	1.2	3	ns
t_{HL}	High to low propagation delay	CLK↑ and $\overline{CLK}$↓ to $\overline{PTYERR}$	0.9	3	ns
t_{PDMSS}	Propagation delay simultaneous switching	CLK↑ and $\overline{CLK}$↓ to Qn		2	ns
t_{PHL}	High to low propagation delay	$\overline{RESET}$↓ to Qn↓		3	ns
t_{PLH}	Low to High propagation delay	$\overline{RESET}$↓ to $\overline{PTYERR}$↑		3	ns

1. Guaranteed by design, not 100% tested in production.

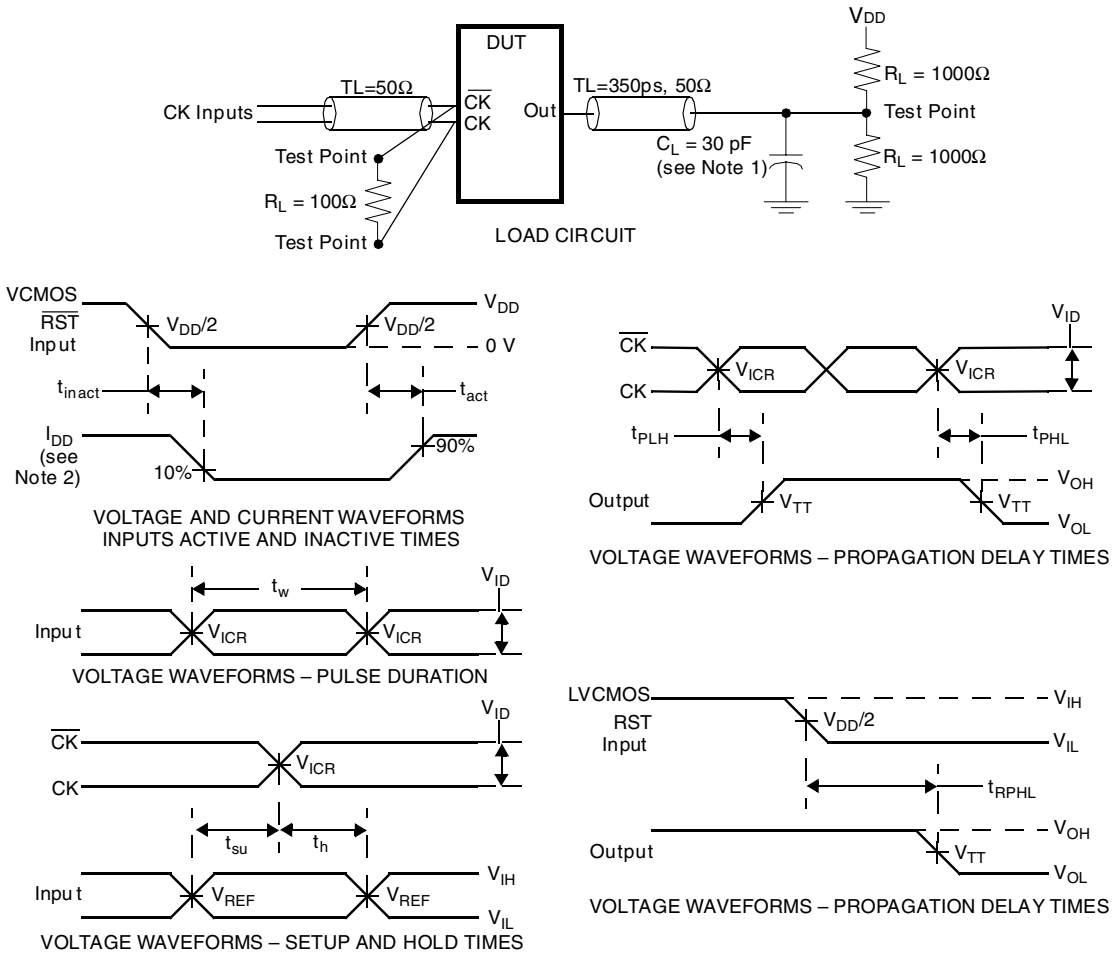
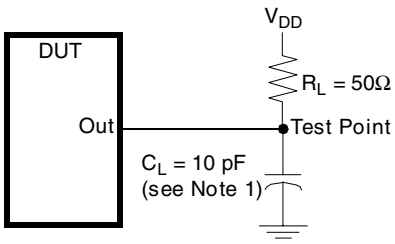


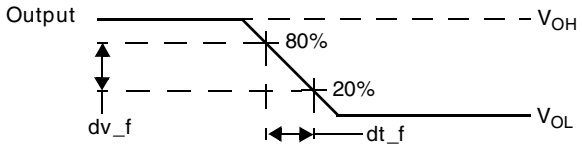
Figure 6 —Parameter Measurement Information (V_{DD} = 1.8V± 0.1V)

Notes: 1. C_L incluces probe and jig capacitance.

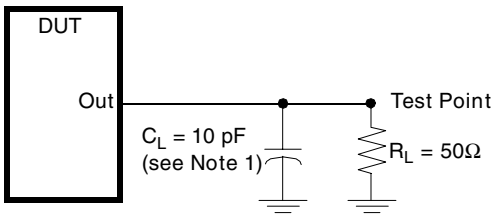
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and Io = 0mA.
3. All input pulses are supplied by generators having the following chareacteristics: PRR ≤10 MHz, Zo=50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{REF} = V_{DD}/2$
6. $V_{IH} = V_{REF}$ + 250 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
7. $V_{IL} = V_{REF}$ - 250 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. V_{ID} = 600 mV
9. t_{PLH} and t_{PHL} are the same as t_{PDM}.



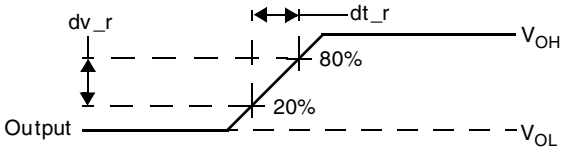
LOAD CIRCUIT – HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS – HIGH-TO-LOW SLEW-RATE MEASUREMENT



LOAD CIRCUIT – LOW-TO-HIGH SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS – LOW-TO-HIGH SLEW-RATE MEASUREMENT

Figure 7 — Output Slew-Rate Measurement Information (V_{DD}= 1.8V± 0.1V)

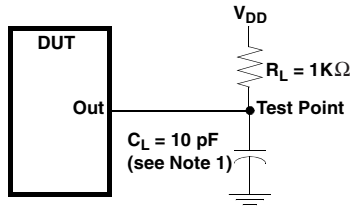
Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

3 Test circuits and switching waveforms (cont'd)

3.3 Error output load circuit and voltage measurement information (V_{DD} = 1.8 V ± 0.1 V)

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50Ω ; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



LOAD CIRCUIT – HIGH-TO-LOW SLEW-RATE MEASUREMENT

(1) C_L includes probe and jig capacitance.

Figure 28 — Load circuit, error output measurements

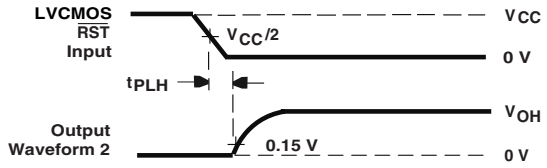


Figure 29 — Voltage waveforms, open-drain output low-to-high transition time with respect to reset input

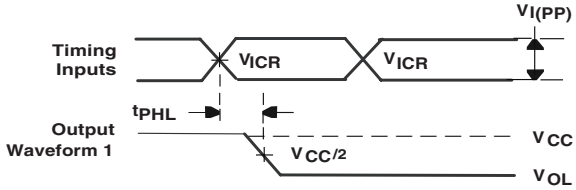


Figure 30 — Voltage waveforms, open-drain output high-to-low transition time with respect to clock inputs

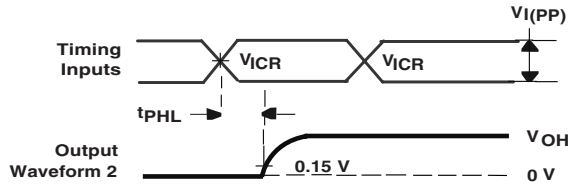
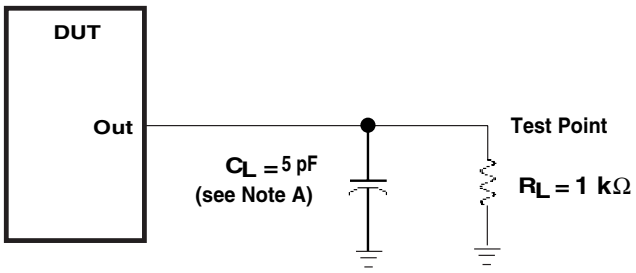


Figure 31 — Voltage waveforms, open-drain output low-to-high transition time with respect to clock inputs

3 Test circuits and switching waveforms (cont'd)

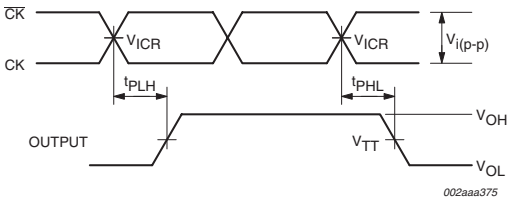
3.4 Partial-parity-out load circuit and voltage measurement information (V_{DD} = 1.8 V ± 0.1 V)

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50Ω ; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



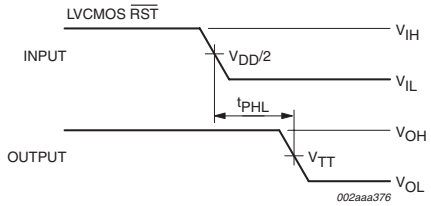
(1) C_L includes probe and jig capacitance.

Figure 32 — Partial-parity-out load circuit,



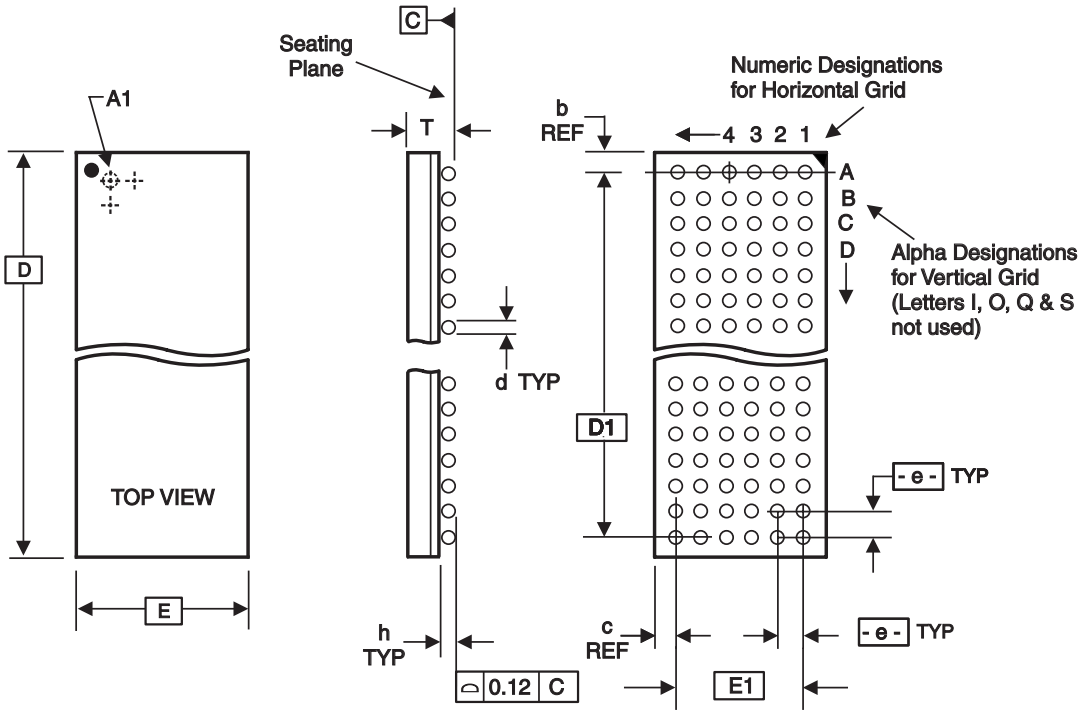
$V_{TT} = V_{DD}/2$
t_{PLH} and t_{PHL} are the same as t_{PD}.
$V_{I(PP)}$ = 600 mV

Figure 33 — Partial-parity-out voltage waveforms; propagation delay times with respect to clock inputs



$V_{TT} = V_{DD}/2$
t_{PLH} and t_{PHL} are the same as t_{PD}.
$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
$V_{IL} = V_{REF}$ - 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 34 — Partial-parity-out voltage waveforms; propagation delay times with respect to reset input



ALL DIMENSIONS IN MILLIMETERS

D	E	T	e	----- BALL GRID ----- HORIZ	VERT	Max. TOTAL	d	h	REF. DIMENSIONS b	c
		Min/Max					Min/Max	Min/Max		
13.50 Bsc	5.50 Bsc	1.20/1.40	0.80 Bsc	6	16	96	0.40/0.50	0.25/0.41	0.75	0.75
11.50 Bsc	5.00 Bsc	1.00/1.20	0.65 Bsc	6	16	96	0.35/0.45	0.25/0.35	0.875	0.875

Note: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

* Source Ref.: JEDEC Publication 95, MO-205

10-0055C

Ordering Information

ICSSSTUB32871Az(LF)T

Example:

ICS XXXX y z (LF) T

Designation for tape and reel packaging

Lead Free, RoHS Compliant (Optional)

Package Type

H = LFBGA (reduced size: 5.5 x 13.50)
HM = TFBGA (reduced size: 5.0 x 11.50)

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix

ICS = Standard Device

1186G—04/16/07

Revision History

Rev.	Issue Date	Description	Page #
B	3/20/2006	Updated Ordering Information.	17
C	2/2/2007	Applications, 2nd bullet, changed ULP877 to ULPA877A, added IDTCSPUA877A	1
D	3/1/2007	Page 1, Applications, 3rd bullet, removed 800; page 11, Electrical table, changed Idd Operating Max from 80 to 150, changed $\overline{\text{RESET}}$ Typ from 2.5 to 4.5; page 12, Timing table, changed ts (Data before...) from 0.5 to 0.6, changed th ($\overline{\text{DCS}}$, DODT...) from 0.5 t	1, 11, 12
E	3/6/2007	Timing table, th hold time, changed Q to Dn; Switching Cha. Table, fixed typos.	12
F	3/13/2007	Page 1, Recc. List, changed 3rd bullet to "Provides complete DDR DIMM solution with ICS98ULPA877A, ICS97ULP877, or IDTCSPUA877A"; page 11, fixed typos.	1, 11
G	4/16/2007	Electrical Cha. Table, changed Ci: Data Inputs max from 3.5 to 5, and CLK Max from 3 to 3.8.	11

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(Rev.1.0 Mar 2020)

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