PIN DESCRIPTION

PIN		NAME	FUNCTION
PDIP	PowerCap		
1, 30	1, 33, 34	N.C.	No Connection
2	3	A16	Address Input
3	32	A14	
4	30	A12	
5	25	A7	
6	24	A6	
7	23	A5	
8	22	A4	
9	21	A3	
10	20	A2	
11	19	A1	
12	18	A0	
25	29	A11	
26	27	A9	
27	26	A8	
28	31	A13	
13	16	DQ0	Data Input/Output
14	15	DQ1	
15	14	DQ2	
17	13	DQ3	
18	12	DQ4	
19	11	DQ5	
20	10	DQ6	
21	9	DQ7	
16	17	GND	Ground
22	8	$\overline{CE}$	Active-Low Chip Enable
23	28	A10	Address Input
24	7	$\overline{OE}$	Active-Low Output Enable
29	6	$\overline{WE}$	Active-Low Write Enable
31	2	A15	Address Input
32	5	V_{CC}	Power-Supply Input
—	4	$\overline{PFO}$	Active-Low Power-Fail Output, Open Drain. Requires a pullup resistor for proper operation.
—		X1, X2, V_{BAT}	Crystal Connection, V_{BAT} Battery Connection

DESCRIPTION

The DS1646 is a 128k x 8 nonvolatile static RAM with a full-function real time clock, which are both accessible in a byte-wide format. The nonvolatile timekeeping RAM is functionally equivalent to any JEDEC standard 128k x 8 SRAM. The device can also be easily substituted for ROM, EPROM and EEPROM, providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1646 also contains its own power-fail circuitry, which deselects the device when the V_{CC} supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

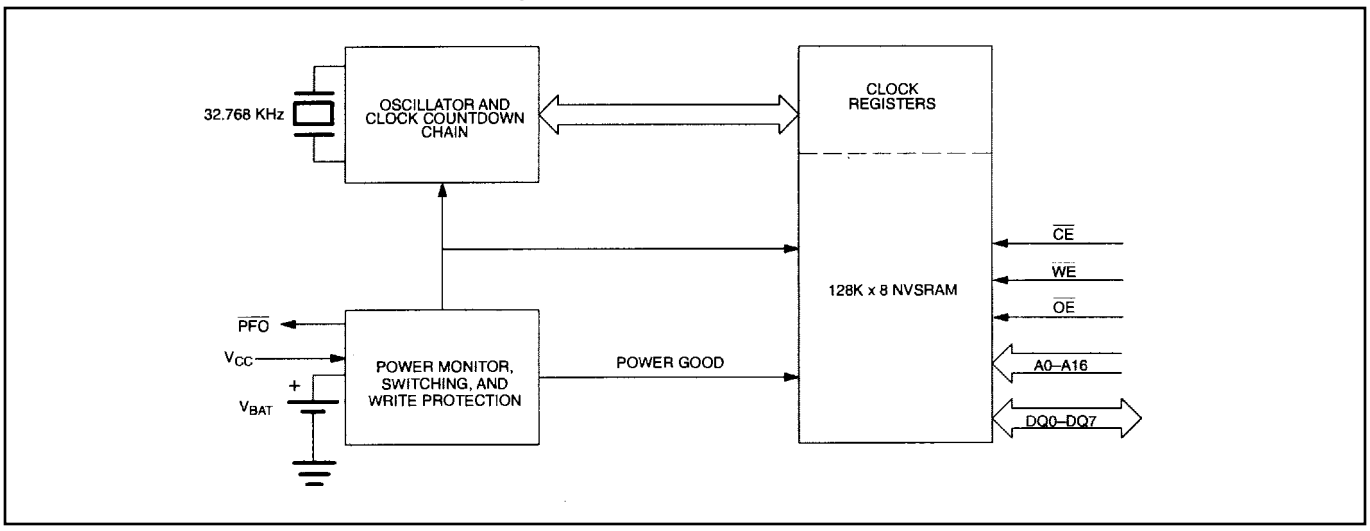
PACKAGES

The DS1646 is available in two packages: 32-pin DIP and 34-pin PowerCap module. The 32-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1646P after the completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers. The part number for the PowerCap is DS9034PCX.

CLOCK OPERATIONS—READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1646 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the 7th most significant bit in the control register. As long as 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was present at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that clock accuracy is not affected by the access of data. All of the DS1646 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to 0.

BLOCK DIAGRAM DS1646 Figure 1



TRUTH TABLE DS1646 Table 1

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5V ± 10%	V_{IH}	X	X	DESELECT	HIGH-Z	STANDBY
	X	X	X	DESELECT	HIGH-Z	STANDBY
	V_{IL}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	READ	HIGH-Z	ACTIVE
<4.5V >V_{BAT}	X	X	X	DESELECT	HIGH-Z	CMOS STANDBY
<V_{BAT}	X	X	X	DESELECT	HIGH-Z	DATA RETENTION MODE

SETTING THE CLOCK

The MSB Bit, B7, of the control register is the write bit. Setting the write bit to a 1, like the read bit halts updates to the DS1646 registers. The user can then load them with the correct day, date and time data in 24-hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the second's registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the second's register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, and address for seconds register remain valid and stable).

CLOCK ACCURACY (DIP MODULE)

The DS1646 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The RTC is calibrated at the factory by Dallas Semiconductor using nonvolatile tuning elements, and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. Clock accuracy is also affected by the electrical environment and caution should be taken to place the RTC in the lowest level EMI section of the PCB layout. For additional information refer to Application Note 58.

CLOCK ACCURACY (POWERCAP MODULE)

The DS1646 and DS9034PCX are each individually tested for accuracy. Once mounted together, the module will typically keep time accuracy to within ±1.53 minutes per month (35 ppm) at 25°C. Clock accuracy is also affected by the electrical environment and caution should be taken to place the RTC in the lowest level EMI section of the PCB layout. For additional information refer to Application Note 58.

1646 REGISTER MAP—BANK1 Table 2

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1FFFF	—	—	—	—	—	—	—	—	Year	00–99
1FFFE	X	X	X	—	—	—	—	—	Month	01–12
1FFFD	X	X	-	—	—	—	—	—	Date	01–31
1FFFC	X	FT	X	X	X	—	—	—	Day	01–07
1FFFB	X	X	—	—	—	—	—	—	Hour	00–23
1FFFA	X	—	—	—	—	—	—	—	Minutes	00–59
1FFF9	$\overline{OSC}$	—	—	—	—	—	—	—	Seconds	00–59
1FFF8	W	R	X	X	X	X	X	X	Control	A

$\overline{OSC}$ = Stop Bit R = Read Bit FT = Frequency Test
W = Write Bit X = Unused

Note: *All indicated "X" bits are unused but must be set to "0" during write cycles to ensure proper clock operation.*

RETRIEVING DATA FROM RAM OR CLOCK

The DS1646 is in the read mode whenever $\overline{WE}$ (write enable) is high; $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NVSRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip-enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1646 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring high to low transition of $\overline{WE}$ and $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CC} is within nominal limits (V_{CC} > 4.5 volts) the DS1646 can be accessed as described above with read or write cycles. However, when V_{CC} is below the power-fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM are blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. At this time the power-fail output signal ($\overline{PFO}$) will be driven active low and will remain active until V_{CC} returns to nominal levels. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +6.0V
Storage Temperature Range
EDIP.....…….....……-40°C to +85°C
PowerCap.....…….....……-55°C to +125°C
Lead Temperature (soldering, 10s) ……..... +260°C
Note: EDIP is wave or hand soldered only.
Soldering Temperature (reflow, PowerCap) ..... +260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C, Noncondensing	5V ±10%

RECOMMENDED DC OPERATING CONDITIONS (Over the Operating Range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS (Over the Operating Range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}			85	mA	2, 3
TTL Standby Current ($\overline{CE}$ =V_{IH})	I_{CC2}		3	6	mA	2, 3
CMOS Standby Current ($\overline{CE}$ =V_{CC}-0.2V)	I_{CC3}		2	4.0	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Power-Fail Voltage	V_{PF}	4.0	4.25	4.5	V	

AC ELECTRICAL CHARACTERISTICS (Over the Operating Range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
Address Access Time	t_{AA}			120	ns	
$\overline{CE}$ Access Time	t_{CEA}			120	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			40	ns	
Output Enable Access Time	t_{OEA}			100	ns	
Output Enable Data Off Time	t_{OEZ}			40	ns	
Output Enable to DQ Low-Z	t_{OEL}	5			ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
Output Hold from Address	t_{OH}	5			ns	
Write Cycle Time	t_{WC}	120			ns	
Address Setup Time	t_{AS}	0			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	100			ns	
Address Hold from End of Write	t_{AH1}	5			ns	5
	t_{AH2}	30			ns	6
Write Pulse Width	t_{WEW}	75			ns	
$\overline{WE}$ Data Off Time	t_{WEZ}			40	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10			ns	
Data Setup Time	t_{DS}	85			ns	
Data Hold Time High	t_{DH1}	0			ns	5
	t_{DH2}	25			ns	6

AC TEST CONDITIONS

Input Levels: 0V to 3V
Transition Times: 5 ns

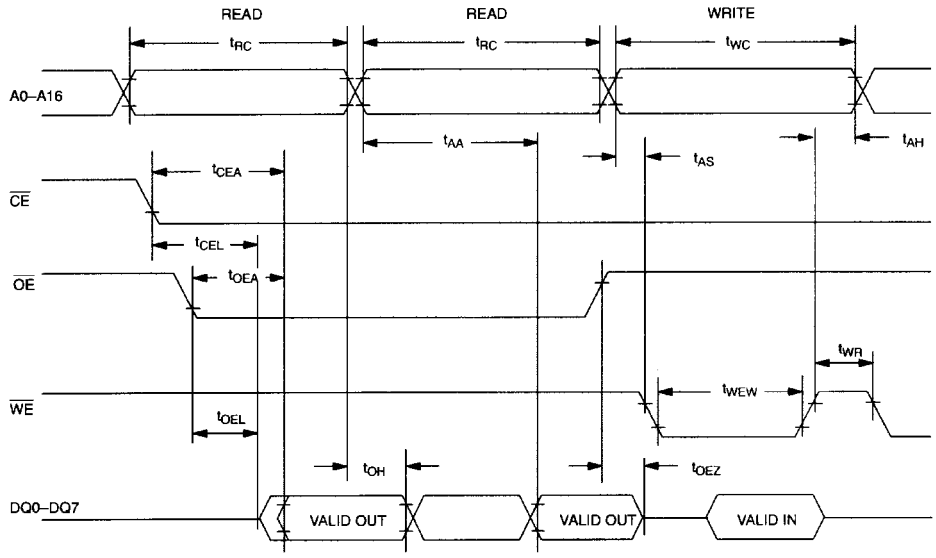
CAPACITANCE (T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Pins (except DQ)	C_I			7	pF	
Capacitance on DQ Pins	C_{DQ}			10	pF	

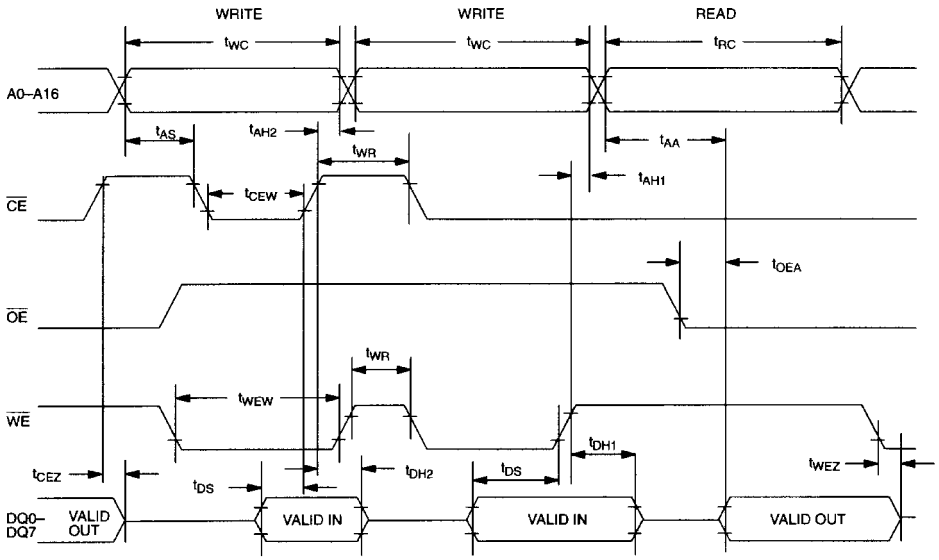
AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (Over the Operating Range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{SO} to V_{PF} (Min) V_{CC} Rise Time	t_{RB}	1			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power-Up	t_{REC}	15		35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4

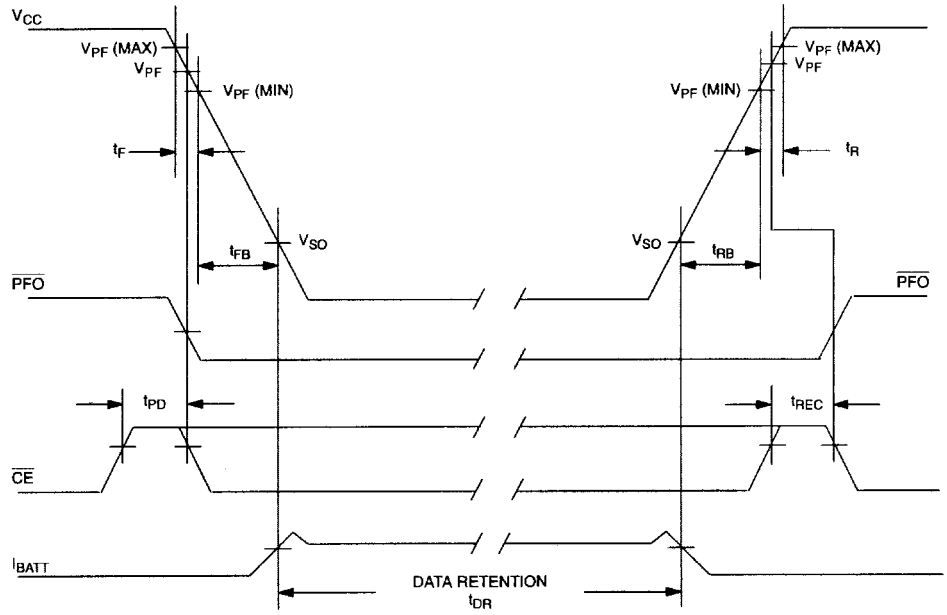
DS1646 READ CYCLE TIMING



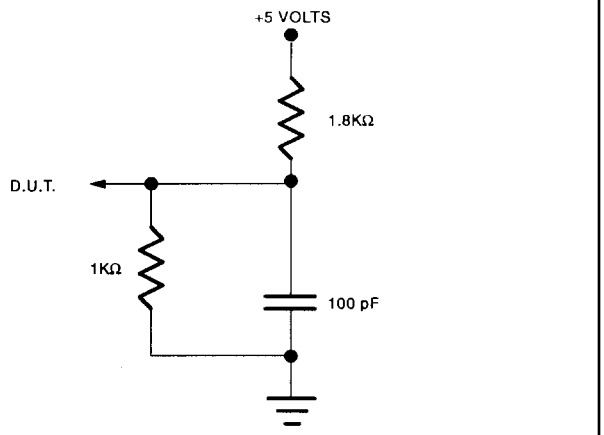
DS1646 WRITE CYCLE TIMING



POWER-DOWN/POWER-UP TIMING



OUTPUT LOAD



NOTES:

1) All voltages are referenced to ground.
2) Typical values are at 25°C and nominal supplies.
3) Outputs are open.
4) Data retention time is at 25°C and is calculated from the date code on the device package. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225 would mean the 25th week of 1992.
5) t_{AH1}, t_{DH1} are measured from $\overline{WE}$ going high.
6) t_{AH2}, t_{DH2} are measured from $\overline{CE}$ going high.
7) Real-Time Clock Modules (EDIP) can be successfully processed through conventional wave-soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.

   In addition, for the PowerCap version:
   a. Dallas Semiconductor recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up ("live-bug").
   b. Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows and use a solder wick to remove solder.

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 EDIP	MDF32+1	**21-0245**	—
34 PCAP	PC2+6	**21-0246**	—

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
10/10	Updated the *Ordering Information* table; updated the storage, lead, and soldering information in the *Absolute Maximum Ratings* section	1, 7

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

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