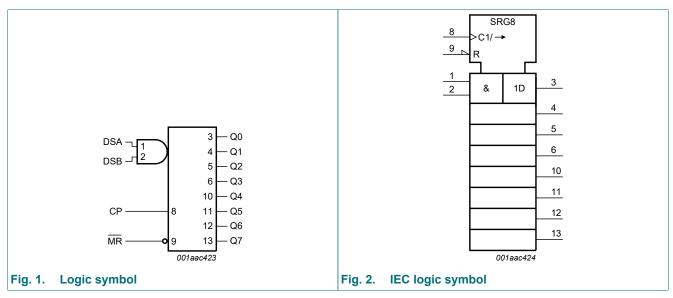
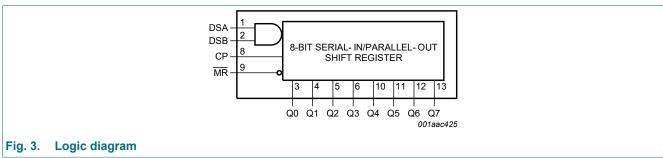
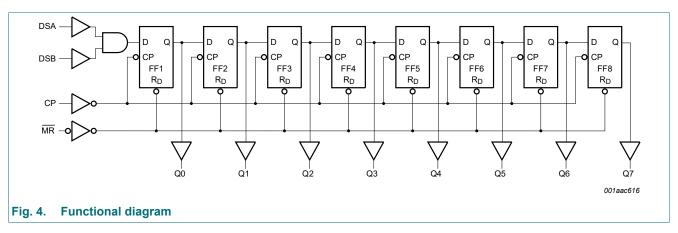
4. Functional diagram

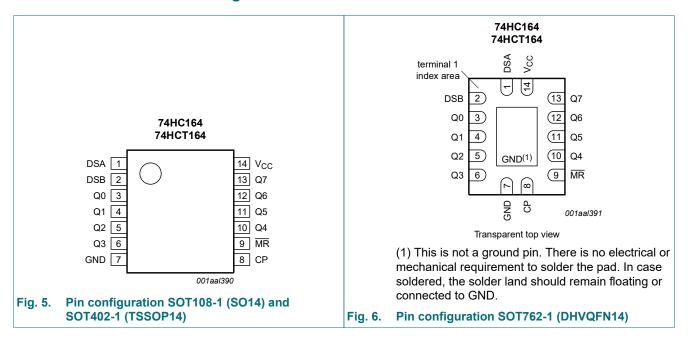






5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Complete	Dim	Description
Symbol	Pin	Description
DSA	1	data input
DSB	2	data input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	3, 4, 5, 6, 10, 11, 12, 13	output
GND	7	ground (0 V)
CP	8	clock input (LOW-to-HIGH, edge-triggered)
MR	9	master reset input (active LOW)
V _{CC}	14	positive supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition

↑ = LOW-to-HIGH clock transition; X = don't care

Operating	Input		Output	Output			
modes	MR	СР	DSA DSB Q0 X X L I I L I h L h I L	Q1 to Q7			
Reset (clear)	L	X	Х	X	L	L to L	
Shift	Н	1	I	I	L	q0 to q6	
	Н	1	I	h	L	q0 to q6	
	Н	1	h	I	L	q0 to q6	
	Н	1	h	h	Н	q0 to q6	

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_1 < -0.5 \text{ V or } V_1 > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For SOT402-1 (TSSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	•	74HC164	4	7	Unit		
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

^[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC16	4									
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μA
Cı	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT1	64									
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V

Symbol	Parameter	Conditions		25 °C		-40 ° +85		-40 ° +12	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
Iı	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8	-	80	-	160	μΑ
ΔI _{CC}	additional supply current	per input pin; $V_1 = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	100	360	-	450	-	490	μА
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; test circuit see Fig. 10; unless otherwise specified

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	-40 ° +12	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
74HC16	4		'							
t _{pd}	propagation	CP to Qn; see Fig. 7]							
	delay	V _{CC} = 2.0 V	-	41	170	-	215	-	255	ns
		V _{CC} = 4.5 V	-	15	34	-	43	-	51	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	12	29	-	37	-	43	ns
t _{PHL}	propagation									
	propagation delay	V _{CC} = 2.0 V	-	39	140	-	175	-	210	ns
	delay	V _{CC} = 4.5 V	-	14	28	-	35	-	42	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	11	24	-	30	-	36	ns
t _t	transition time	see Fig. 7	2]							
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _W	pulse width	CP HIGH or LOW; see Fig. 7								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	-	ns
		MR LOW; see Fig. 8								
		V _{CC} = 2.0 V	60	17	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	6	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	5	-	13	-	15	-	ns

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
t _{rec}	recovery time	MR to CP; see Fig. 8								
		V _{CC} = 2.0 V	60	17	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	6	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	5	-	13	-	15	-	ns
t _{su}	set-up time	DSA, and DSB to CP; see Fig. 9								
		V _{CC} = 2.0 V	60	8	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	3	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	2	-	13	-	15	-	ns
t _h	hold time	DSA, and DSB to CP; see Fig. 9								
		V _{CC} = 2.0 V	+4	-6	-	4	-	4	-	ns
		V _{CC} = 4.5 V	+4	-2	-	4	-	4	-	ns
		V _{CC} = 6.0 V	+4	-2	-	4	-	4	-	ns
f _{max}	maximum	for Cp, see Fig. 7								
	frequency	V _{CC} = 2.0 V	6	23	-	5	-	4	-	MHz
		V _{CC} = 4.5 V	30	71	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	78	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	85	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	per package; $V_I = GND$ to V_{CC} [3]	-	40	-	-	-	-	-	pF
74HCT1	64									
t _{pd}	propagation	CP to Qn; see Fig. 7 [1]								
	delay	V _{CC} = 4.5 V	-	17	36	-	45	-	54	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	14	-	-	-	-	-	ns
t _{PHL}	HIGH to LOW	MR to Qn; see Fig. 8								
	propagation	V _{CC} = 4.5 V	-	19	38	-	48	-	57	ns
	delay	V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
t _t	transition time	see Fig. 7 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _W	pulse width	CP HIGH or LOW; see Fig. 7								
		V _{CC} = 4.5 V	18	7	-	23	-	27	-	ns
		MR LOW; see Fig. 8								
		V _{CC} = 4.5 V	18	10	_	23	-	27	-	ns
t _{rec}	recovery time	MR to CP; see Fig. 8								
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
t _{su}	set-up time	DSA, and DSB to CP; see Fig. 9								
54		V _{CC} = 4.5 V	12	6	-	15	-	18	-	ns
t _h	hold time	DSA, and DSB to CP; see Fig. 9	_	-						
		$V_{CC} = 4.5 \text{ V}$			_	4	_	4		ns

Symbol	Parameter	Conditions			25 °C		_	°C to 5 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max		
f _{max}	maximum	for Cp, see Fig. 7									
	frequency	V _{CC} = 4.5 V		27	55	-	22	-	18	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF		-	61	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V	[3]	-	40	-	-	-	-	-	pF

- $\begin{array}{ll} [1] & t_{pd} \text{ is the same as } t_{PHL} \text{ and } t_{PLH}. \\ [2] & t_{t} \text{ is the same as } t_{THL} \text{ and } t_{TLH}. \\ [3] & C_{PD} \text{ is used to determine the dynamic power dissipation } (P_{D} \text{ in } \mu \text{W}): \end{array}$

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

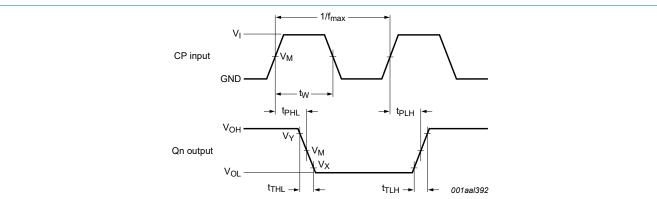
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

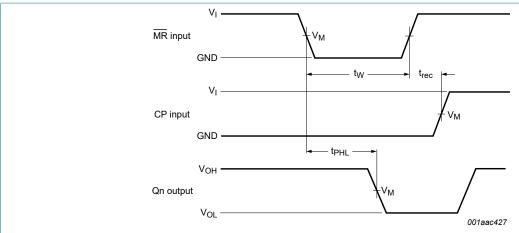
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

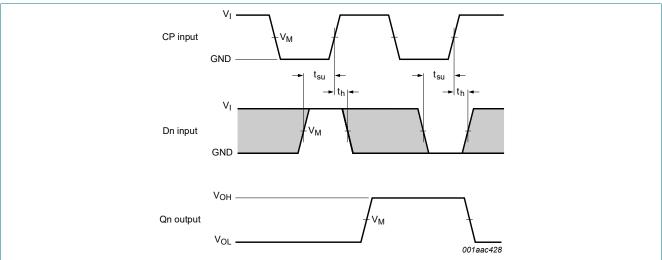
Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Waveforms showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (CP) removal time



Measurement points are given in Table 8.

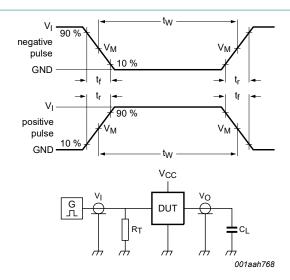
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 9. Waveforms showing the data set-up and hold times for Dn inputs

Table 8. Measurement points

Туре	Input	Output						
	V _M	V _M	V _X	V _Y				
74HC164	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}				
74HCT164	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}				



Test data is given in Table 9.

Definitions test circuit:

 R_{T} = termination resistance should be equal to output impedance Z_{o} of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

Fig. 10. Test circuit for measuring switching times

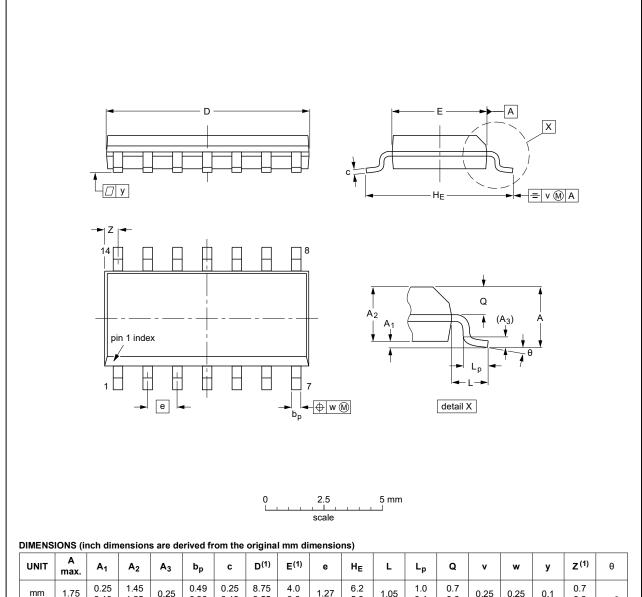
Table 9. Test data

Туре	Input		Load	Test
	V _I	t _r , t _f	C _L	
74HC164	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT164	3.0 V	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



	UNIT	A max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	q	v	w	у	Z ⁽¹⁾	θ
	mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
iı	nches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

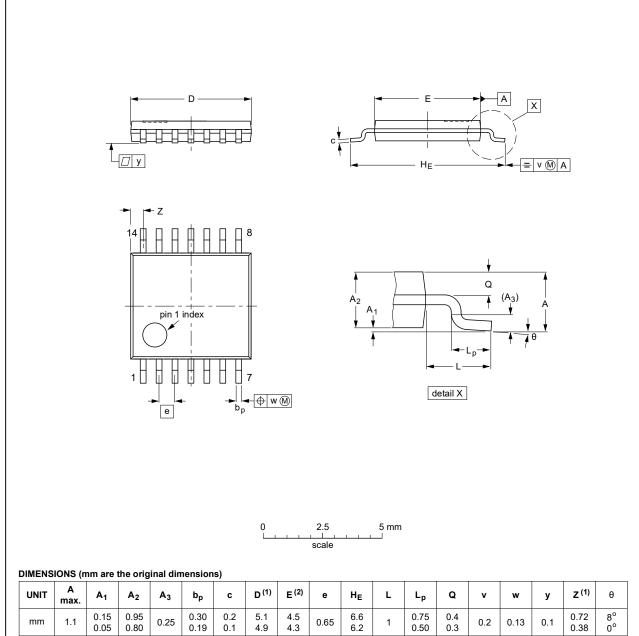
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

Fig. 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



	IIIax.																	
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT402-1		MO-153				99-12-27 03-02-18	

Fig. 12. Package outline SOT402-1 (TSSOP14)

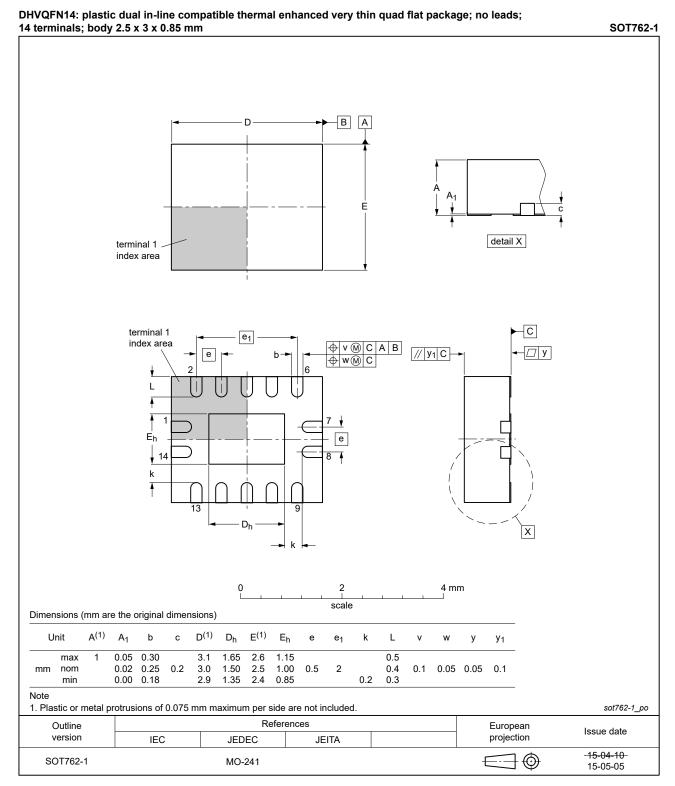


Fig. 13. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT164 v.10	20210901	Product data sheet	-	74HC_HCT164 v.9
Modifications:	Type number	ers 74HC164DB and 74HC	T164DB (SOT33	7-1/SSOP14) removed.
74HC_HCT164 v.9	20200611	Product data sheet	-	74HC_HCT164 v.8
Modifications:	guidelines o Legal texts	of this data sheet has been of Nexperia. have been adapted to the rating values for P _{tot} total p	new company nar	ne where appropriate.
74HC_HCT164 v.8	20151119	Product data sheet	-	74HC_HCT164 v.7
Modifications:	Type number	ers 74HC164N and 74HCT	164N (SOT27-1)	removed.
74HC_HCT164 v.7	20130613	Product data sheet	-	74HC_HCT164 v.6
Modifications:	General des	scription updated.		
74HC_HCT164 v.6	20111212	Product data sheet	-	74HC_HCT164 v.5
Modifications:	Legal page:	s updated.		
74HC_HCT164 v.5	20101125	Product data sheet	-	74HC_HCT164 v.4
74HC_HCT164 v.4	20100202	Product data sheet	-	74HC_HCT164 v.3
74HC_HCT164 v.3	20050404	Product data sheet	-	74HC_HCT164_ CNV v.2
74HC_HCT164_CNV v.2	19901201	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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