

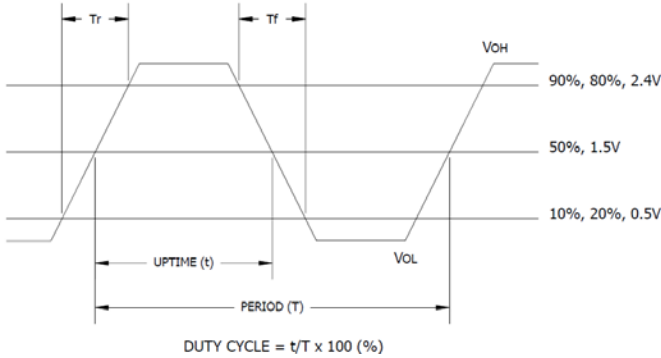
ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Maximum Supply Voltage	V _{CC}	-	-0.5	-	+7.0	V	
Storage Temperature	T _{STG}	-	-40	-	+100	°C	
Frequency Range	f ₀	-	1.5	-	107	MHz	
CB3LV		-	1.5	-	200		
Frequency Stability	Δf/f ₀	See Note 1 and Ordering Information	-	-	20,25,50 or 100	± ppm	
Aging	Δf	First year	-	3	5	± ppm	
Operating Temperature	T _A	-	-20	25	+70	°C	
Commercial Industrial		-	-40	-	+85		
Supply Voltage	V _{CC}	±10%	4.5	5.0	5.5	V	
CB3 CB3LV		-	3.0	3.3	3.6		
Supply Current	I _{CC}	Frequency Range				mA	
CB3		Tested load condition noted for typical values.					
		1.5MHz to 20MHz	C _L =50pF	-	10		25
		20.001MHz to 80MHz	C _L =50pF	-	30		50
CB3LV		80.001MHz to 107MHz	C _L =15pF	-	40		80
		1.5MHz to 20MHz	C _L =15pF	-	7		12
	20.001MHz to 80MHz	C _L =15pF	-	20	40		
Output Load	C _L	80.001MHz to 200MHz	C _L =15pF	-	30	pF	
		1.5MHz to 50MHz	-	-	50		
		50.001MHz to 80MHz	-	-	30		
Output Voltage Levels	V _{OH} V _{OL}	CMOS Load	90%V _{CC}	-	-	V	
		10 TTL LOAD	V _{CC} -0.6V	-	-		
Logic '0' Level	V _{OL}	CMOS	-	-	10%V _{CC}	0.4	
		TTL Load	-	-	-		
Output Current	I _{OH} I _{OL}	V _{OH} = 3.9V/2.2V	V _{CC} = 4.5V/3.0V	-	-	mA	
Logic '1' Level		V _{OL} = 0.4V	V _{CC} = 4.5V/3.0V	-	-		
Logic '0' Level	I _{OL}	-	-	-	+16/+8		
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%	
Rise and Fall Time	T _R , T _F	@ 10% - 90% Levels				ns	
CB3		Tested load condition noted for typical values.					
		1.5MHz to 20MHz	C _L =50pF	-	8		10
		20.001MHz to 80MHz	C _L =50pF	-	5		8
CB3LV		80.001MHz to 200MHz	C _L =15pF	-	2.5		5
		1.5MHz to 20MHz	C _L =15pF	-	6		8
	20.001MHz to 80MHz	C _L =15pF	-	3	5		
80.001MHz to 200MHz	C _L =15pF	-	1.5	3			
Start Up Time	T _S	Application of V _{CC}	-	-	10	ms	
Enable Function	V _{IH} V _{IL}	Pin 1 Logic '1', Output Enabled	2.0	-	-	V	
Enable Input Voltage		Pin 1 Logic '0', Output Disabled	-	-	0.8		
Disable Input Voltage	V _{IL}	-	-	-	-		
Enable Time	T _{PLZ}	Pin 1 Logic '1'	-	-	200	ns	
Standby Current	I _{ST}	Pin 1 Logic '0', Output Disabled	-	-	10	μA	
Period Jitter, Pk-Pk	-	-	-	-	50		
Period Jitter, RMS	-	-	-	-	5	ps	
Phase Jitter, RMS	-	Bandwidth 12kHz - 20MHz	-	-	1		

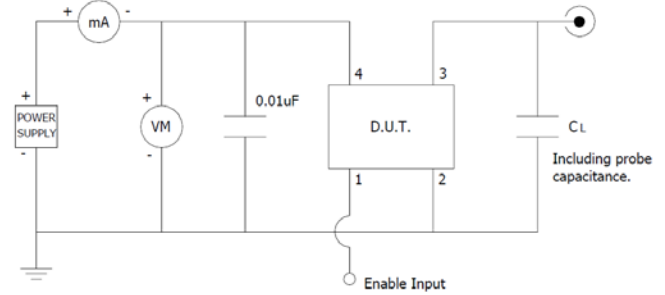
- Notes:
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

ELECTRICAL CHARACTERISTICS

LVC MOS OUTPUT WAVEFORM



TEST CIRCUIT, CMOS LOAD



ENABLE TRUTH TABLE

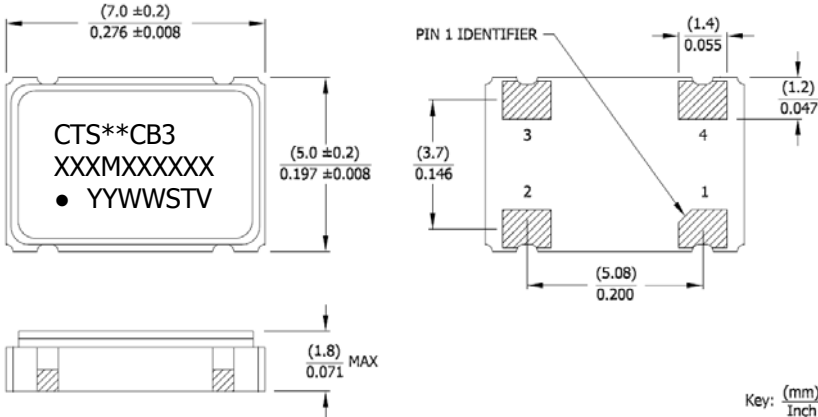
PIN 1	PIN 3
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V _{CC}	Supply Voltage

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

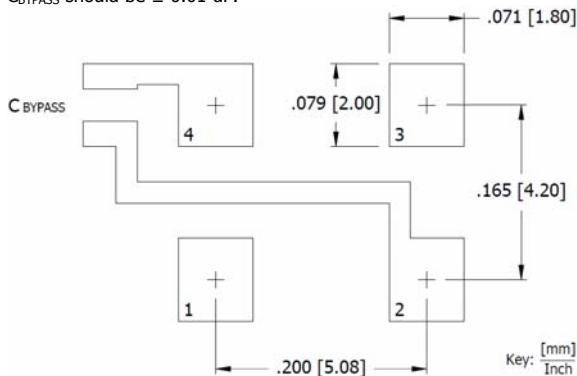
- ** – Manufacturing Site Code.
[Note a dash may follow the site code and is acceptable.]
- XXXMXXXXXX – Frequency is marked with only leading significant digits before the 'M' and 4 – 6 digits after the 'M' (including zeros).
Ex. XMXXXXXX [3M579545]
XXMXXXXXX [14M31818]
XXXMXXXXXX [125M0000]
- YYWW – Date code, YY – year, WW – week.
- ST – Frequency stability/temperature code.
[Refer to Ordering Information.]
- V – Voltage code. 3 = 3.3V, 5 = 5.0V.

NOTES

- Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020, 260°C maximum.
- Moisture Sensitivity Level 1 per JEDEC J-STD-020.

SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be ≥ 0.01 uF.



Mouser Electronics

Authorized Distributor

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CTS:

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[CB3LV-3C-24M000000](#) [CB3-3C-33M333000](#) [CB3LV-3C-10M000000](#) [CB3LV-3C-16M384000](#) [CB3-3C-12M000000](#)
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[45M000000](#) [CB3-3C-20M000000](#) [CB3-3C-60M000000](#) [CB3-3C-10M000000](#) [CB3LV-3C-45M000000](#) [CB3-3C-](#)
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[33M0000](#) [CB3LV-3I-24M5760](#) [CB3LV-3I-125M0000](#) [CB3LV-3I-66M0000](#) [CB3LV-3I-33M3333](#) [CB3LV-3I-27M0000](#)
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