

High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC} to V _{EE})	12V	8-Pin μ MAX (derate 4.1mW/°C above +70°C)	330mW
IN ₋ , IN ₊ , OUT ₋ , EN ₋	(V _{EE} - 0.3V) to (V _{CC} + 0.3V)	14-Pin SO (derate 8.3mW/°C above +70°C)	667mW
Output Short-Circuit Duration to V _{CC} or V _{EE}	Continuous	16-Pin QSOP (derate 8.3mW/°C above +70°C)	667mW
Continuous Power Dissipation (T _A = +70°C)		Operating Temperature Range	-40°C to +85°C
5-Pin SOT23 (derate 7.1mW/°C above +70°C)	571mW	Storage Temperature Range	-65°C to +150°C
8-Pin SO (derate 5.9mW/°C above +70°C)	471mW	Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = 0, IN₋ = 0, EN₋ = 5V, R_L = ∞ to 0, V_{OUT} = V_{CC}/2, noninverting configuration, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range		V _{CC} to V _{EE} , guaranteed by PSRR tests		3.15		11.0	V
Input Voltage Range	V _{IN}	IN ₊		V _{EE} - 0.1		V _{CC} - 2.25	V
		IN ₋		V _{EE} - 0.1		V _{CC} + 0.1	
Input Offset Voltage	V _{OS}	R _L = 50 Ω	SO, QSOP		4	10	mV
			SOT23-5, μ MAX		4	15	
Input Offset Voltage Drift	TCV _{OS}				8		μ V/°C
Input Offset Voltage Matching		Between any two channels for MAX4217/MAX4219/MAX4222			1		mV
Input Bias Current	I _B	IN ₊			5.4	12	μ A
Input Resistance	R _{IN}	IN ₊ , over input voltage range			3		M Ω
Voltage Gain	A _v	R _L \geq 50 Ω , (V _{EE} + 0.5V) \leq V _{OUT} \leq (V _{CC} - 2.0V)		1.9	2	2.1	V/V
Power-Supply Rejection Ratio (Note 2)	PSRR	V _{CC} = 5V, V _{EE} = 0, V _{OUT} = 2.0V		55	58		dB
		V _{CC} = 5V, V _{EE} = -5V, V _{OUT} = 0		60	66		
		V _{CC} = 3.3V, V _{EE} = 0, V _{OUT} = 0.90V			45		
Output Resistance	R _{OUT}	f = DC			25		m Ω
Output Current	I _{OUT}	R _L = 20 Ω to V _{CC} or V _{EE}	T _A = +25°C	\pm 70	\pm 120		mA
			T _A = T _{MIN} to T _{MAX}	\pm 60			
Short-Circuit Output Current	I _{SC}	Sinking or sourcing			\pm 150		mA
Output Voltage Swing	V _{OUT}	R _L = 50 Ω	V _{CC} - V _{OH}		1.60	1.90	V
			V _{OL} - V _{EE}		0.04	0.075	
		R _L = 150 Ω	V _{CC} - V _{OH}		0.75	1.00	
			V _{OL} - V _{EE}		0.04	0.075	
		R _L = 2k Ω	V _{CC} - V _{OH}		0.06		
			V _{OL} - V _{EE}		0.06		
Disabled Output Resistance	R _{OUT(OFF)}	MAX4215/MAX4219, EN ₋ = 0, 0 \leq V _{OUT} \leq 5V			1		k Ω
EN ₋ Logic Low Threshold	V _{IL}	MAX4215/MAX4219			V _{CC} - 2.6		V
EN ₋ Logic High Threshold	V _{IH}	MAX4215/MAX4219		V _{CC} - 1.6			V

High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

MAX4214/MAX4215/MAX4217/MAX4219/MAX4222

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 5V$, $V_{EE} = 0$, $I_{N-} = 0$, $E_{N-} = 5V$, $R_L = \infty$ to 0 , $V_{OUT} = V_{CC}/2$, noninverting configuration, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN_ Logic Input Low Current	I_{IL}	MAX4215/MAX4219, $(V_{EE} + 0.2V) \leq E_{N-} \leq V_{CC}$		0.5		μA
		MAX4215/MAX4219, $E_{N-} = V_{EE}$		200	350	
EN_ Logic Input High Current	I_{IH}	MAX4215/MAX4219, $E_{N-} = V_{CC}$		0.5	10	μA
Quiescent Supply Current (per Buffer)	I_{CC}			5.5	7.0	mA
Shutdown Supply Current	I_{SD}	MAX4215/MAX4219, disabled ($E_{N-} = V_{EE}$)		400	550	μA

Note 1: The MAX421_EU_ is 100% production tested at $T_A = 25^{\circ}C$. Specifications over temperature limits are guaranteed by design.

Note 2: PSRR for single 5V supply tested with $V_{EE} = 0$, $V_{CC} = 4.5V$ to $5.5V$; for dual $\pm 5V$ supply with $V_{EE} = -4.5V$ to $-5.5V$, $V_{CC} = 4.5V$ to $5.5V$; and for single 3V supply with $V_{EE} = 0$, $V_{CC} = 3.15V$ to $3.45V$.

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V$, $V_{EE} = 0$, $I_{N-} = 0$, $E_{N-} = 5V$, $R_L = 100\Omega$ to $V_{CC}/2$, noninverting configuration, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW-3dB	$V_{OUT} = 100mV_{P-P}$	MAX4214/MAX4215/MAX4217		230		MHz
			MAX4219/MAX4222		200		
Full-Power -3dB Bandwidth	FPBW	$V_{OUT} = 2V_{P-P}$	MAX4214/MAX4215/MAX4217		220		MHz
			MAX4219/MAX4222		200		
Bandwidth for 0.1dB Gain Flatness	BW _{0.1dB}	$V_{OUT} = 100mV_{P-P}$	MAX4214/MAX4215/MAX4217		50		MHz
			MAX4219/MAX4222		90		
Slew Rate	SR	$V_{OUT} = 2V$ step			600		V/ μs
Settling Time to 0.1%	t_S	$V_{OUT} = 2V$ step			45		ns
Rise/Fall Time	t_R, t_F	$V_{OUT} = 100mV_{P-P}$			1		ns
Spurious-Free Dynamic Range	SFDR	$f_C = 5MHz$, $V_{OUT} = 2V_{P-P}$			-72		dBc
Harmonic Distortion	HD	$V_{OUT} = 2V_{P-P}$, $f_C = 5MHz$	Second harmonic		-72		dBc
			Third harmonic		-77		
			Total harmonic distortion		-71		
Third-Order Intercept	IP3	$f = 10MHz$			35		dBm
Input 1dB Compression Point		$f = 10MHz$			11		dBm
Differential Phase Error	DP	NTSC, $R_L = 150\Omega$			0.04		degrees
Differential Gain Error	DG	NTSC, $R_L = 150\Omega$			0.03		%
Input Noise-Voltage Density	e_n	$f = 10kHz$			10		nV/\sqrt{Hz}
Input Noise-Current Density	i_n	$f = 10kHz$			1.3		pA/\sqrt{Hz}
Input Capacitance	C_{IN}				1		pF
Disabled Output Capacitance	$C_{OUT(OFF)}$	MAX4215/MAX4219, $E_{N-} = 0$			2		pF

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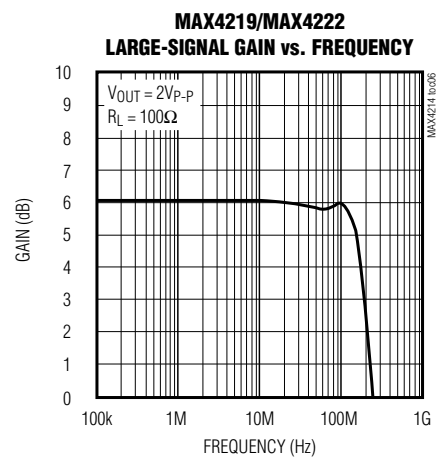
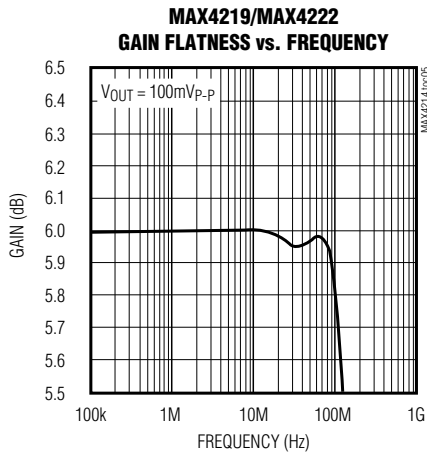
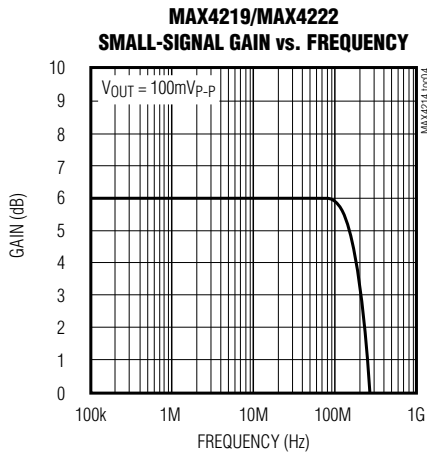
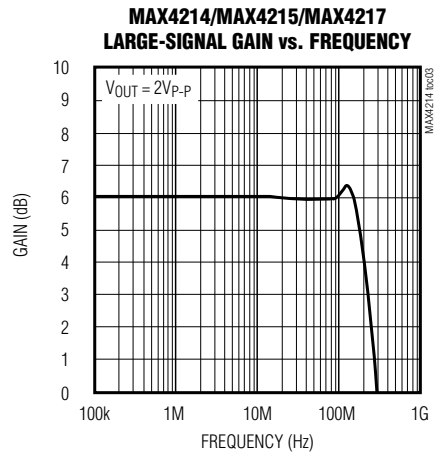
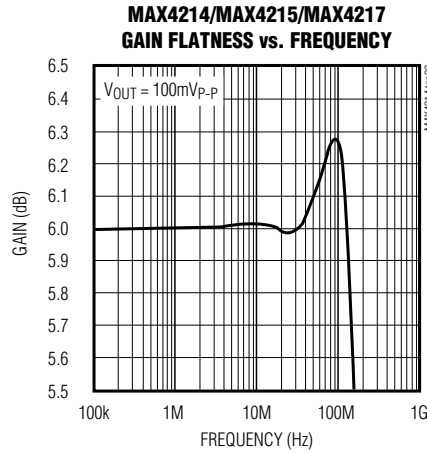
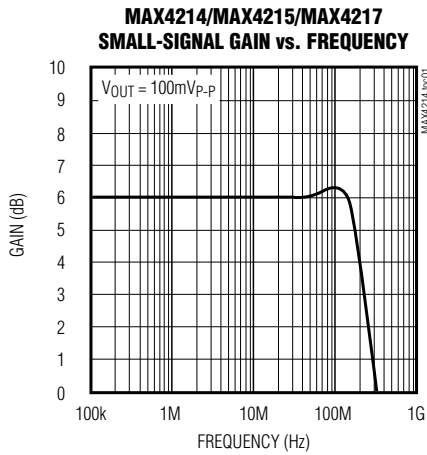
AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 5V$, $V_{EE} = 0$, $IN_- = 0$, $EN_- = 5V$, $R_L = 100\Omega$ to $V_{CC}/2$, noninverting configuration, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_{OUT}	$f = 10MHz$		200		$m\Omega$
Buffer Enable Time	t_{ON}	MAX4215/MAX4219		100		ns
Buffer Disable Time	t_{OFF}	MAX4215/MAX4219		1		μs
Buffer Gain Matching		MAX4217/MAX4219/MAX4222, $f = 10MHz$, $V_{OUT} = 100mV_{P-P}$		0.1		dB
All-Hostile Crosstalk	XTALK	MAX4217/MAX4219/MAX4222, $f = 10MHz$, $V_{OUT} = 2V_{P-P}$		-95		dB

Typical Operating Characteristics

($V_{CC} = 5V$, $V_{EE} = 0$, $A_{VCL} = 2V/V$, $R_L = 100\Omega$ to $V_{CC}/2$, $T_A = +25^\circ C$, unless otherwise noted.)

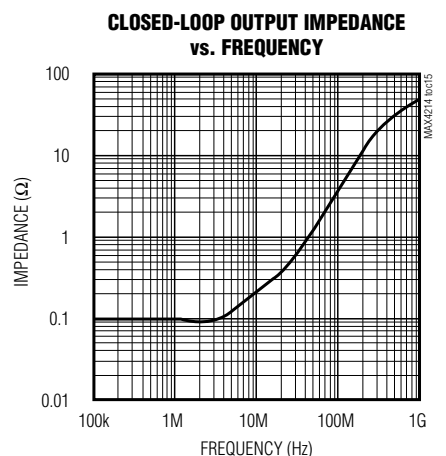
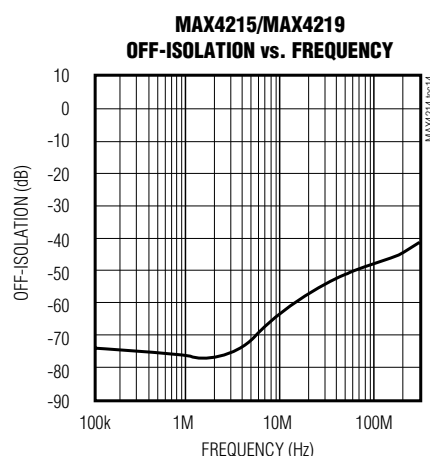
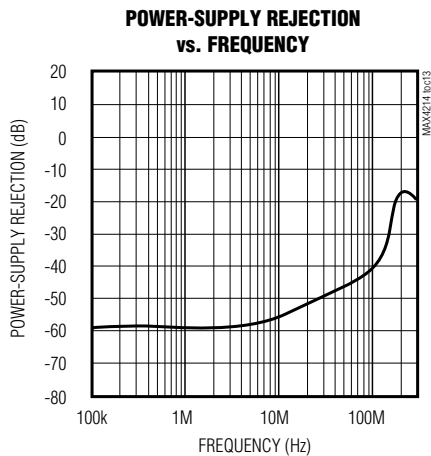
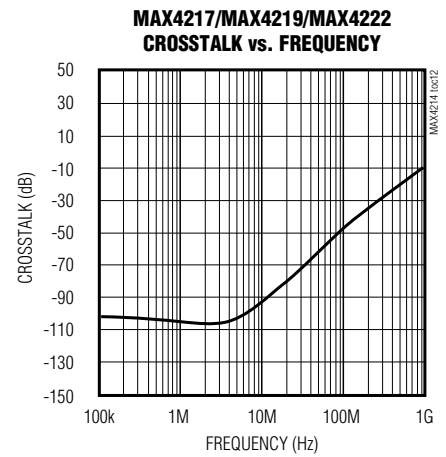
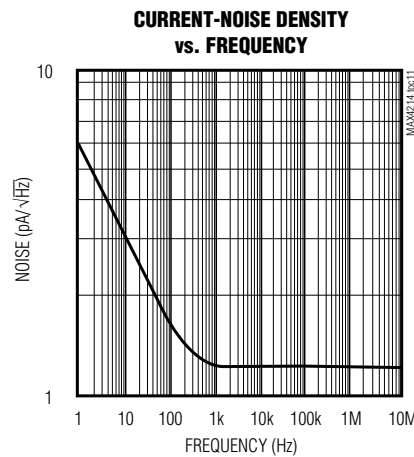
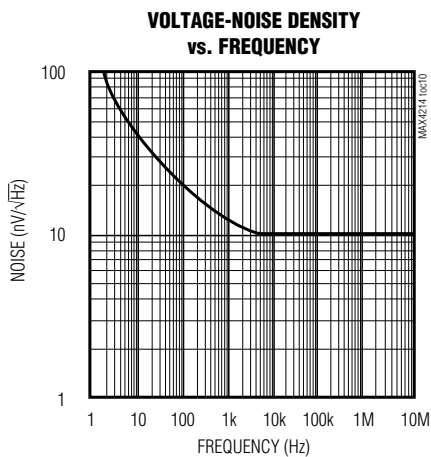
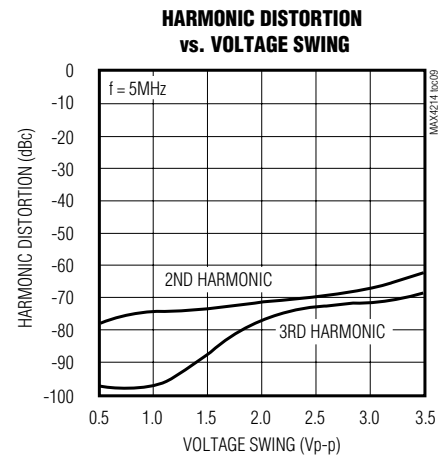
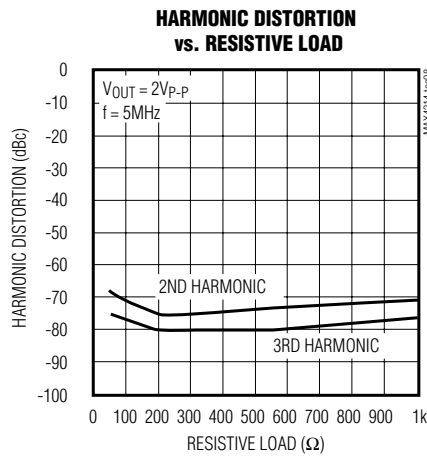
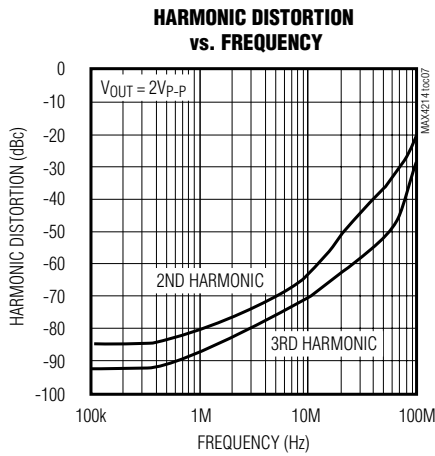


High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

Typical Operating Characteristics (continued)

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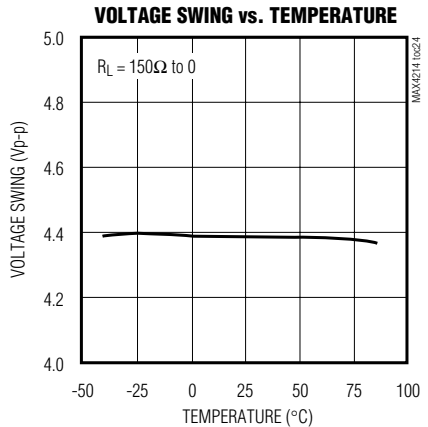
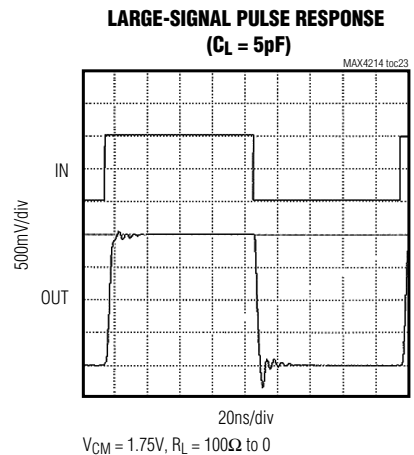
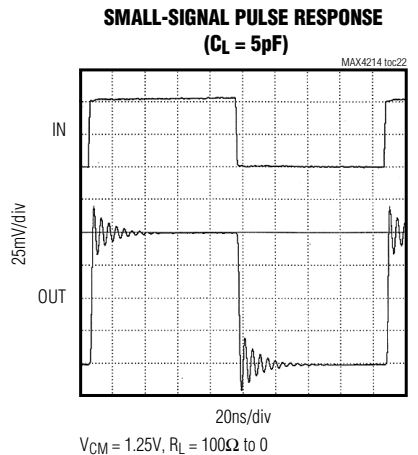
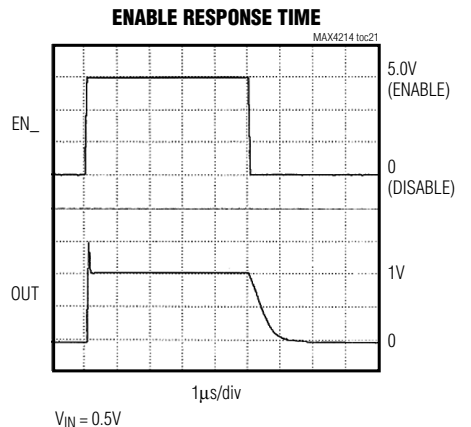
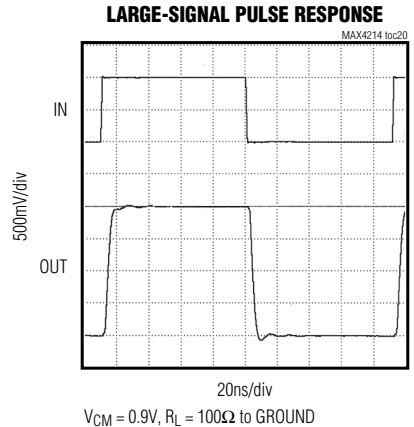
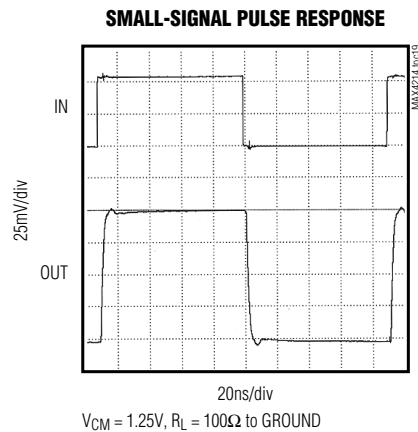
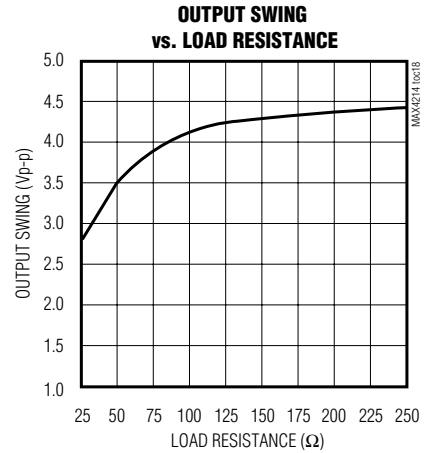
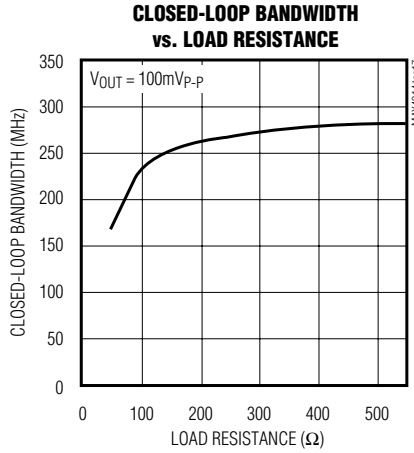
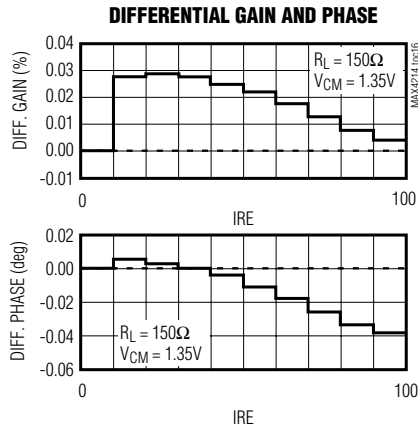
MAX4214/MAX4215/MAX4217/MAX4219/MAX4222



High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

Typical Operating Characteristics (continued)

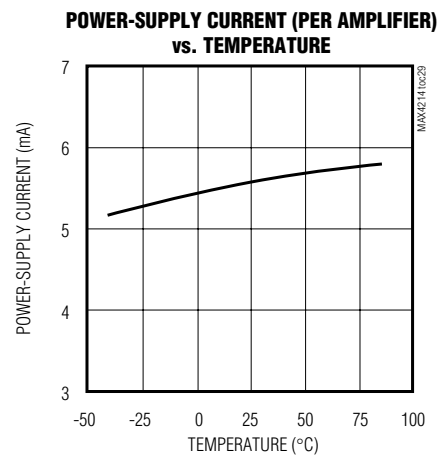
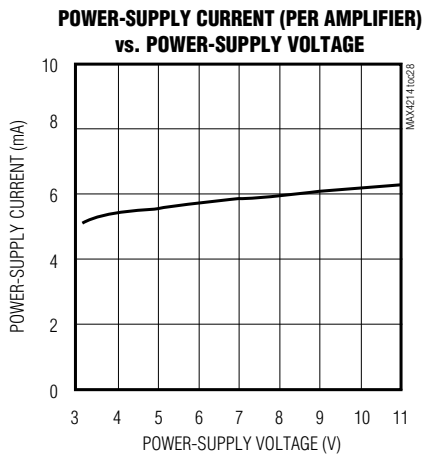
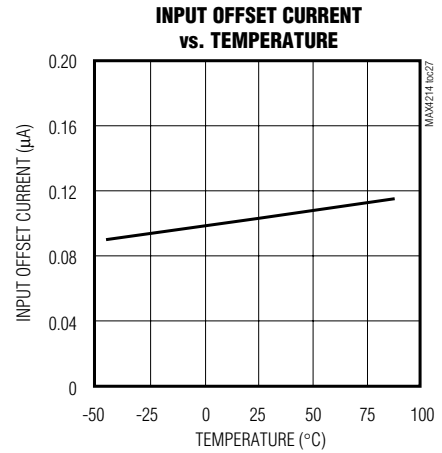
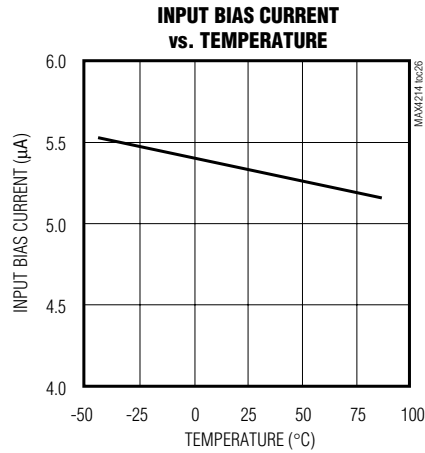
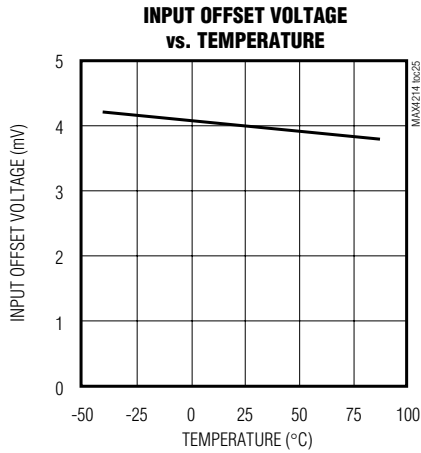
($V_{CC} = 5V$, $V_{EE} = 0$, $A_{VCL} = 2V/V$, $R_L = 100\Omega$ to $V_{CC}/2$, $T_A = +25^\circ C$, unless otherwise noted.)



High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{EE} = 0$, $A_{vCL} = 2V/V$, $R_L = 100\Omega$ to $V_{CC}/2$, $T_A = +25^\circ C$, unless otherwise noted.)



MAX4214/MAX4215/MAX4217/MAX4219/MAX4222

High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

Pin Description

PIN							NAME	FUNCTION
MAX4214	MAX4215	MAX4217	MAX4219		MAX4222			
SOT23-5	SO/ μ MAX	SO/ μ MAX	SO	QSOP	SO	QSOP		
—	1,5	—	—	8,9	—	8,9	N.C.	No Connection. Not internally connected. Tie to ground or leave open.
1	6	—	—	—	—	—	OUT	Amplifier Output
2	4	4	11	13	11	13	V _{EE}	Negative Power Supply or Ground (in single-supply operation)
3	3	—	—	—	—	—	IN+	Noninverting Input
4	2	—	—	—	—	—	IN-	Inverting Input
5	7	8	4	4	4	4	V _{CC}	Positive Power Supply
—	8	—	—	—	—	—	EN	Enable Amplifier
—	—	—	1	1	—	—	ENA	Enable Amplifier A
—	—	—	3	3	—	—	ENB	Enable Amplifier B
—	—	—	2	2	—	—	ENC	Enable Amplifier C
—	—	1	7	7	1	1	OUTA	Amplifier A Output
—	—	2	6	6	2	2	INA-	Amplifier A Inverting Input
—	—	3	5	5	3	3	INA+	Amplifier A Noninverting Input
—	—	7	8	10	7	7	OUTB	Amplifier B Output
—	—	6	9	11	6	6	INB-	Amplifier B Inverting Input
—	—	5	10	12	5	5	INB+	Amplifier B Noninverting Input
—	—	—	14	16	8	10	OUTC	Amplifier C Output
—	—	—	13	15	9	11	INC-	Amplifier C Inverting Input
—	—	—	12	14	10	12	INC+	Amplifier C Noninverting Input
—	—	—	—	—	14	16	OUTD	Amplifier D Output
—	—	—	—	—	13	15	IND-	Amplifier D Inverting Input
—	—	—	—	—	12	14	IND+	Amplifier D Noninverting Input

MAX4214/MAX4215/MAX4217/MAX4219/MAX4222

High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

Detailed Description

The MAX4214/MAX4215/MAX4217/MAX4219/MAX4222 are single-supply, rail-to-rail output, voltage-feedback, closed-loop buffers that employ current-feedback techniques to achieve 600V/ μ s slew rates and 230MHz bandwidths. These buffers use internal 500 Ω resistors to provide a preset closed-loop gain of 2V/V in the noninverting configuration or -1V/V in the inverting configuration. Excellent harmonic distortion and differential gain/phase performance make them an ideal choice for a wide variety of video and RF signal-processing applications.

Local feedback around the buffer's output stage ensures low output impedance, which reduces gain sensitivity to load variations. This feedback also produces demand-driven current bias to the output transistors for \pm 120mA drive capability, while constraining total supply current to less than 7mA.

Applications Information

Power Supplies

These devices operate from a single 3.15V to 11V power supply or from dual supplies of \pm 1.575V to \pm 5.5V. For single-supply operation, bypass the VCC pin to ground with a 0.1 μ F capacitor as close to the pin as possible. If operating with dual supplies, bypass each supply with a 0.1 μ F capacitor.

Selecting Gain Configuration

Each buffer in the MAX4214 family can be configured for a voltage gain of 2V/V or -1V/V. For a gain of 2V/V, ground the inverting terminal. Use the noninverting terminal as the signal input of the buffer (Figure 1a). Grounding the noninverting terminal and using the inverting terminal as the signal input configures the buffer for a gain of -1V/V (Figure 1b).

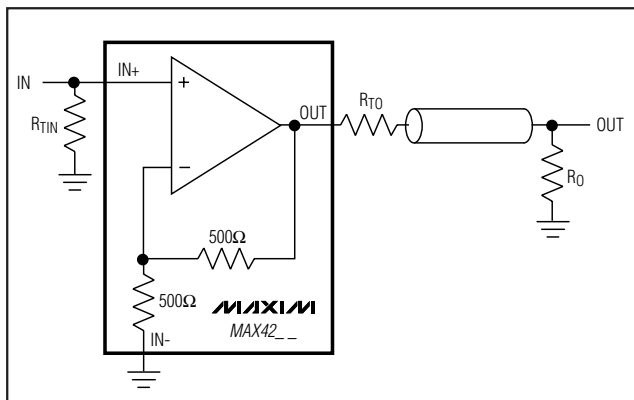


Figure 1a. Noninverting Gain Configuration ($A_V = +2V/V$)

Since the inverting input exhibits a 500 Ω input impedance, terminate the input with a 56 Ω resistor when configured for an inverting gain in 50 Ω applications (terminate with 88 Ω in 75 Ω applications). Terminate the input with a 49.9 Ω resistor in the noninverting case. Output terminating resistors should directly match cable impedances in either configuration.

Layout Techniques

Maxim recommends using microstrip and stripline techniques to obtain full bandwidth. To ensure the PC board does not degrade the buffer's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Whether or not you use a constant-impedance board, observe the following guidelines when designing the board:

- Don't use wire-wrapped boards. They are too inductive.
- Don't use IC sockets. They increase parasitic capacitance and inductance.
- Use surface-mount instead of through-hole components for better high-frequency performance.
- Use a PC board with at least two layers; it should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

Input Voltage Range and Output Swing

The MAX4214 family's input range extends from ($V_{EE} - 100\text{mV}$) to ($V_{CC} - 2.25\text{V}$). Input ground sensing increases the dynamic range for single-supply applications. The outputs drive a 2k Ω load to within 60mV of the power-supply rails. With smaller resistive loads, the output swing is reduced as shown in the *Electrical Characteristics* and *Typical Operating Characteristics*.

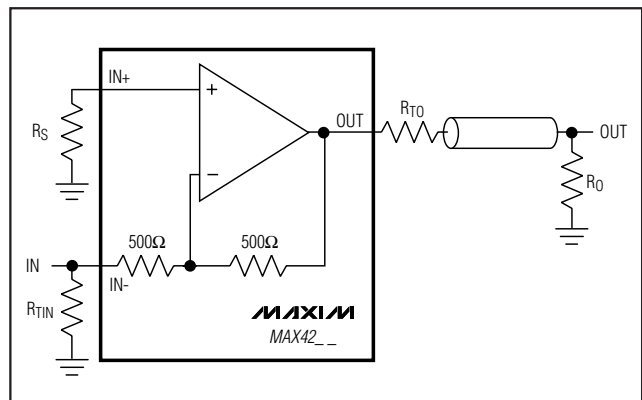


Figure 1b. Inverting Gain Configuration ($A_V = -1V/V$)

High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

As the load resistance decreases, the useful input range is effectively limited by the output drive capability, since the buffers have a fixed voltage gain of 2V/V or -1V/V.

For example, a 50Ω load can typically be driven from 40mV above V_{EE} to 1.6V below V_{CC}, or 40mV to 3.4V when operating from a single 5V supply. If the buffer is operated in the noninverting, gain of 2V/V configuration with the inverting input grounded, the useful input voltage range becomes 20mV to 1.7V instead of the -100mV to 2.75V indicated by the *Electrical Characteristics*. Beyond the useful input range, the buffer output is a nonlinear function of the input, but it will not undergo phase reversal or latchup.

Enable

The MAX4215/MAX4219 have an enable feature (EN₋) that allows the buffer to be placed in a low-power state. When the buffers are disabled, the supply current is reduced to 400μA per buffer.

As the voltage at the EN₋ pin approaches the negative supply rail, the EN₋ input current rises. Figure 2 shows a graph of EN₋ input current versus EN₋ pin voltage. Figure 3 shows the addition of an optional resistor in series with the EN pin, to limit the magnitude of the current increase. Figure 4 displays the resulting EN pin input current to voltage relationship.

Disabled Output Resistance

The MAX4214/MAX4215/MAX4217/MAX4219/MAX4222 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages (Figure 5). This protection circuitry con-

sists of five back-to-back Schottky diodes between IN₊ and IN₋. These diodes reduce the disabled output resistance from 1kΩ to 500Ω when the output voltage is 3V greater or less than the voltage at IN₊. Under these conditions, the input protection diodes will be forward biased, lowering the disabled output resistance to 500Ω.

Output Capacitive Loading and Stability

The MAX4214 family provides maximum AC performance with no load capacitance. This is the case when the load is a properly terminated transmission line. These devices are designed to drive up to 20pF of load capacitance without oscillating, but AC performance will be reduced under these conditions.

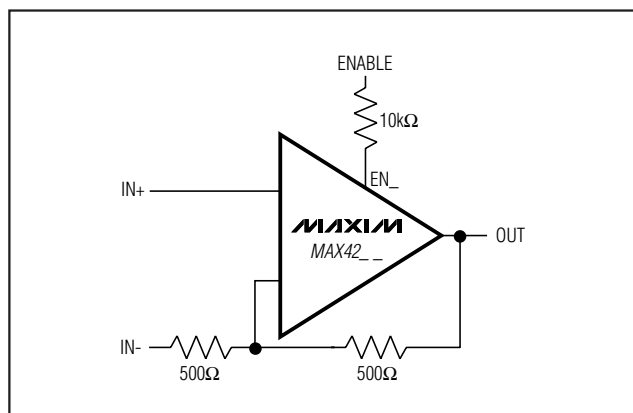


Figure 3. Circuit to Reduce Enable Logic-Low Input Current

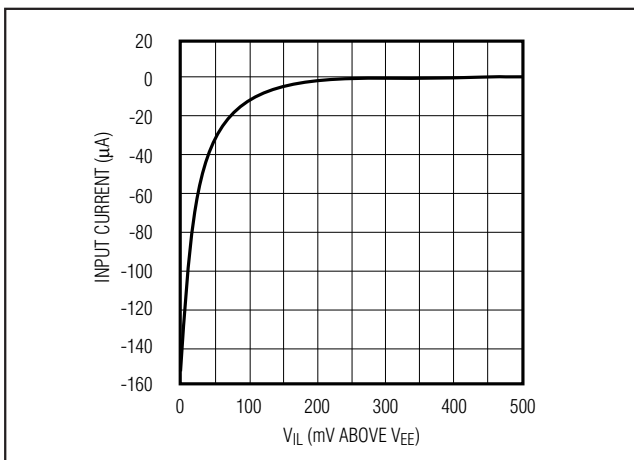


Figure 2. Enable Logic-Low Input Current vs. Enable Logic-Low Threshold

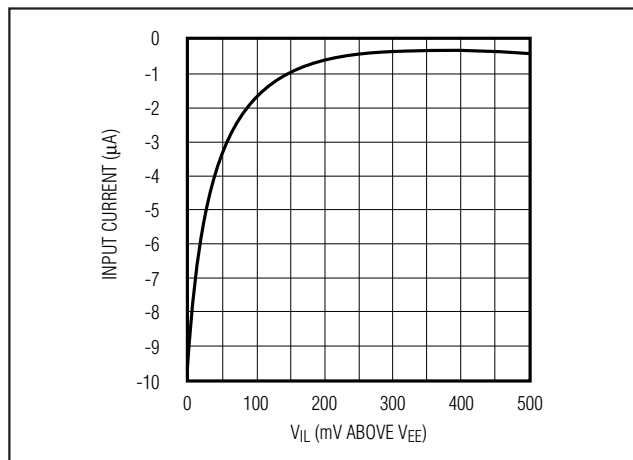


Figure 4. Enable Logic-Low Input Current vs. Enable Logic-Low Threshold with 10kΩ Series Resistor

High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

MAX4214/MAX4215/MAX4217/MAX4219/MAX4222

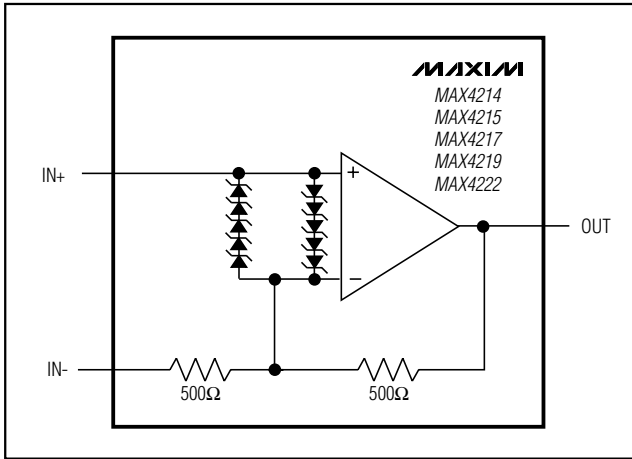


Figure 5. Input Protection Circuit

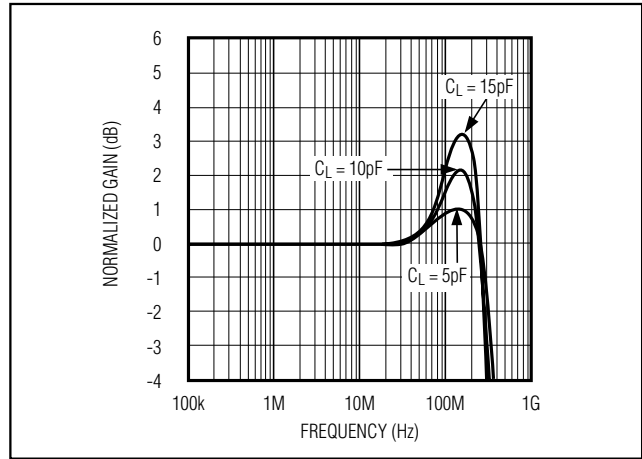


Figure 6. Small-Signal Gain vs. Frequency with Load Capacitance and No Isolation Resistor

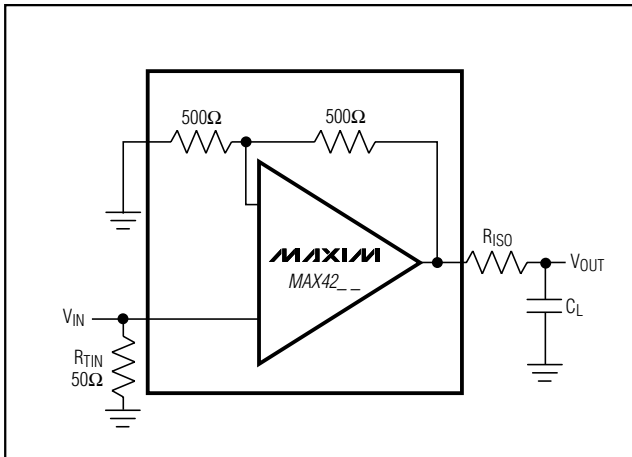


Figure 7. Driving a Capacitive Load Through an Isolation Resistor

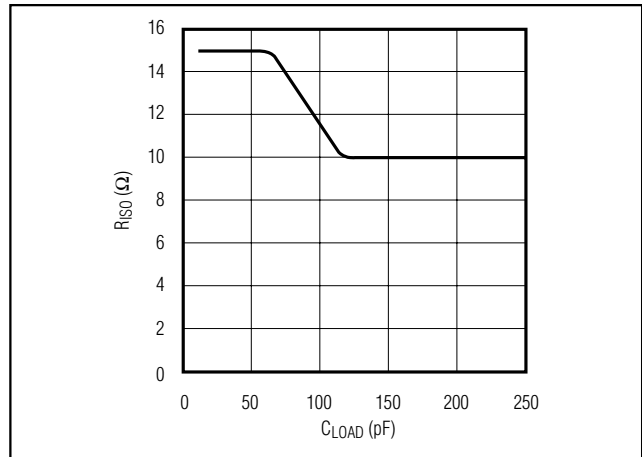


Figure 8. Isolation Resistance vs. Capacitive Load

Driving large capacitive loads increases the chance of oscillations occurring in most amplifier circuits. This is especially true for circuits with high loop gains, such as voltage followers. The buffer's output resistance and the load capacitor combine to add a pole and excess phase to the loop response. If the frequency of this pole is low enough to interfere with the loop response and degrade phase margin sufficiently, oscillations can occur.

A second problem when driving capacitive loads results from the amplifier's output impedance, which looks inductive at high frequencies. This inductance forms an L-C resonant circuit with the capacitive load, which causes peaking in the frequency response and degrades the amplifier's gain margin.

Figure 6 shows the devices' frequency response under different capacitive loads. To drive loads with greater than 20pF of capacitance or to settle out some of the peaking, the output requires an isolation resistor like the one shown in Figure 7. Figure 8 is a graph of the Optimal Isolation Resistor vs. Load Capacitance. Figure 9 shows the frequency response of the MAX4214/MAX4215/MAX4217/MAX4219/MAX4222 when driving capacitive loads with a 27Ω isolation resistor.

Coaxial cables and other transmission lines are easily driven when properly terminated at both ends with their characteristic impedance. Driving back-terminated transmission lines essentially eliminates the lines' capacitance.

High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

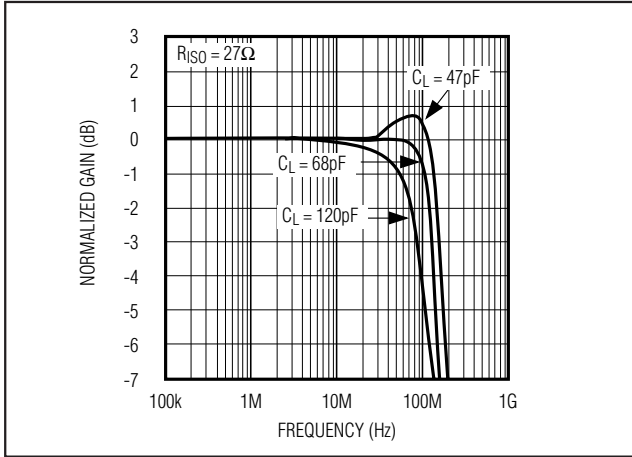
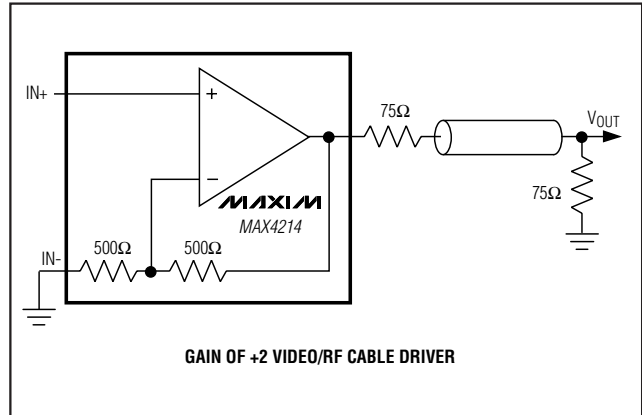


Figure 9. Small-Signal Gain vs. Frequency with Load Capacitance and 27Ω Isolation Resistor

Typical Application Circuit



Chip Information

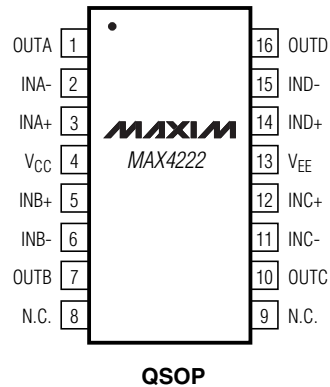
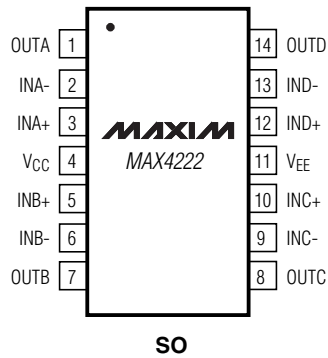
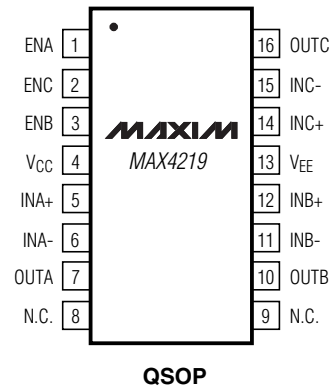
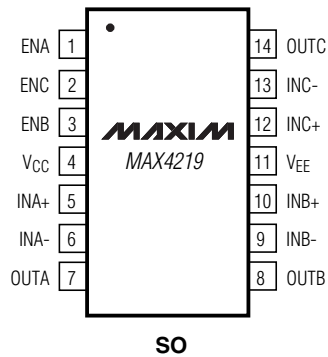
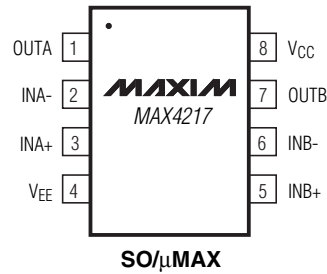
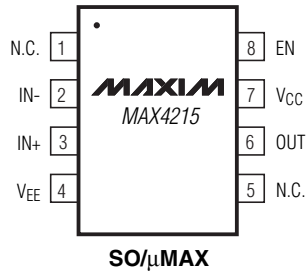
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- MAX4215 TRANSISTOR COUNT: 95
- MAX4217 TRANSISTOR COUNT: 190
- MAX4219 TRANSISTOR COUNT: 299
- MAX4222 TRANSISTOR COUNT: 362
- SUBSTRATE CONNECTED TO V_{EE}

High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

Pin Configurations (continued)

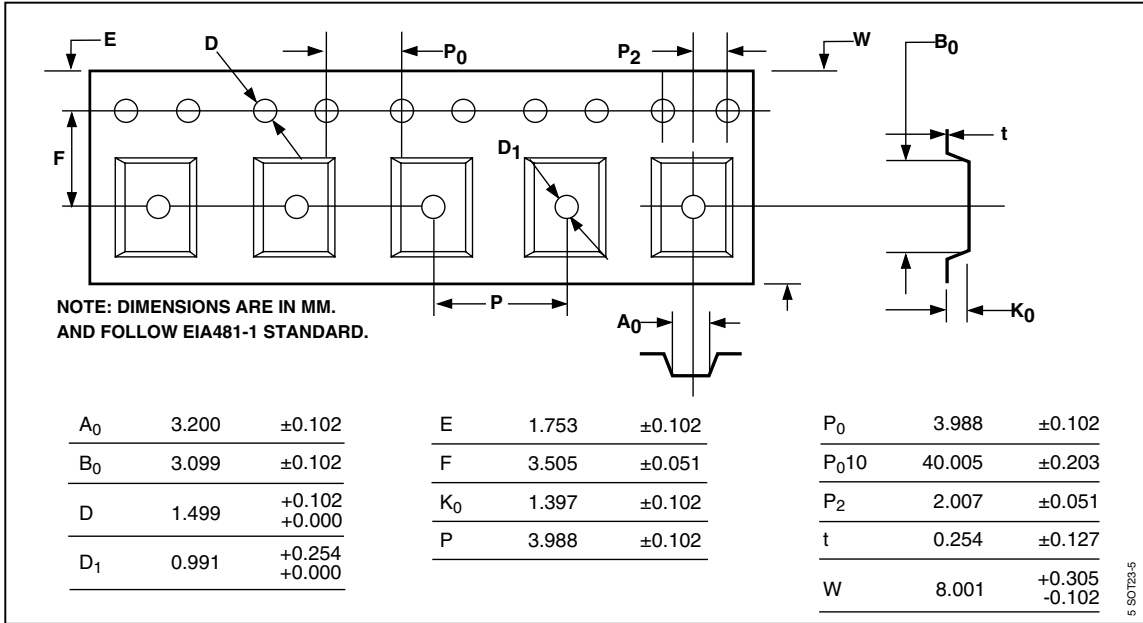
MAX4214/MAX4215/MAX4217/MAX4219/MAX4222

TOP VIEW



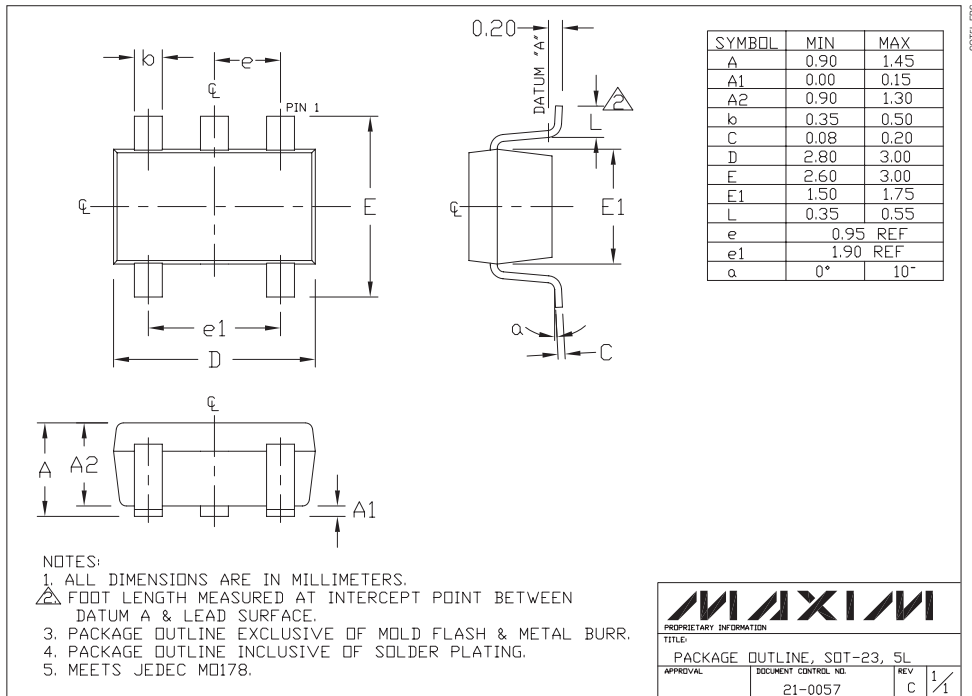
High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

Tape-and-Reel Information



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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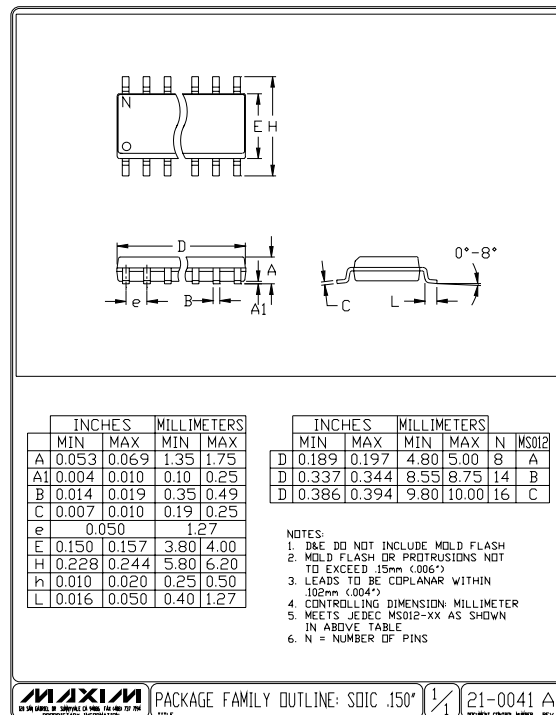
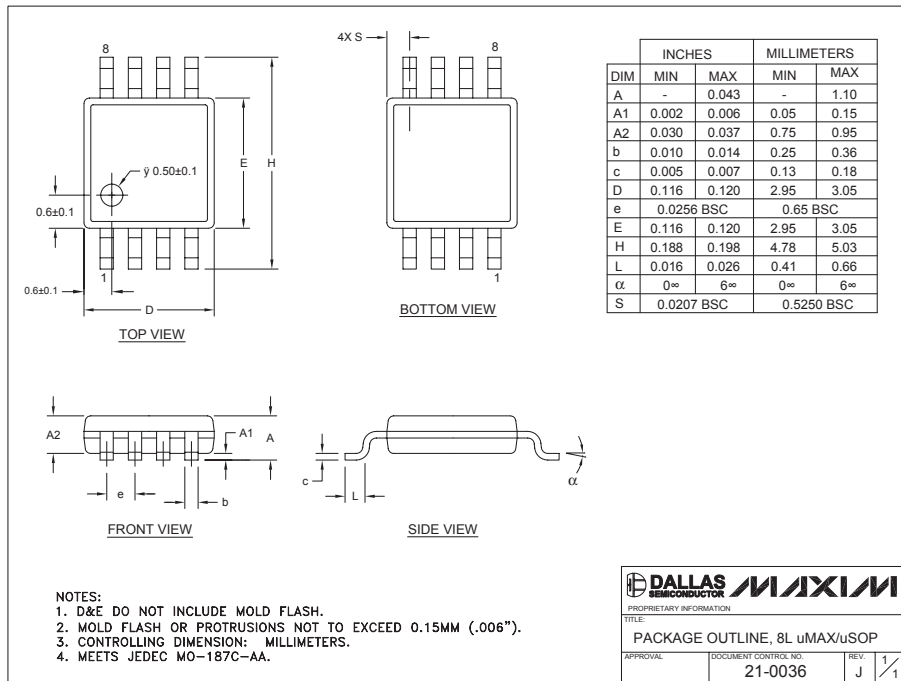
TITLE: PACKAGE OUTLINE, SOT-23, 5L

APPROVAL:	DOCUMENT CONTROL NO.	REV
	21-0057	C 1/1

High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

Package Information (continued)

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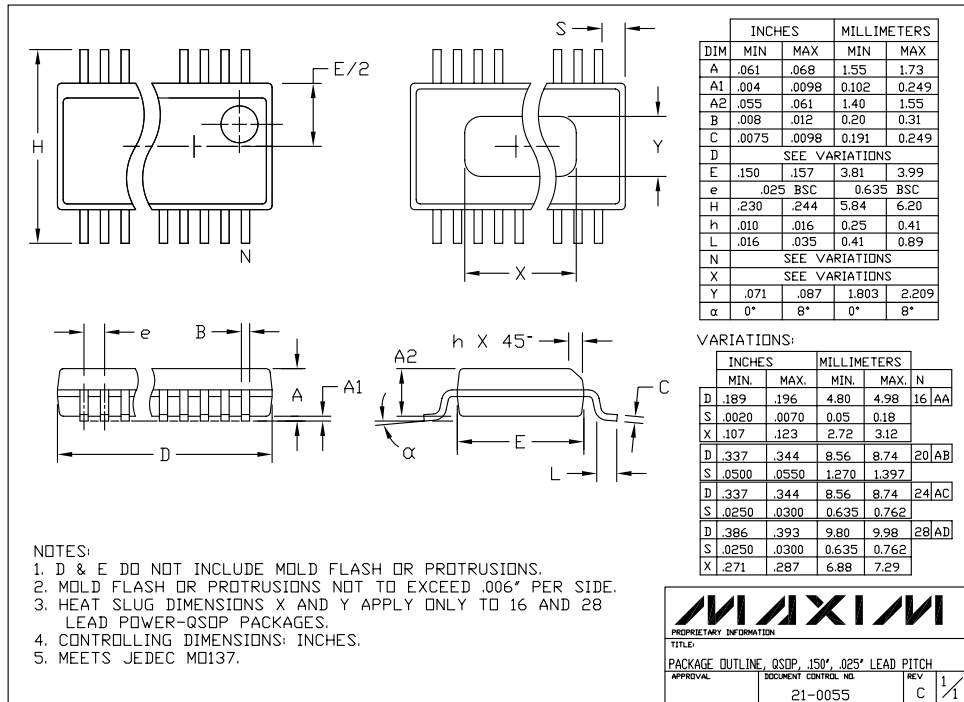


MAX4214/MAX4215/MAX4217/MAX4219/MAX4222

High-Speed, Single-Supply, Gain of 2, Closed-Loop, Rail-to-Rail Buffers with Enable

Package Information (continued)

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QSDP-EPS

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 TITLE: PACKAGE OUTLINE, QSDP, J50°, .025° LEAD PITCH
 APPROVAL: _____ DOCUMENT CONTROL NO: 21-0055 REV: C 1/1

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