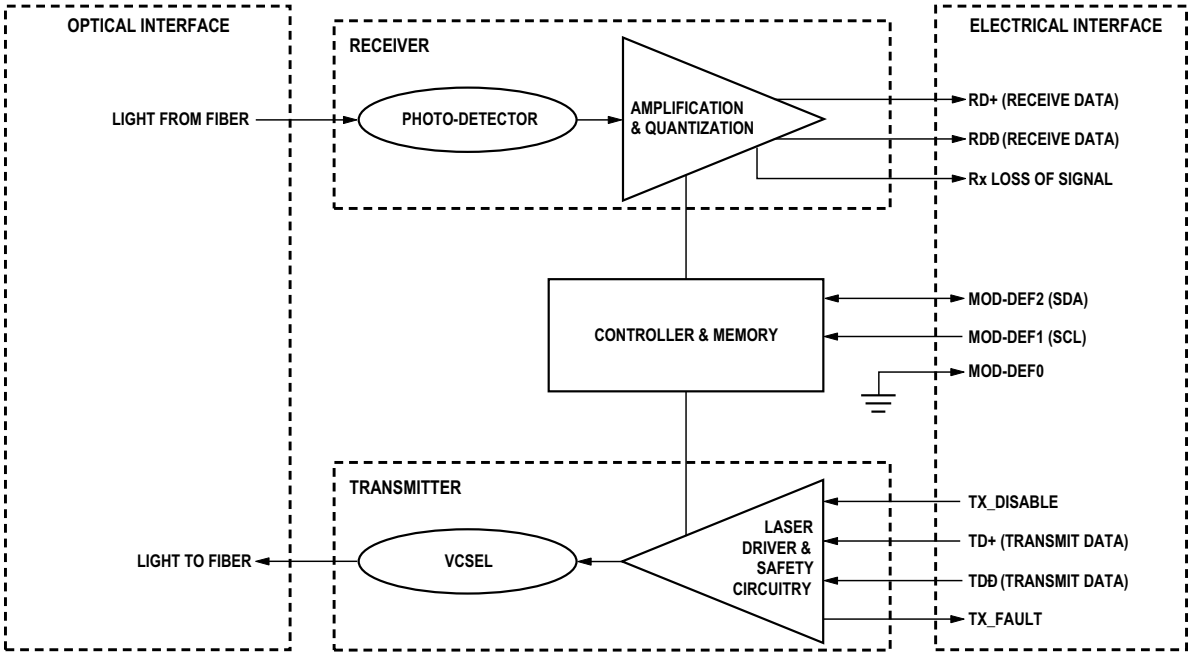


Figure 1. SFP Block Diagram

Overview

The AFBR-571*x*Z family of optical transceivers are compliant with the specifications set forth in the IEEE802.3 (1000BASE-SX) and the Small Form-Factor Pluggable (SFP) Multi-Source Agreement (MSA). This family of transceivers is qualified in accordance with Telcordia GR-468-CORE. Its primary application is servicing Gigabit Ethernet links between optical networking equipment.

The AFBR-571*x*Z offers maximum flexibility to designers, manufacturers, and operators of Gigabit Ethernet networking equipment. A pluggable architecture allows the module to be installed into MSA standard SFP ports at any time – even with the host equipment operating and online. This facilitates the rapid configuration of equipment to precisely the user's needs – reducing inventory costs and network downtime. Compared with traditional transceivers, the size of the Small Form Factor package enables higher port densities.

Module Diagrams

Figure 1 illustrates the major functional components of the AFBR-571*x*Z. The external configuration of the module is depicted in Figure 7. Figure 8 depicts the panel and host board footprints.

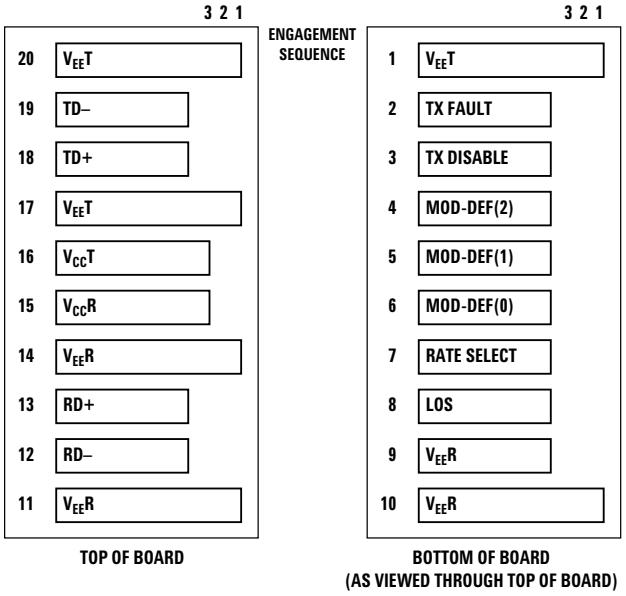


Figure 2. Pin description of the SFP electrical interface.

Installation

The AFBR-571*x*Z can be installed in or removed from any MSA-compliant Pluggable Small Form Factor port regardless of whether the host equipment is operating or not. The module is simply inserted, electrical-interface first, under finger-pressure. Controlled hot-plugging is ensured by 3-stage pin sequencing at the electrical interface. This printed circuit board card-edge connector is depicted in Figure 2.

As the module is inserted, first contact is made by the housing ground shield, discharging any potentially component-damaging static electricity. Ground pins engage next and are followed by Tx and Rx power supplies. Finally, signal lines are connected. Pin functions and sequencing are listed in Table 2.

Transmitter Section

The transmitter section includes the Transmitter Optical Subassembly (TOSA) and laser driver circuitry. The TOSA, containing an 850 nm VCSEL (Vertical Cavity Surface Emitting Laser) light source, is located at the optical interface and mates with the LC optical connector. The TOSA is driven by a custom IC, which converts differential logic signals into an analog laser diode drive current. This Tx driver circuit regulates the optical power at a constant level provided the data pattern is DC balanced (8B10B code for example).

Transmit Disable (Tx_Disable)

The AFBR-571*x*Z accepts a TTL and CMOS compatible transmit disable control signal input (pin 3) which shuts down the transmitter optical output. A high signal implements this function while a low signal allows normal transceiver operation. In the event of a fault (e.g. eye safety circuit activated), cycling this control signal resets the module as depicted in Figure 6. An internal pull-up resistor disables the transceiver transmitter until the host pulls the input low. Host systems should allow a 10ms interval between successive assertions of this control signal. Tx_Disable can also be asserted via the 2-wire serial interface (address A2h, byte 110, bit 6) and monitored (address A2h, byte 110, bit 7).

The contents of A2h, byte 110, bit 6 are logic OR'd with hardware Tx_Disable (pin 3) to control transmitter operation.

Transmit Fault (Tx_Fault)

A catastrophic laser fault will activate the transmitter signal, TX_FAULT, and disable the laser. This signal is an open collector output (pull-up required on the host board). A low signal indicates normal laser operation and a high signal indicates a fault. The TX_FAULT will be latched high when a laser fault occurs and is cleared by toggling the TX_DISABLE input or power cycling the transceiver. The transmitter fault condition can also be monitored via the 2-wire serial interface (address A2, byte 110, bit 2).

Eye Safety Circuit

The AFBR-571*x*Z provides Class 1 eye safety by design and has been tested for compliance with the requirements listed in Table 1. The eye safety circuit continuously monitors optical output power levels and will disable the transmitter and assert a TX_FAULT signal upon detecting an unsafe condition. Such unsafe conditions can be created by inputs from the host board (Vcc fluxuation, unbalanced code) or faults within the module.

Receiver Section

The receiver section includes the Receiver Optical Subassembly (ROSA) and amplification/quantization circuitry. The ROSA, containing a PIN photodiode and custom trans-impedance preamplifier, is located at the optical interface and mates with the LC optical connector. The ROSA is mated to a custom IC that provides post-amplification and quantization. Also included is a Loss Of Signal (LOS) detection circuit.

Receiver Loss of Signal (Rx_LOS)

The Loss Of Signal (LOS) output indicates an unusable optical input power level. The Loss Of Signal thresholds are set to indicate a definite optical fault has occurred (e.g., disconnected or broken fiber connection to receiver, failed transmitter, etc.).

The post-amplification IC includes transition detection circuitry which monitors the ac level of incoming optical signals and provides a TTL/CMOS compatible status signal to the host (pin 8). An adequate optical input results in a low Rx_LOS output while a high Rx_LOS output indicates an unusable optical input. The Rx_LOS thresholds are factory-set so that a high output indicates a definite optical fault has occurred. For the AFBR-5715Z family, Rx_LOS can also be monitored via the 2-wire serial interface (address A2h, byte 110, bit 1).

Functional I/O

The AFBR-571*x*Z accepts industry standard differential signals such as LVPECL and CML within the scope of the SFP MSA. To simplify board requirements, transmitter bias resistors and ac coupling capacitors are incorporated, per SFF-8074i, and hence are not required on the host board. The module is AC-coupled and internally terminated.

Figure 3 illustrates a recommended interface circuit to link the AFBR-571*x*Z to the supporting Physical Layer integrated circuits.

Timing diagrams for the MSA compliant control signals implemented in this module are depicted in Figure 6.

The AFBR-571*x*Z interfaces with the host circuit board through twenty I/O pins (SFP electrical connector) identified by function in Table 2. The AFBR-571*x*Z high speed transmit and receive interfaces require SFP MSA compliant signal lines on the host board. The Tx_Disable, Tx_Fault, and Rx_LOS lines require TTL lines on the host board (per SFF-8074i) if used. If an application chooses not to take advantage of the functionality of these pins, care must be taken to ground Tx_Disable (for normal operation).

Digital Diagnostic Interface and Serial Identification (EEPROM)

The entire AFBR-571*x*Z family complies with the SFF-8074i SFP specification. The AFBR-5715Z family further complies with SFF-8472, the SFP specification for Digital Diagnostic Monitoring Interface. Both specifications can be found at http://www.sffcommittee.org.

The AFBR-571*x*Z features an EEPROM for Serial ID, which contains the product data stored for retrieval by host equipment. This data is accessed via the 2-wire serial EEPROM protocol of the ATMEL AT24C01A or similar, in compliance with the industry standard SFP Multi-Source Agreement. The base EEPROM memory, bytes 0-255 at memory address 0xA0, is organized in compliance with SFF-8074i. Contents of this serial ID memory are shown in Table 10.

The I2C accessible memory page address 0xB0 is used internally by SFP for the test and diagnostic purposes and it is reserved.

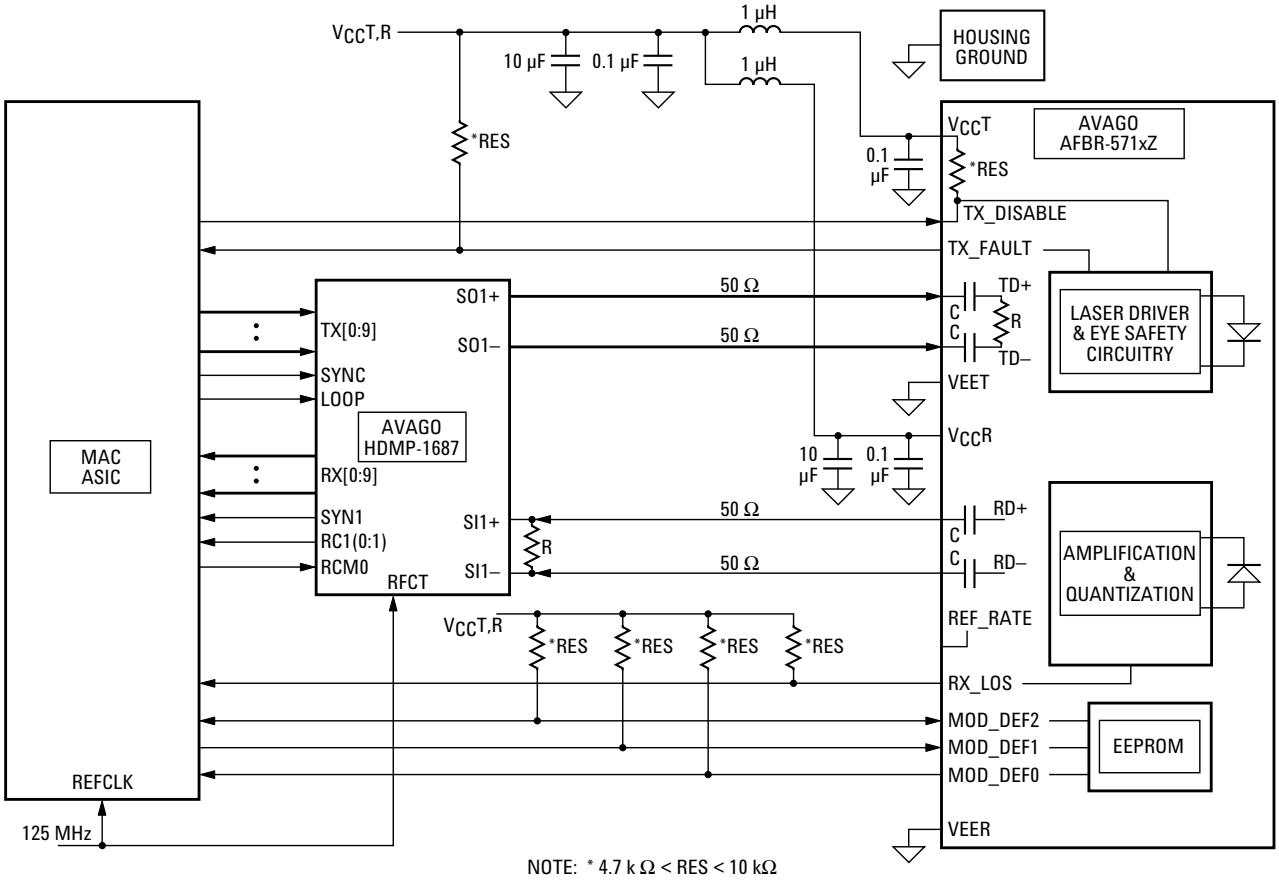


Figure 3. Typical application configuration.

As an enhancement to the conventional SFP interface defined in SFF-8074i, the AFBR-5715Z family is compliant to SFF-8472 (digital diagnostic interface for optical transceivers). This new digital diagnostic information is stored in bytes 0-255 at memory address 0xA2.Using the 2-wire serial interface defined in the MSA, the AFBR-5715Z provides real time temperature, supply voltage, laser bias current, laser average output power and received input power. These parameters are internally calibrated, per the MSA.

The digital diagnostic interface also adds the ability to disable the transmitter (TX_DISABLE), monitor for Transmitter Faults (TX_FAULT), and monitor for Receiver Loss of Signal (RX_LOS).

The new diagnostic information provides the opportunity for Predictive Failure Identification, Compliance Prediction, Fault Isolation and Component Monitoring.

Predictive Failure Identification

The predictive failure feature allows a host to identify potential link problems before system performance is impacted. Prior identification of link problems enables a host to service an application via "fail over" to a redundant link or replace a suspect device, maintaining system uptime in the process. For applications where ultra-high system uptime is required, a digital SFP provides a means to monitor two real-time laser metrics associated with observing laser degradation and predicting failure: average laser bias current (Tx_Bias) and average laser optical power (Tx_Power).

Compliance Prediction

Compliance prediction is the ability to determine if an optical transceiver is operating within its operating and environmental requirements. AFBR-5715Z devices provide real-time access to transceiver internal supply voltage and temperature, allowing a host to identify potential component compliance issues. Received optical power is also available to assess compliance of a cable plant and remote transmitter. When operating out of requirements, the link cannot guarantee error free transmission.

Fault Isolation

The fault isolation feature allows a host to quickly pinpoint the location of a link failure, minimizing downtime. For optical links, the ability to identify a fault at a local device, remote device or cable plant is crucial to speeding service of an installation. AFBR-5715Z real-time monitors of Tx_Bias, Tx_Power, Vcc, Temperature and Rx_Power can be used to assess local transceiver current operating conditions. In addition, status flags Tx_Disable and Rx Loss of Signal (LOS) are mirrored in memory and available via the two-wire serial interface.

Component Monitoring

Component evaluation is a more casual use of the AFBR-5715Z real-time monitors of Tx_Bias, Tx_Power, Vcc, Temperature and Rx_Power. Potential uses are as debugging aids for system installation and design, and transceiver parametric evaluation for factory or field qualification. For example, temperature per module can be observed in high density applications to facilitate thermal evaluation of blades, PCI cards and systems.

Required Host Board Components

The MSA power supply noise rejection filter is required on the host PCB to meet data sheet performance. The MSA filter incorporates an inductor which should be rated 400 mADC and 1 Ω series resistance or better. It should not be replaced with a ferrite. The required filter is illustrated in Figure 4.

The MSA also specifies that 4.7 K to 10 KΩ pull-up resistors for TX_FAULT, LOS, and MOD_DEF0,1,2 are required on the host PCB.

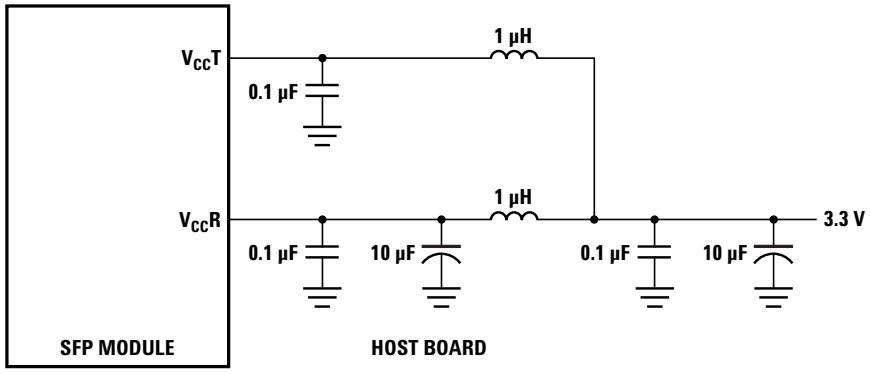


Figure 4. MSA required power supply filter.

Fiber Compatibility

The AFBR-571xZ transciever is capable of transmission at 2 to 550 meters with 50/125 µm fiber, and at 2 to 275 meters with 62.5 125 µm fiber, for 1.25 GBd Ethernet. It is capable of transmission up to 500m with 50/125 µm fiber and up to 300m with 62.5/125 µm fiber, for 1.0625 GBd Fiber Channel.

Application Support

To assist in the transceiver evaluation process, Agilent offers a 1.25 Gbd Gigabit Ethernet evaluation board which facilitates testing of the AFBR-571*x*Z. It can be obtained through the Agilent Field Organization by referencing Agilent part number HFBR-0571.

A Reference Design including the AFBR-571*x*Z and the HDMP-1687 GigaBit Quad SerDes is available. It may be obtained through the Agilent Field Sales organization.

Regulatory Compliance

See Table 1 for transceiver Regulatory Compliance. Certification level is dependent on the overall configuration of the host equipment. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

The AFBR-571*x*Z exceeds typical industry standards and is compatible with ESD levels found in typical manufacturing and operating environments as described in Table 1.

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to insertion into the transceiver port. To protect the transceiver, it's important to use normal ESD handling precautions. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas. The ESD sensitivity of the AFBR-571*x*Z is compatible with typical industry production environments.

The second case to consider is static discharges to the exterior of the host equipment chassis after installation. To the extent that the optical interface is exposed to the outside of the host equipment chassis, it may be subject to system-level ESD requirements.

Electromagnetic Interference (EMI)

Equipment using the AFBR-571*x*Z family of transceivers is typically required to meet the requirements of the FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe, and VCCI in Japan.

The metal housing and shielded design of the AFBR-571xZ minimize the EMI challenge facing the host equipment designer.

EMI Immunity

Equipment hosting AFBR-571*x*Z modules will be subjected to radio-frequency electromagnetic fields in some environments. The transceiver has excellent immunity to such fields due to its shielded design.

Flammability

The AFBR-571*x*Z transceiver is made of metal and high strength, heat resistant, chemically resistant, and UL 94V-0 flame retardant plastic.

Customer Manufacturing Processes

This module is pluggable and is not designed for aqueous wash, IR reflow, or wave soldering processes.

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD)to the Electrical Pins	JEDEC/EIAJESD22-A114-A	Class 2 (> +2000 Volts)
Electrostatic Discharge (ESD) to the Duplex LC Reseptacle	Variation of IEC 6100-4-2	Typically withstands at least 25 kV without damage when the duplex LC connector receptacle is contacted by a Human Body Model probe
Electromagnetic Interference(EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class 1	Applications with high SFP port counts are expected to be compliant; however, margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows a negligible effect from a 10 V/m field swept from 80 to 1000 MHz applied to the transceiver without a chassis enclosure.
Eye Safety	US FDA CDRH AEL Class 1 EN(IEC)60825-1,2, EN60950 Class 1	CDRH certification #9720151-57 TUV file #R 50235455
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment Including Electrical Business Equipment	UL File #E484615
ROHS Compliance		Less than 1000ppm of: cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl ethers.

Caution

There are no user serviceable parts nor any maintenance required for the AFBR-571*x*Z. All adjustments are made at the factory before shipment to our customers. Tampering with, modifying, misusing or improperly handling the AFBR-571*x*Z will void the product warranty. It may also result in improper operation of the AFBR-571*x*Z circuitry, and possible overstress of the laser source. Device degradation or product failure may result. Connection of the AFBR-571*x*Z to a non-Gigabit Ethernet compliant or non-Fiber Channel compliant optical source, operating above the recommended absolute maximum conditions or operating the AFBR-571*x*Z in a manner inconsistent with its design and function may result in hazardous radiation exposure and may be considered an act of modifying or manufacturing a laser product. The person(s) performing such an act is required by law to re-certify and re-identify the laser product under the provisions of U.S. 21 CFR (Subchapter J).

Table 2. Pin Description

Pin	Name	Function/Description	Engagement Order (insertion)	Notes
1	VeeT	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	1
3	TX Disable	Transmitter Disable - Module disables on high or open	3	2
4	MOD-DEF2	Module Definition 2 - Two wire serial ID interface	3	3
5	MOD-DEF1	Module Definition 1 - Two wire serial ID interface	3	3
6	MOD-DEF0	Module Definition 0 - Grounded in module	3	3
7	Rate Selection	Not Connected	3	
8	LOS	Loss of Signal	3	4
9	VeeR	Receiver Ground	1	
10	VeeR	Receiver Ground	1	
11	VeeR	Receiver Ground	1	
12	RD-	Inverse Received Data Out	3	5
13	RD+	Received Data Out	3	5
14	VeeR	Reciver Ground	1	
15	VccR	Receiver Power -3.3 V ±5%	2	6
16	VccT	Transmitter Power -3.3 V ±5%	2	6
17	VeeT	Transmitter Ground	1	
18	TD+	Transmitter Data In	3	7
19	TD-	Inverse Transmitter Data In	3	7
20	VeeT	Transmitter Ground	1	

Notes:

1. TX Fault is an open collector/drain output which should be pulled up externally with a 4.7KΩ – 10 KΩ resistor on the host board to a supply <VccT+0.3 V or VccR+0.3 V. When high, this output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8 V.
2. TX disable input is used to shut down the laser output per the state table below. It is pulled up within the module with a 4.7-10 KΩ resistor.
   - Low (0 – 0.8 V): Transmitter on
   - Between (0.8 V and 2.0 V): Undefined
   - High (2.0 – 3.465 V): Transmitter Disabled
   - Open: Transmitter Disabled
3. Mod-Def 0,1,2. These are the module definition pins. They should be pulled up with a 4.7-10 KΩ resistor on the host board to a supply less than VccT +0.3 V or VccR+0.3 V.
   - Mod-Def 0 is grounded by the module to indicate that the module is present
   - Mod-Def 1 is clock line of two wire serial interface for optional serial ID
   - Mod-Def 2 is data line of two wire serial interface for optional serial ID
4. LOS (Loss of Signal) is an open collector/drain output which should be pulled up externally with a 4.7 K – 10 KΩ resistor on the host board to a supply < VccT,R+0.3 V. When high, this output indicates the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). Low indicates normal operatio0n. In the low state, the output will be pulled to < 0.8 V.
5. RD-/+: These are the differential receiver outputs. They are AC coupled 100 Ω differential lines which should be terminated with 100 Ω differential at the user SERDES. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines must be between 370 and 2000 mV differential (185 – 1000 mV single ended) according to the MSA. Typically it will be 1500mv differential.
6. VccR and VccT are the receiver and transmitter power supplies. They are defined as 3.135 – 3.465 V at the SFP connector pin. The in-rush current will typically be no more than 30 mA above steady state supply current after 500 nanoseconds.
7. TD-/+: These are the differential transmitter inputs. They are AC coupled differential lines with 100 Ω differential termination inside the module. The AC coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 500 – 2400 mV (250 – 1200 mV single ended). However, the applicable recommended differential voltage swing is found in Table 5.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Ambient Storage Temperature (Non-operating)	Ts	-40	+100	°C	1, 2
Case Temperature	T_C	-40	+85	°C	1, 2
Relative Humidity	RH	5	95	%	1
Supply Voltage	$V_{CCT,R}$	-0.5	3.8	V	1, 2, 3
Low Speed Input Voltage	V_{IN}	-0.5	V_{CC}+0.5	V	1

Notes:
1. Absolute Maximum Ratings are those values beyond which damage to the device may occur if these limits are exceeded. See Reliability Data Sheet for specific reliability performance.
2. Between Absolute Maximum Ratings and the Recommended Operating Conditions functional performance is not intended, device reliability is not implied, and damage to the device may occur.
3. The module supply voltages, $V_{CC}T$ and $V_{CC}R$, must not differ by more than 0.5V or damage to the device may occur.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Case Temperature						
AFBR-571xLZ/PZ	T_C	-10	25	85	°C	1, 2
AFBR-571xALZ/APZ	T_C	-40	25	85	°C	1, 2
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	1

Notes:
1. Recommended Operating Conditions are those within which functional performance within data sheet characteristics is intended.
2. Refer to the Reliability Data Sheet for specific reliability performance predictions.

Table 5. Transceiver Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Module Supply Current	I_{CC}		160	220	mA	
Power Dissipation	P_{DISS}		530	765	mW	
Power Supply Noise Rejection(peak-peak)	PSNR		100		mV_{PP}	1
Data input: Transmitter Differential Input Voltage (TD +/-)	V_I	500		2400	mV_{PP}	2
Data Output: Receiver Differential Output Voltage (RD +/-)	V_O	370	1500	2000	mV_{PP}	3
Receive Data Rise & Fall Times	T_{RF}		220		ps	
Low Speed Outputs: Transmit Fault (TX_FAULT)	V_{OH}	2.0		V_{CC}T,R+0.3	V	4
Loss of Signal (LOS), MOD_DEF2	V_{OL}	0		0.8	V	
Low Speed Inputs: Transmitter Disable(TX_DISABLE),	V_{IH}	2.0		V_{CC}	V	5
MOD_DEF 1, MOD_DEF 2	V_{IL}	0		0.8	V	

Notes:
1. Measured at the input of the required MSA Filter on host board.
2. Internally AC coupled and terminated to 100 Ω differential load.
3. Internally AC coupled, but requires a 100 Ω differential termination at or internal to Serializer/Deserializer.
4. Pulled up externally with a 4.7-10 KΩ resistor on the host board to V_{CC}T,R.
5. Mod_Def1 and Mod_Def2 must be pulled up externally with a 4.7-10 KΩ resistor on the host board to V_{CC}T,R.

Table 6. Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Output Optical Power (Average)	P_{OUT}	-9.5	-6.5	-3	dBm	1
Optical Extinction Ratio	ER	9	12		dB	
Center Wavelength	λ_C	830	850	860	nm	
Spectral Width - rms	σ			0.85	nm	
Optical Rise/Fall Time	$T_{RISE/FALL}$		150	260	ps	
Relative Intensity Noise	RIN			-117	dB/Hz	
Total Jitter (TP1 to TP2 Contribution	TJ			227	ps	
				0.284	UI	
Pout TX_DISABLE Assorted	P_{OFF}			-35	dBm	

Notes:
1. 50/125 µm fiber with NA = 0.2, 62.5/125 µm fiber with NA = 0.275.

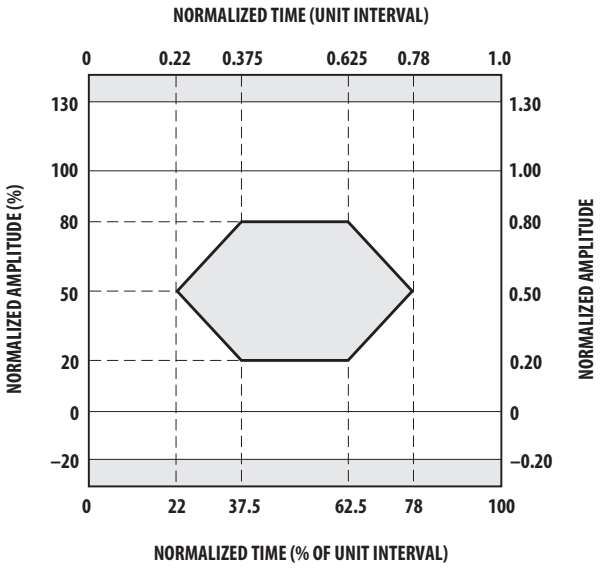


Figure 5a. Gigabit Ethernet transmitter eye mask diagram

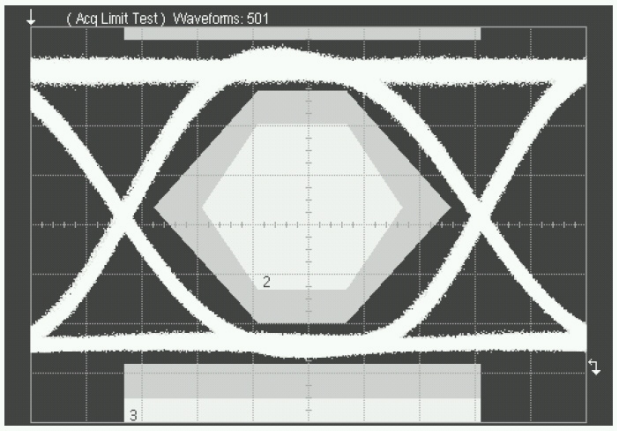


Figure 5b. Typical AFBR-571xZ eye mask diagram

Table 7. Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Optical Input Power	P_R	-17		0	dBm	
Receiver Sensitivity (Optical Input Power)	P_{RMIN}		-21	-17	dBm	
Stressed Receiver Sensitivity				-12.5	dBm	62.5/125 µm fiber
				-13.5	dBm	50/125 µm fiber
Total Jitter (TP3 to TP4 Contribution 1.25GBd)	TJ			266	ps	
				0.332	UI	
Return Loss				-12	dB	
LOS De-Asserted	P_D	-		-17	dBm	
LOS Asserted	P_A	-30			dBm	
LOS Hysterisis	P_D-P_A		3		dB	

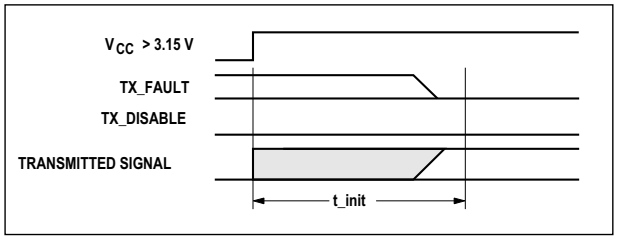
Table 10. Transceiver SOFT DIAGNOSTIC Timing Characteristics

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Hardware TX_DISABLE Assert Time	t_off		10	µs	Note 1
Hardware TX_DISABLE Negate Time	t_on		1	ms	Note 2
Time to initialize, including reset of TX_FAULT	t_init		300	ms	Note 3
Hardware TX_FAULT Assert Time	t_fault		100	µs	Note 4
Hardware TX_DISABLE to Reset	t_reset	10		µs	Note 5
Hardware RX_LOS Assert Time	t_loss_on		100	µs	Note 6
Hardware RX_LOS De-Assert Time	t_loss_off		100	µs	Note 7
Software TX_DISABLE Assert Time	t_off_soft		100	ms	Note 8
Software TX_DISABLE Negate Time	t_on_soft		100	ms	Note 9
Software Tx_FAULT Assert Time	t_fault_soft		100	ms	Note 10
Software Rx_LOS Assert Time	t_loss_on_soft		100	ms	Note 11
Software Rx_LOS Deassert Time	t_loss_off_soft		100	ms	Note 12
Analog parameter data ready	t_data		1000	ms	Note 13
Serial bus hardware ready	t_serial		300	ms	Note 14
Write Cycle Time	t_write		10	ms	Note 15
Serial ID Clock Rate	f_serial_clock		400	kHz	

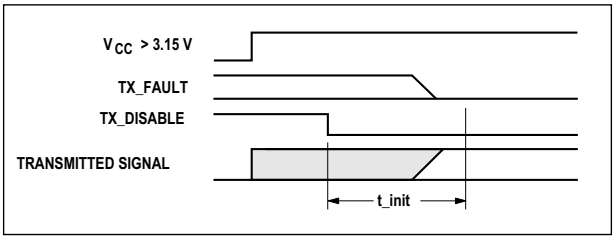
Notes:
1. Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal.
2. Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal.
3. Time from power on or falling edge of Tx_Disable to when the modulated optical output rises above 90% of nominal.
4. From power on or negation of TX_FAULT using TX_DISABLE.
5. Time TX_DISABLE must be held high to reset the laser fault shutdown circuitry.
6. Time from loss of optical signal to Rx_LOS Assertion.
7. Time from valid optical signal to Rx_LOS De-Assertion.
8. Time from two-wire interface assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output falls below 10% of nominal. Measured from falling clock edge after stop bit of write transaction.
9. Time from two-wire interface de-assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the modulated optical output rises above 90% of nominal.
10. Time from fault to two-wire interface TX_FAULT (A2h, byte 110, bit 2) asserted.
11. Time for two-wire interface assertion of Rx_LOS (A2h, byte 110, bit 1) from loss of optical signal.
12. Time for two-wire interface de-assertion of Rx_LOS (A2h, byte 110, bit 1) from presence of valid optical signal.
13. From power on to data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates analog monitoring circuitry is functional.
14. Time from power on until module is ready for data transmission over the serial bus (reads or writes over A0h and A2h).
15. Time from stop bit to completion of a 1-8 byte write command.

Table 9. Transceiver Digital Diagnostic Monitor (Real Time Sense) Characteristics

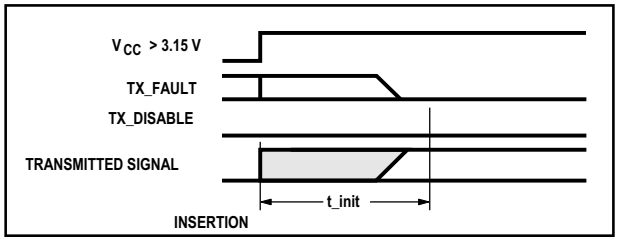
Parameter	Symbol	Min.	Units	Notes
Transceiver Internal Temperature Accuracy	T_{INT}	±3.0	°C	Temperature is measured internal to the transceiver. Valid from = -40°C to 85°C case temperature.
Transceiver Internal Supply Voltage Accuracy	V_{INT}	±0.1	V	Supply voltage is measured internal to the transceiver and can, with less accuracy, be correlated to voltage at the SFP Vcc pin. Valid over 3.3 V ± 5%.
Transmitter Laser DC Bias Current Accuracy	I_{INT}	±10	%	I_{INT} is better than ±10% of the nominal value.
Transmitted Average Optical Output Power Accuracy	P_T	±3.0	dB	Coupled into 50/125 µm multi-mode fiber. Valid from 100 µW to 500 µW, avg.
Received Average Optical Input Power Accuracy	P_R	±3.0	dB	Coupled from 50/125 µm multi-mode fiber. Valid from 31 µW to 500 µW, avg.



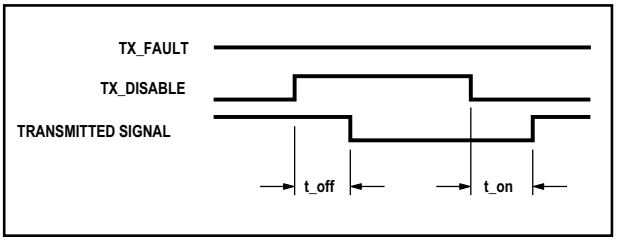
t-init: TX DISABLE NEGATED



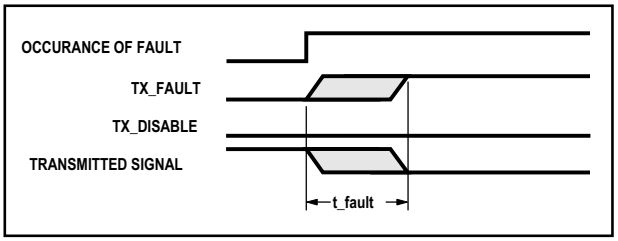
t-init: TX DISABLE ASSERTED



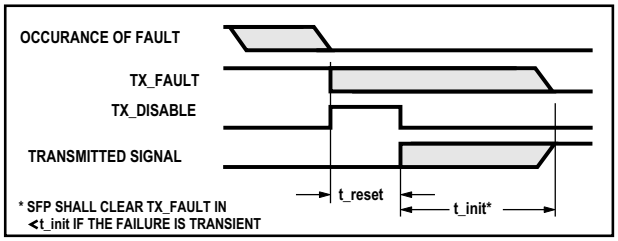
t-init: TX DISABLE NEGATED, MODULE HOT PLUGGED



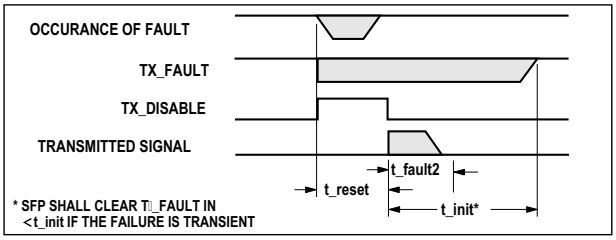
t-off & t-on: TX DISABLE ASSERTED THEN NEGATED



t-fault: TX FAULT ASSERTED, TX SIGNAL NOT RECOVERED

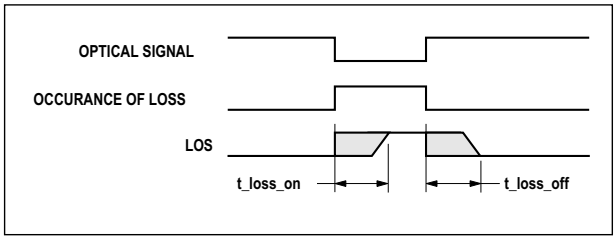


t-reset: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL RECOVERED



t-fault2: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL NOT RECOVERED

NOTE: t_fault2 timing is typically 1.7 to 2 ms.



t-loss-on & t-loss-off

Figure 6. Transceiver timing diagrams (Module installed except where noted).

Table 10. EEPROM Serial ID Memory Contents, Page A0h

Byte Decimal	# Hex	Data Notes	Byte Decimal	# Hex	Data Notes
0	03	SFP physical device	37	00	Vendor OUI (Note 4)
1	04	SFP function defined by serial ID only	38	17	Vendor OUI (Note 4)
2	07	LC optical connector	39	6A	Vendor OUI (Note 4)
3	00		40	41	"A" - Vendor Part Number ASCII character
4	00		41	46	"F" - Vendor Part Number ASCII character
5	00		42	42	"B" - Vendor Part Number ASCII character
6	01	1000BaseSX	43	52	"R" - Vendor Part Number ASCII character
7	00		44	2D	"-" - Vendor Part Number ASCII character
8	00		45	35	"5" - Vendor Part Number ASCII character
9	00		46	37	"7" - Vendor Part Number ASCII character
10	00		47	31	"1" - Vendor Part Number ASCII character
11	01	Compatible with 8B/10B encoded data	48		Note 5
12	0C	1200Mbps nominal bit rate (1.25Gbps)	49		Note 5
13	00		50		Note 5
14	00		51		Note 5
15	00		52	20	" " - Vendor Part Number ASCII character
16	37	550m of 50/125mm fiber @ 1.25Gbps (Note 2)	53	20	" " - Vendor Part Number ASCII character
17	1B	275m of 62.5/125mm fiber @ 1.25Gbps (Note 3)	54	20	" " - Vendor Part Number ASCII character
18	00		55	20	" " - Vendor Part Number ASCII character
19	00		56	20	" " - Vendor Revision Number ASCII character
20	41	'A' - Vendor Name ASCII character	57	20	" " - Vendor Revision Number ASCII character
21	56	"V" - Vendor Name ASCII character	58	20	" " - Vendor Revision Number ASCII character
22	41	"A" - Vendor Name ASCII character	59	20	" " - Vendor Revision Number ASCII character
23	47	"G"- - Vendor Name ASCII character	60	03	Hex Byte of Laser Wavelength (Note 6)
24	4F	"O" - Vendor Name ASCII character	61	52	Hex Byte of Laser Wavelength (Note 6)
25	20	" " - Vendor Name ASCII character	62	00	
26	20	" " - Vendor Name ASCII character	63		Checksum for bytes 0-62 (Note 7)
27	20	" " - Vendor Name ASCII character	64	00	
28	20	" " - Vendor Name ASCII character	65	1A	Hardware SFP TX_DISABLE, TX_FAULT, & RX_LOS
29	20	" " - Vendor Name ASCIIcharacter	66	00	
30	20	" " - Vendor Name ASCIIcharacter	67	00	
31	20	" " - Vendor Name ASCIIcharacter	68-83		Vendor Serial Number, ASCII (Note 8)
32	20	" " - Vendor Name ASCIIcharacter	84-91		Vendor Date Code, ASCII (Note 9)
33	20	" " - Vendor Name ASCIIcharacter	92		Note 5
34	20	" " - Vendor Name ASCIIcharacter	93		Note 5
35	20	" " - Vendor Name ASCIIcharacter	94		Note 5
36	00		95		Checksum for bytes 64-94 (Note 7)
			96 - 255	00	

Notes:
1. FC-PI speed 100 MBytes/sec is a serial bit rate of 1.0625 GBit/sec.
2. Link distance with 50/125µm cable at 1.25Gbps is 550m.
3. Link distance with 62.5/125µm cable at 1.25Gbps is 275m.
4. The IEEE Organizationally Unique Identifier (OUI) assigned to Avago Technologies is 00-17-6A (3 bytes of hex).
5. See Table 11 for part number extensions and data-fields.
6. Laser wavelength is represented in 16 unsigned bits. The hex representation of 850nm is 0352.
7. Addresses 63 and 95 are checksums calculated per SFF-8472 and SFF-8074, and stored prior to product shipment.
8. Addresses 68-83 specify the module's ASCII serial number and will vary by unit.
9. Addresses 84-91 specify the module's ASCII date code and will vary according to manufactured date-code.

Table 11. Part Number Extensions

AFBR-5710ALZ			AFBR-5710APZ			AFBR-5710LZ			AFBR-5710PZ		
Address	**Hex**	**ASCII**	**Address**	**Hex**	**ASCII**	**Address**	**Hex**	**ASCII**	**Address**	**Hex**	**ASCII**
48	30	0	48	30	0	48	30	0	48	30	0
49	41	A	49	41	A	49	4C	L	49	50	P
50	4C	L	50	50	P	50	5A	Z	50	5A	Z
51	5A	Z	51	5A	Z	51	20		51	20	
92	00		92	00		92	00		92	00	
93	00		93	00		93	00		93	00	
94	00		94	00		94	00		94	00	

AFBR-5715ALZ			AFBR-5715APZ			AFBR-5715LZ			AFBR-5715PZ		
Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII
48	35	5	48	35	5	48	35	5	48	35	5
49	41	A	49	41	A	49	4C	L	49	50	P
50	4C	L	50	50	P	50	5A	Z	50	5A	Z
51	5A	Z	51	5A	Z	51	20		51	20	
92	68		92	68		92	68		92	68	
93	F0		93	F0		93	F0		93	F0	
94	01		94	01		94	01		94	01	

Table 12. EEPROM Serial ID Memory Contents - Address A2h (AFBR-5715Z family only)

Byte #Decimal	Notes	Byte #Decimal	Notes	Byte #Decimal	Notes
0	Temp H Alarm MSB[1]	26	Tx Pwr L Alarm MSB[4]	104	Real Time Rx P_{AV} MSB[5]
1	Temp H Alarm LSB[1]	27	Tx Pwr L Alarm LSB[4]	105	Real Time Rx P_{AV} LSB[5]
2	Temp L Alarm MSB[1]	28	Tx Pwr H Warning MSB[4]	106	Reserved
3	Temp L Alarm LSB[1]	29	Tx Pwr H Warning LSB[4]	107	Reserved
4	Temp H Warning MSB[1]	30	Tx Pwr L Warning MSB[4]	108	Reserved
5	Temp H Warning LSB[1]	31	Tx Pwr L Warning LSB[4]	109	Reserved
6	Temp L Warning MSB[1]	32	Rx Pwr H Alarm MSB[5]	110	Status/Control - see Table 13
7	Temp L Warning LSB[1]	33	Rx Pwr H Alarm LSB[5]	111	Reserved
8	V_{CC} H Alarm MSB[2]	34	Rx Pwr L Alarm MSB[5]	112	Flag Bits - see Table 14
9	V_{CC} H Alarm LSB[2]	35	Rx Pwr L Alarm LSB[5]	113	Flag Bit - see Table 14
10	V_{CC} L Alarm MSB[2]	36	Rx Pwr H Warning MSB[5]	114	Reserved
11	V_{CC} L Alarm LSB[2]	37	Rx Pwr H Warning LSB[5]	115	Reserved
12	V_{CC} H Warning MSB[2]	38	Rx Pwr L Warning MSB[5]	116	Flag Bits - see Table 14
13	V_{CC} H Warning LSB[2]	39	Rx Pwr L Warning LSB[5]	117	Flag Bits - see Table 14
14	V_{CC} L Warning MSB[2]	40-55	Reserved	118	Reserved
15	V_{CC} L Warning LSB[2]	56-94	External Calibration Constants[6]	119	Reserved
16	Tx Bias H Alarm MSB[3]	95	Checksum for Bytes 0-94[7]	120-122	Reserved
17	Tx Bias H Alarm LSB[3]	96	Real Time Temperature MSB[1]	123	
18	Tx Bias L Alarm MSB[3]	97	Real Time Temperature LSB[1]	124	
19	Tx Bias L Alarm LSB[3]	98	Real Time Vcc MSB[2]	125	
20	Tx Bias H Warning MSB[3]	99	Real Time Vcc LSB[2]	126	
21	Tx Bias H Warning LSB[3]	100	Real Time Tx Bias MSB[3]	127	Reserved[8]
22	Tx Bias L Warning MSB[3]	101	Real Time Tx Bias LSB[3]	128-247	Customer Writable[9]
23	Tx Bias L Warning LSB[3]	102	Real Time Tx Power MSB[4]	248-255	Vendor Specific
24	Tx Pwr H Alarm MSB[4]	103	Real Time Tx Power LSB[4]		
25	Tx Pwr H Alarm LSB[4]				

Notes:

1. Temperature (Temp) is decoded as a 16 bit signed twos compliment integer in increments of 1/256 °C.
2. Supply voltage (V_{CC}) is decoded as a 16 bit unsigned integer in increments of 100 µV.
3. Laser bias current (Tx Bias) is decoded as a 16 bit unsigned integer in increments of 2 µA.
4. Transmitted average optical power (Tx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 µW.
5. Received average optical power (Rx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 µW.
6. Bytes 55-94 are not intended from use with AFBR-5715Z, but have been set to default values per SFF-8472.
7. Bytes 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.
8. Byte 127 accepts a write but performs no action (reserved legacy byte).
9. Bytes 128-247 are write enabled (customer writable).

Table 13. EEPROM Serial ID Memory Contents - Address A2h, Byte 110 (AFBR-5715Z family only)

Bit #	Status/Control Name	Description
7	Tx Disable State	Digital state of SFP Tx Disable Input Pin (1 = Tx_ Disable asserted)
6	Soft Tx Disable	Read/write bit for changing digital state of SFP Tx_Disable function[1]
5	Reserved	
4	Rx Rate Select State	Digital state of SFP Rate Select Input Pin (1 = full bandwidth of 155 Mbit)[2]
3	Reserved	
2	Tx Fault State	Digital state of the SFP Tx Fault Output Pin (1 = Tx Fault asserted)
1	Rx LOS State	Digital state of the SFP LOS Output Pin (1 = LOS asserted)
0	Data Ready (Bar)	Indicates transceiver is powered and real time sense data is ready (0 = Ready)

Notes:
1. Bit 6 is logic OR'd with the SFP Tx_Disable input pin 3 ... either asserted will disable the SFP transmitter.
2. AFBR-5715Z does not respond to state changes on Rate Select Input Pin. It is internally hardwired to full bandwidth.

Table 14. EEPROM Serial ID Memory Contents - Address A2h, Bytes 112, 113, 116, 117 (AFBR-5715Z family only)

Byte	Bit #	Flag Bit Name	Description
112	7	Temp High Alarm	Set when transceiver nternal temperature exceeds high alarm threshold.
	6	Temp Low Alarm	Set when transceiver internal temperature exceeds alarm threshold.
	5	V_{CC} High Alarm	Set when transceiver internal supply voltage exceeds high alarm threshold.
	4	V_{CC} Low Alarm	Set when transceiver internal supply voltage exceeds low alarm threshold.
	3	Tx Bias High Alarm	Set when transceiver laser bias current exceeds high alarm threshold.
	2	Tx Bias Low Alarm	Set when transceiver laser bias current exceeds low alarm threshold.
	1	Tx Power High Alarm	Set when transmitted average optical power exceeds high alarm threshold.
	0	Tx Power Low Alarm	Set when transmitted average optical power exceeds low alarm threshold.
113	7	Rx Power High Alarm	Set when received P_Avg optical power exceeds high alarm threshold.
	6	Rx Power Low Alarm	Set when received P_Avg optical power exceeds low alarm threshold.
	0-5	Reserved	
116	7	Temp High Warning	Set when transceiver internal temperature exceeds high warning threshold.
	6	Temp Low Warning	Set when transceiver internal temperature exceeds low warning threshold.
	5	V_{CC} High Warning	Set when transceiver internal supply voltage exceeds high warning threshold.
	4	V_{CC} Low Warning	Set when transceiver internal supply voltage exceeds low warning threshold.
	3	Tx Bias High Warning	Set when transceiver laser bias current exceeds high warning threshold.
	2	Tx Bias Low Warning	Set when transceiver laser bias current exceeds low warning threshold.
	1	Tx Power High Warning	Set when transmitted average optical power exceeds high warning threshold.
	0	Tx Power Low Warning	Set when transmitted average optical power exceeds low warning threshold.
117	7	Rx Power High Warning	Set when received P_Avg optical power exceeds high warning threshold.
	9	Rx Power Low Warning	Set when received P_Avg optical power exceeds low warning threshold.
	0-5	Reserved	

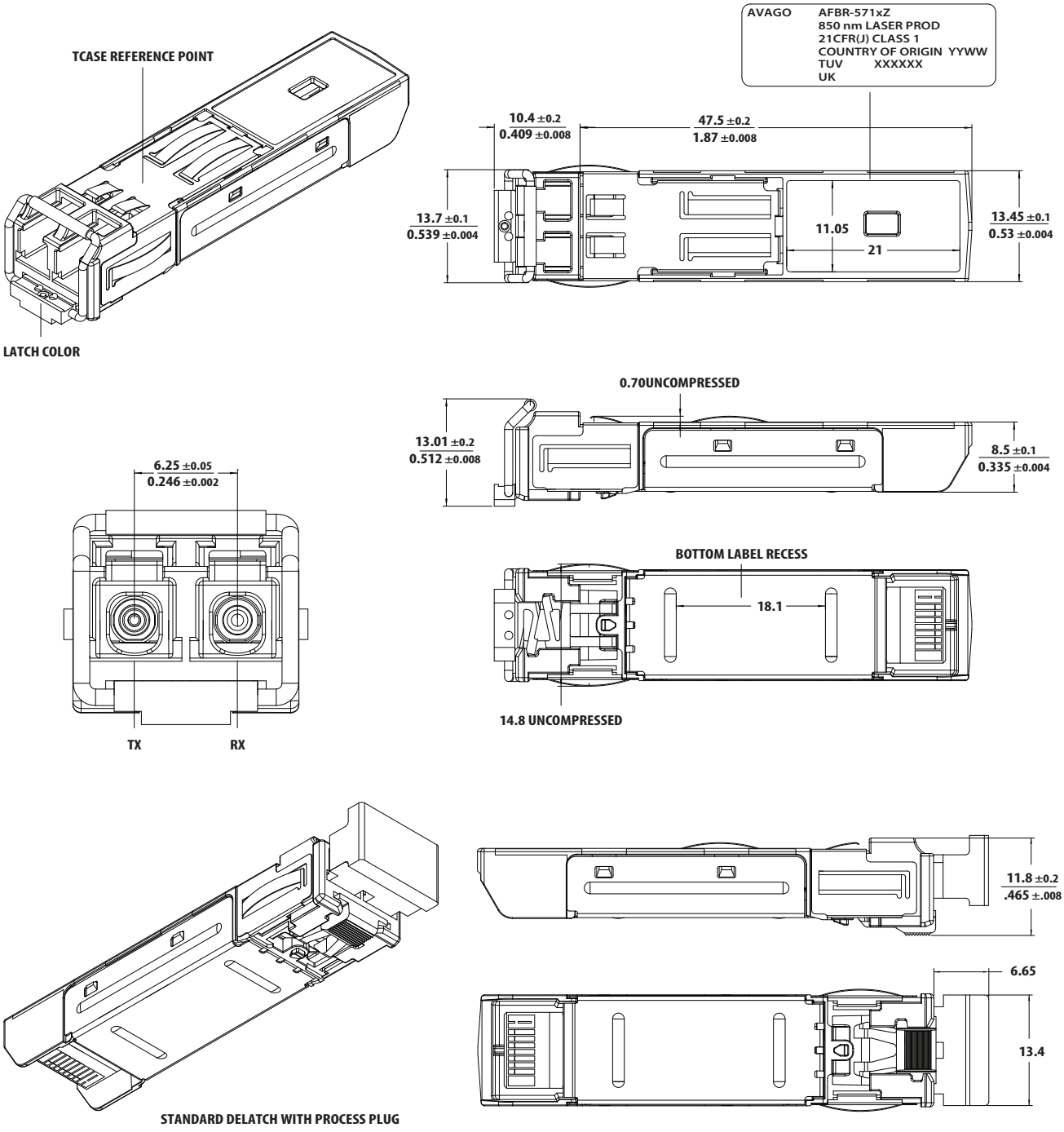
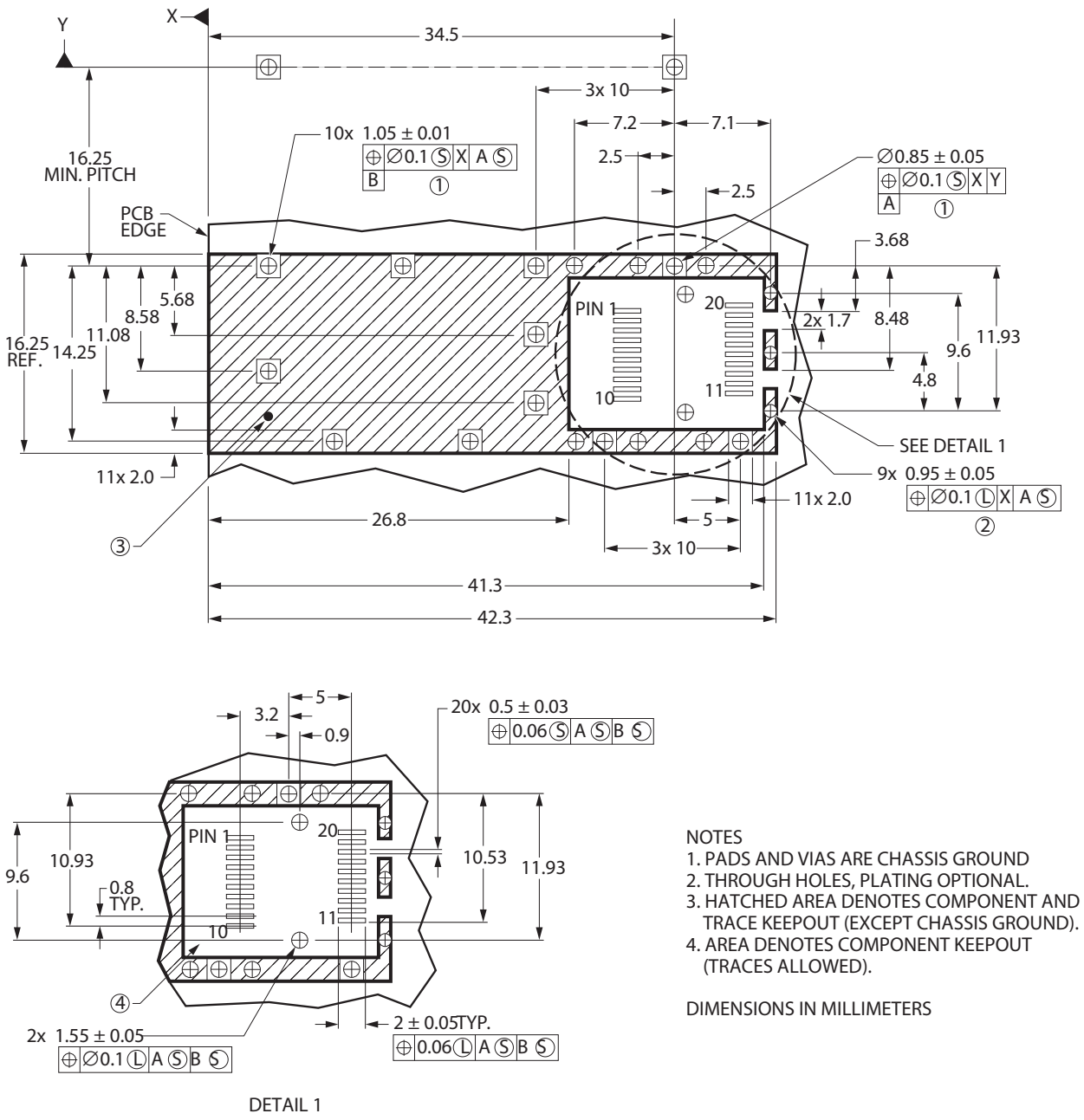


Figure 7. Module drawing



DETAIL 1

NOTES
1. PADS AND VIAS ARE CHASSIS GROUND
2. THROUGH HOLES, PLATING OPTIONAL.
3. HATCHED AREA DENOTES COMPONENT AND TRACE KEEPOUT (EXCEPT CHASSIS GROUND).
4. AREA DENOTES COMPONENT KEEPOUT (TRACES ALLOWED).

DIMENSIONS IN MILLIMETERS

Figure 8. SFP host board mechanical layout

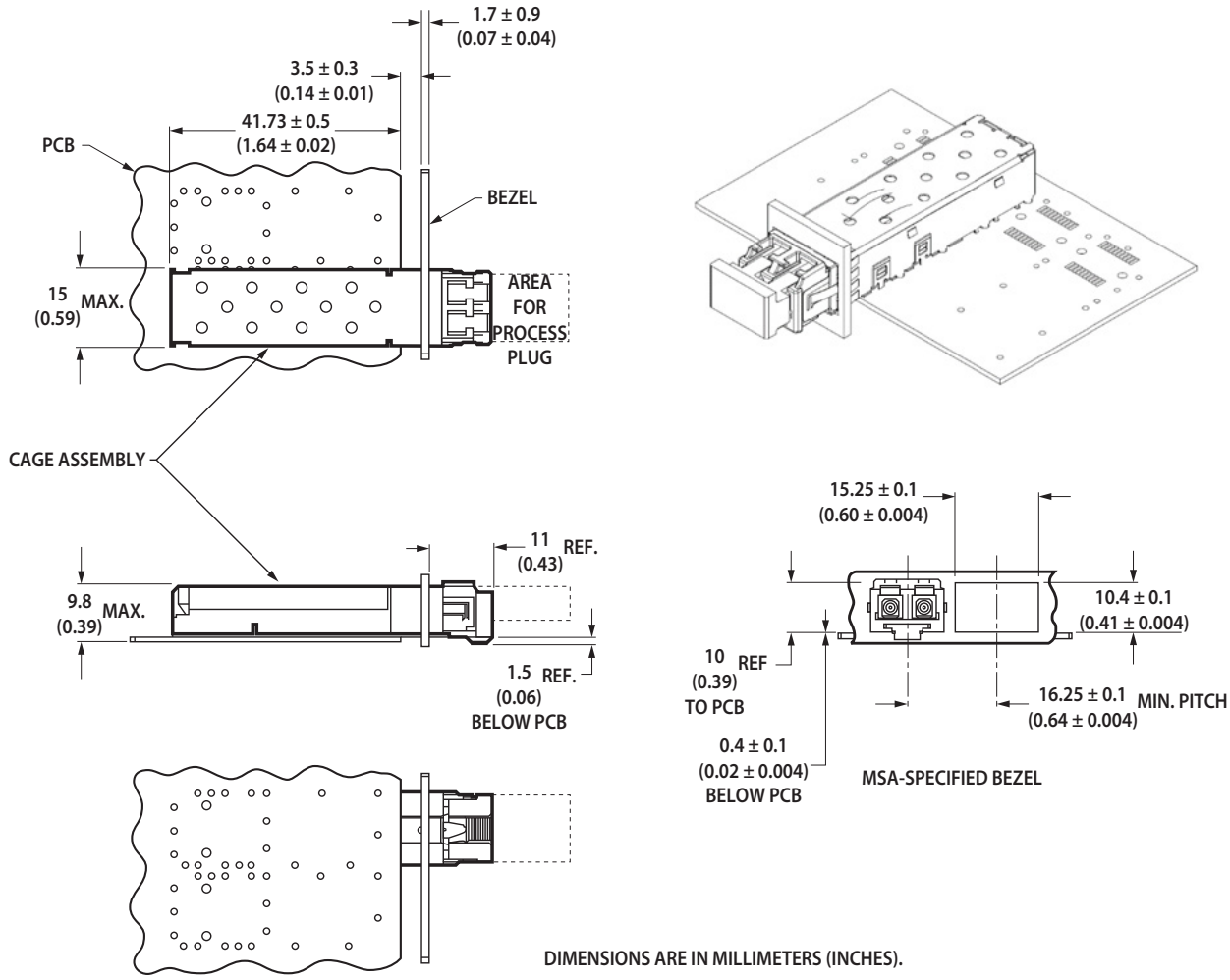


Figure 9. Assembly drawing

Ordering Information

Please contact your local field sales engineer or one of Avago Technologies franchised distributors for ordering information. For technical information, please visit Avago Technologies' web-page at **www.avagotech.com** or contact one of Avago Technologies' regional Technical Response Centers. For information related to SFF Committee documentation visit **www.sffcommittee.org**.

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