Characteristics ESDALC6V1-1U2

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25 \, ^{\circ}C$)

Symbol	Parameter	Value	Unit
V _{PP}	Peak pulse voltage: IEC 61000-4-2 contact discharge	±8	kV
P _{PP}	Peak pulse power dissipation (8/20 µs) (1) $T_{j initial} = T_{amb}$	20	W
I _{PP}	Peak pulse current (8/20 µs)	2	Α
T _j	Junction temperature	125	°C
T _{stg}	Storage temperature range	- 55 to +150	°C
T _L	Maximum lead temperature for soldering during 10 s	260	°C
T _{op}	Operating junction temperature range	-40 to +125	°C

^{1.} For a surge greater than the maximum values, the diode will fail in short-circuit

Figure 2. Electrical characteristics (definitions)

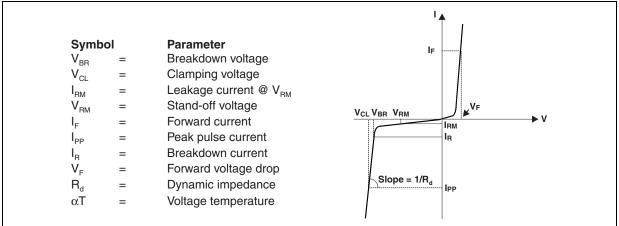


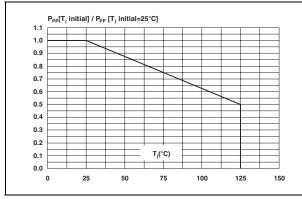
Table 2. Electrical characteristics (values, $T_{amb} = 25 \,^{\circ}$ C)

Symbol	Test conditions	Min.	Тур.	Max.	Unit
V_{BR}	I _R = 1 mA	6.1		8.0	V
I _{RM}	V _{RM} = 3 V			100	nA
R _d	Square pulse, $I_{PP} = 1 \text{ A t}_p = 2.5 \mu \text{s}$		1.3		Ω
αΤ	$\Delta V_{BR} = \alpha T(T_{amb} - 25 ^{\circ}C) \times V_{BR} (25 ^{\circ}C)$			4.5	10 ⁻⁴ /°C
C _{line}	$V_R = 0 \text{ V}, F_{osc} = 1 \text{ MHz}, V_{osc} = 30 \text{ mV}$		12.0		pF

ESDALC6V1-1U2 Characteristics

Figure 3. Relative variation of peak pulse power versus initial junction temperature

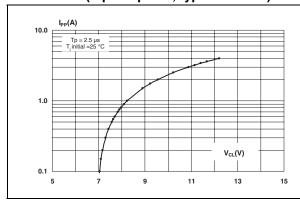
Figure 4. Peak pulse power versus exponential pulse duration



1000 P_{PP}(W)
1000 T_j initial = 25 °C
100 t_p(µs)
100 1000

Figure 5. Clamping voltage versus peak pulse current (square pulse, typical values)

Figure 6. Junction capacitance versus reverse applied voltage (typical values)



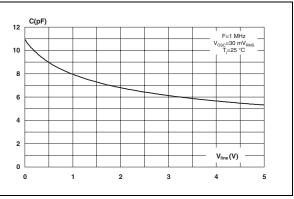
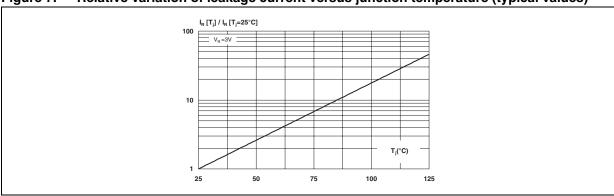


Figure 7. Relative variation of leakage current versus junction temperature (typical values)



Characteristics ESDALC6V1-1U2

Figure 8. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

Figure 9. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

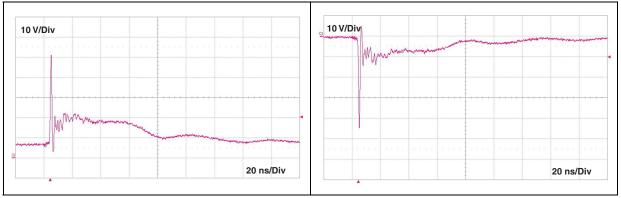
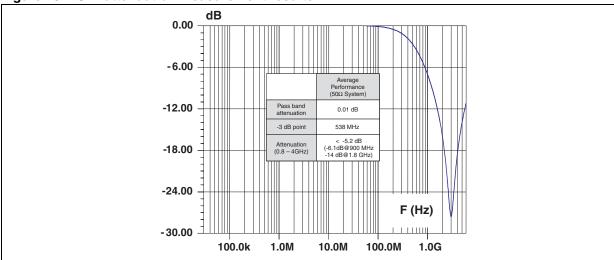


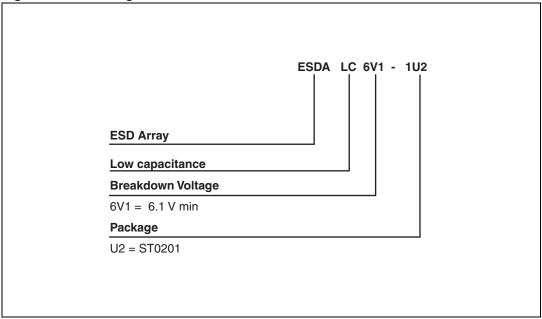
Figure 10. S21 attenuation measurement results



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2 Ordering information scheme

Figure 11. Ordering information scheme



3 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 3. ST0201 dimensions

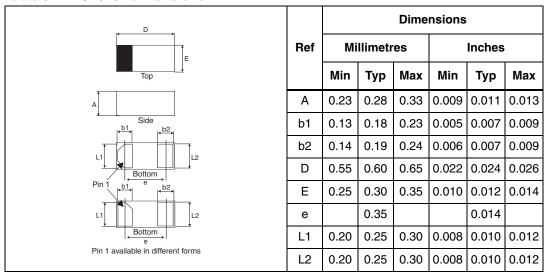
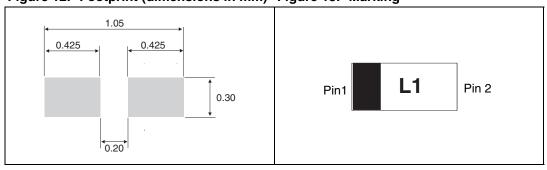


Figure 12. Footprint (dimensions in mm) Figure 13. Marking



Note: Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

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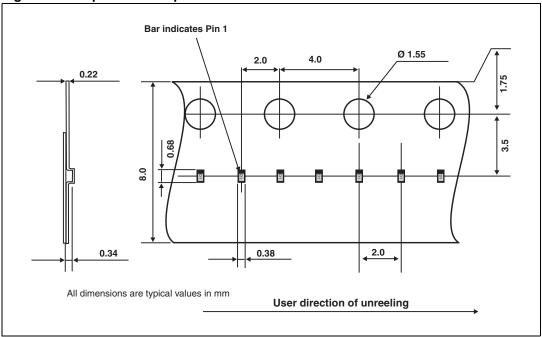
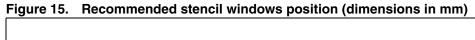
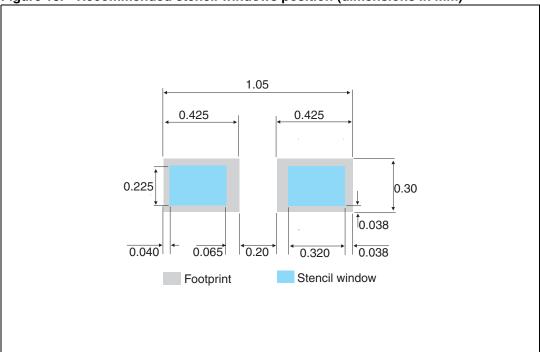


Figure 14. Tape and reel specifications

Recommendation on PCB assembly 4

4.1 Stencil opening design





4.2 Solder paste

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- Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
- "No clean" solder paste is recommended. 2.
- 3. Offers a high tack force to resist component movement during high speed
- 4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
- 3. Standard tolerance of \pm 0.05 mm is recommended.
- 4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

- To control the solder paste amount, the closed via is recommended instead of open vias.
- The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

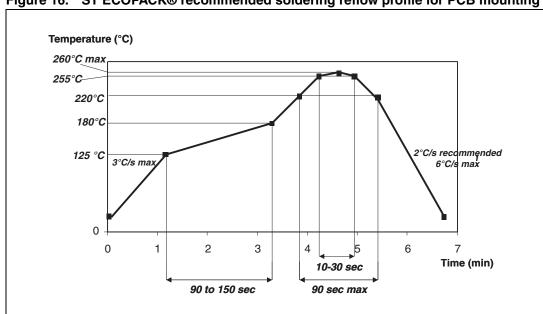


Figure 16. ST ECOPACK® recommended soldering reflow profile for PCB mounting

Note: Minimize air convection currents in the reflow oven to avoid component movement.

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5 Ordering information

Table 4. Ordering information

Order code	Marking	Weight	Base qty	Delivery mode
ESDALC6V1-1U2	L1 ⁽¹⁾	0.124 mg	15000	Tape and reel

^{1.} The marking can be rotated by multiples of 90° to differentiate assembly location

6 Revision history

 Table 5.
 Document revision history

Date	Revision	Changes
07-Oct-2008	1	Initial release.
25-Jan-2010	2	Updated base qty <i>Table 4</i> .
22-Sep-2011 3		Updated package illustrations <i>on page 1</i> and in <i>Table 3</i> for Pin 1 available forms.

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