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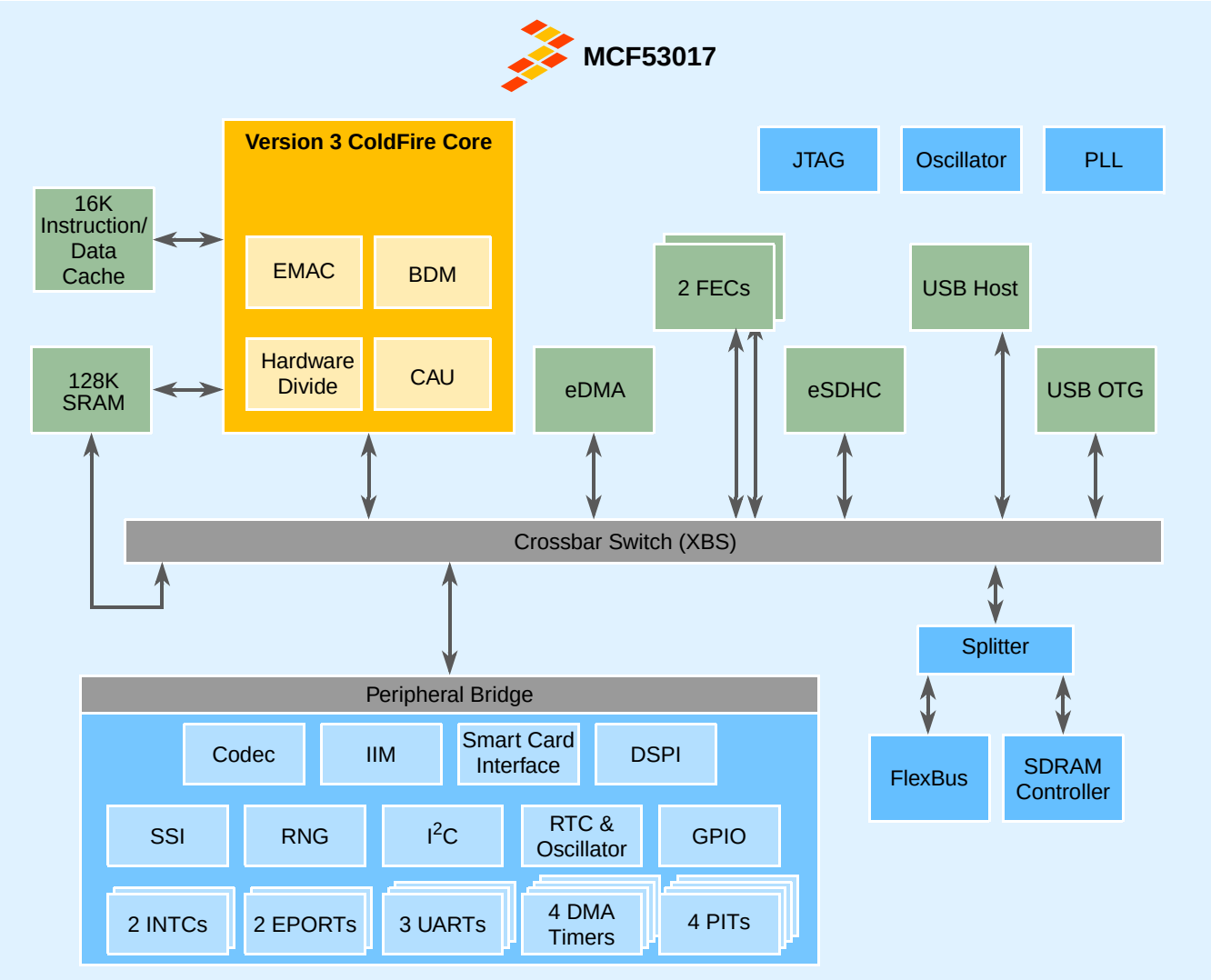


LEGEND

BDM	– Background debug module	**IIM**	– IC identification module
CAU	– Cryptography acceleration unit	**INTC**	– Interrupt controller
DSPI	– DMA serial peripheral interface	**JTAG**	– Joint Test Action Group interface
eDMA	– Enhanced direct memory access module	**PCI**	– Peripheral Component Interconnect
eSDHC	– Enhanced Secure Digital host controller	**PIT**	– Programmable interrupt timers
EMAC	– Enchanced multiply-accumulate unit	**PLL**	– Phase locked loop module
EPORT	– Edge port module	**RNG**	– Random number generator
FEC	– Fast Ethernet Controller	**RTC**	– Real time clock
GPIO	– General purpose input/output module	**SSI**	– Synchronous serial interface
I^2C	– Inter-Integrated Circuit	**USB OTG**	– Universal Serial Bus On-the-Go controller

1 MCF5301*x* Family Comparison

The following table compares the various device derivatives available within the MCF5301*x* family.

Table 1. MCF5301*x* Family Configurations

Module	MCF53010	MCF53011	MCF53012	MCF53013	MCF53014	MCF53015	MCF53016	MCF53017
Version 3 ColdFire Core with EMAC (enhanced multiply-accumulate unit)	•	•	•	•	•	•	•	•
Core (system) clock	up to 240 MHz							
Peripheral and external bus clock (Core clock ÷ 3)	up to 80 MHz							
Performance (Dhrystone/2.1 MIPS)	up to 211							
Unified data/instruction cache	16 Kbytes							
Static RAM (SRAM)	128 Kbytes							
Voice-over-IP software	—	—	•	•	—	—	•	•
Cryptography acceleration unit (CAU)	—	•	—	•	—	•	—	•
Random number generator	—	•	—	•	—	•	—	•
Smart card interface (SIM)	1 port				2 ports			
Voice-band audio codec	•	•	•	•	•	•	•	•
Integrated audio amplifiers	—	—	—	—	•	•	•	•
IC identification module (IIM)	2 Kbits							
Enhanced Secure Digital host controller (eSDHC)	•	•	•	•	•	•	•	•
SDR/DDR SDRAM controller	•	•	•	•	•	•	•	•
FlexBus external interface	•	•	•	•	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•	•	•	•	•
USB 2.0 Host	—	—	—	—	•	•	•	•
Synchronous serial interface (SSI)	•	•	•	•	•	•	•	•
Fast Ethernet controller (FEC)	2	2	2	2	2	2	2	2
UARTs	3	3	3	3	3	3	3	3
I^2C	•	•	•	•	•	•	•	•
DSPI	•	•	•	•	•	•	•	•
Real-time clock	•	•	•	•	•	•	•	•
32-bit DMA timers	4	4	4	4	4	4	4	4
Watchdog timer (WDT)	•	•	•	•	•	•	•	•
Periodic interrupt timers (PIT)	4	4	4	4	4	4	4	4
Edge port module (EPORT)	•	•	•	•	•	•	•	•
Interrupt controllers (INTC)	2	2	2	2	2	2	2	2

Table 1. MCF5301*x* Family Configurations (continued)

Module	MCF53010	MCF53011	MCF53012	MCF53013	MCF53014	MCF53015	MCF53016	MCF53017
16-channel direct memory access (DMA)	•	•	•	•	•	•	•	•
General purpose I/O Module (GPIO)	•	•	•	•	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•	•	•	•
Package	208 LQFP				256 MAPBGA			

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF53010CQT240	MCF53010 Microprocessor	208 LQFP	240 MHz	–40° to +85° C
MCF53011CQT240	MCF53011 Microprocessor			
MCF53012CQT240	MCF53012 Microprocessor			
MCF53013CQT240	MCF53013 Microprocessor			
MCF53014CMJ240J	MCF53014 Microprocessor	256 MAPBGA		
MCF53015CMJ240J	MCF53015 Microprocessor			
MCF53016CMJ240J	MCF53016 Microprocessor			
MCF53017CMJ240J	MCF53017 Microprocessor			
The following are not available from Freescale for import or sale in the United States prior to September 2010				
MCF53014CMJ240	MCF53014 Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C
MCF53015CMJ240	MCF53015 Microprocessor			
MCF53016CMJ240	MCF53016 Microprocessor			
MCF53017CMJ240	MCF53017 Microprocessor			

3 Hardware Design Considerations

3.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 1 should be connected between the board IV_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated PV_{DD} pin as possible. The 10-ohm resistor in the given filter is required, do not implement the filter circuit using only capacitors. The PV_{DD} pins draw very little current, so concerns regarding voltage loss across the 10-ohm resistor are not valid.

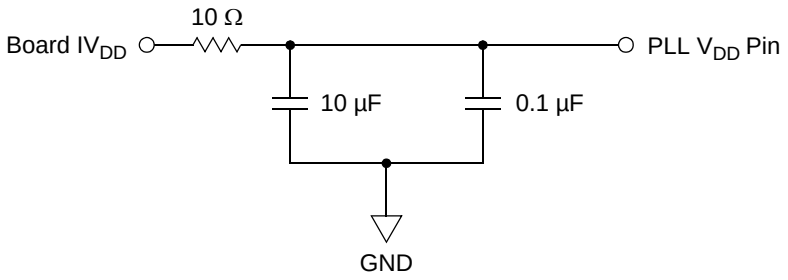


Figure 1. System PLL V_{DD} Power Filter

3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 2 should be connected between the board EV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

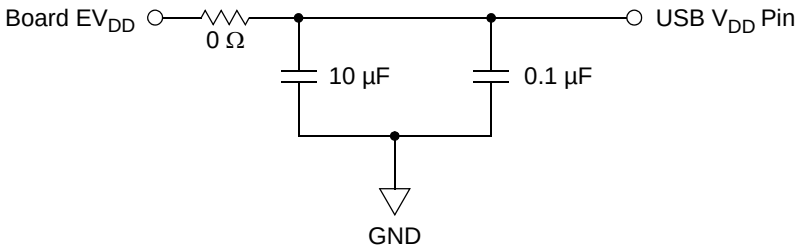


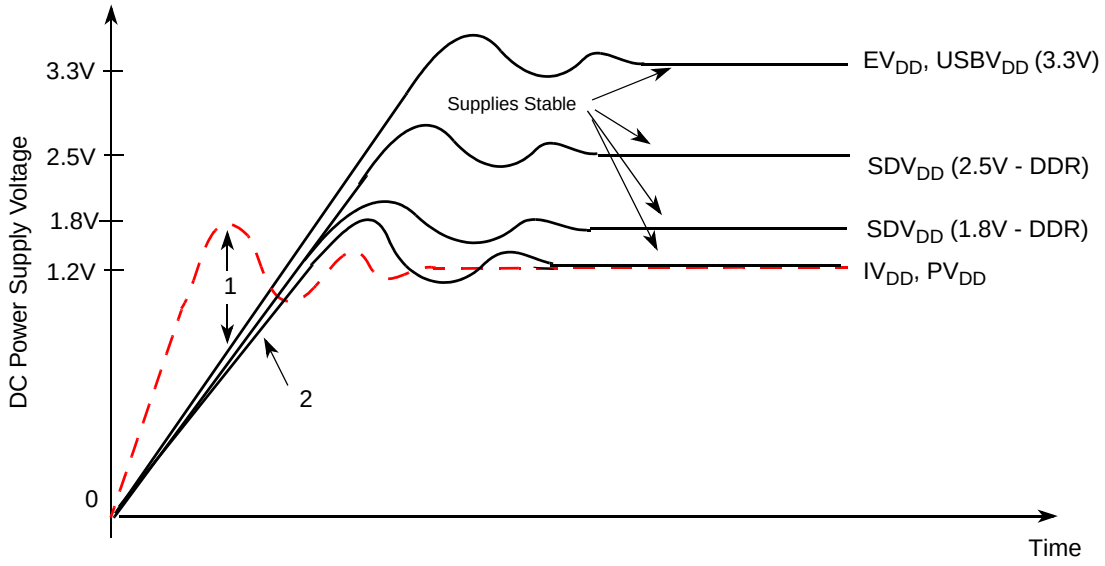
Figure 2. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

3.3 Supply Voltage Sequencing

Figure 3 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (PV_{DD}), and internal logic / core V_{DD} (IV_{DD}). The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.



Notes:
1. IV_{DD} should not exceed EV_{DD}, SDV_{DD} or PV_{DD} by more than 0.4V at any time, including power-up.
2. Recommended that IV_{DD}/PV_{DD} should track EV_{DD}/SDV_{DD} up to 0.9V then separate for completion of ramps
3. Input voltage must not be greater than the supply voltage (EV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 3. Supply Voltage Sequencing and Separation Cautions

3.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with the IV_{DD} at 0V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD}, SDV_{DD} or PV_{DD} by more than 0.4V during power ramp up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. IV_{DD}/PV_{DD} and EV_{DD}/SDV_{DD} should track up to 0.9V and then separate for the completion of ramps with EV_{DD}/SDV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

3.3.2 Power Down Sequence

If IV_{DD}/PV_{DD} are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PV_{DD} power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or PV_{DD} going low by more than 0.4V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/PV_{DD} to 0V.
2. Drop EVDD/SDVDD supplies.

3.4 Power Consumption Specifications

Estimated maximum RUN mode power consumption measurements are shown in the below figure.

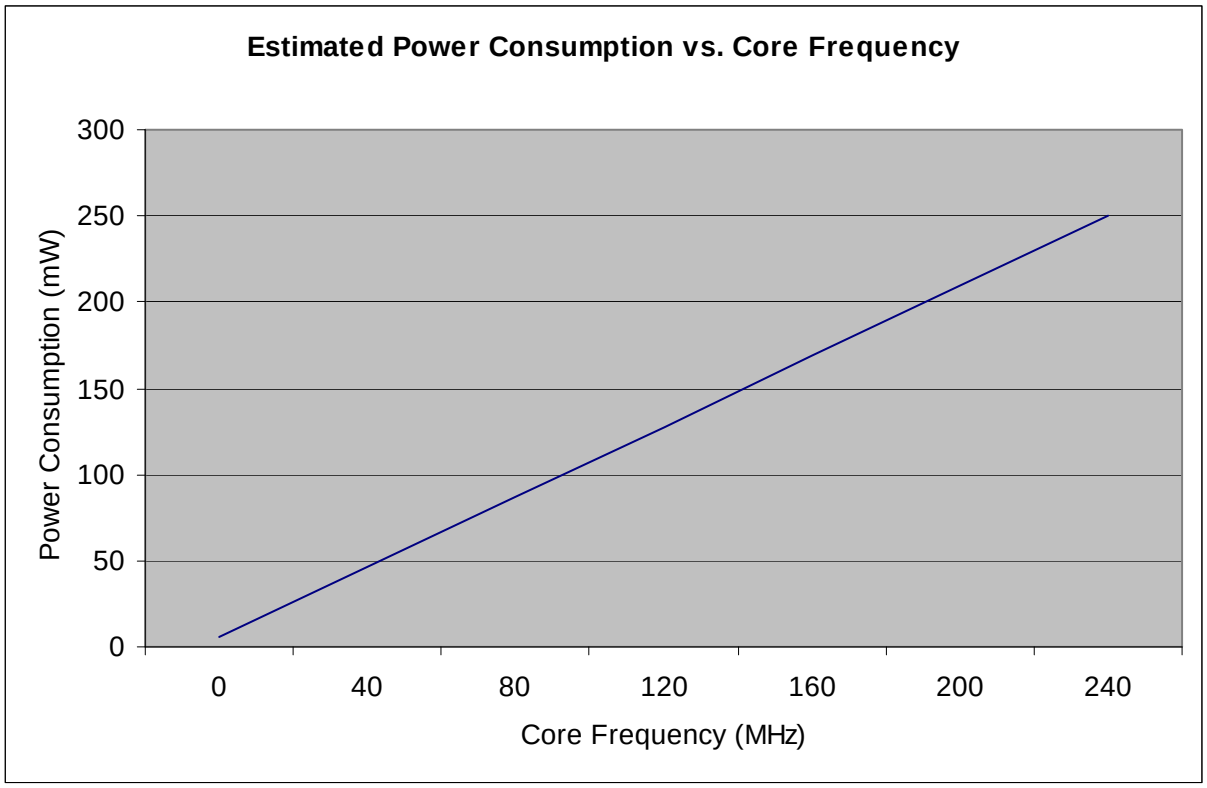


Figure 4. Estimated Maximum RUN Mode Power Consumption

Table 3 lists estimated maximum power and current consumption for the device in various operating modes.

Table 3. Estimated Maximum Power Consumption Specifications

Characteristic	Symbol	Typical	Max	Unit
Run Mode — Total Power Dissipation Static Dynamic		— — —	TBD TBD TBD	mW mW mW
Core Operating Supply Current [1] Run Mode	I_{DD}	—	82.9	mA
Pad Operating Supply Current Run Mode (application dependent) Wait Mode Stop Mode	EI_{DD}	— — —	TBD TBD TBD	mA mA mA

1 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

Table 4. Current Measurementas at Different VCO vs. Core Frequencies

Stop Mode	480VCO, 240MHz core	240VCO, 120MHz core	480VCO, 120MHz core	480VCO, 48MHz core	Limp Mode, 20HMHz crystal
Executing	55.3mA	28.36mA	30.00mA	13.6mA	5.90mA
Run	39.5mA	20.3mA	22.02mA	10.29mA	4.42mA
Wait	16.28mA	8.53mA	10.23mA	5.53mA	2.43mA
Doze	16.19mA	8.53mA	10.18mA	5.55mA	2.41mA
Stop(0)	8.41mA	4.60mA	6.29mA	3.90mA	1.78mA
Stop(1)	8.13mA	4.48mA	6.15mA	3.88mA	1.77mA
Stop(2)	1.83mA	1.86mA	1.87mA	1.82mA	1.76mA
Stop(3)	0.65mA	0.66mA	0.67mA	0.67mA	0.65mA

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF5301*x* pins grouped by function. The “Dir” column is the direction for the primary function of the pin only. Refer to Section 4.2, “Pinout—208 LQFP,” and Section 4.3, “Pinout–256 MAPBGA,” for package diagrams. For a more detailed discussion of the MCF3xx*x* signals, consult the *MCF5301x Reference Manual* (MCF53017RM).

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., FB_A23), while designations for multiple signals within a group use brackets (i.e., FB_A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO will default to their GPIO functionality. See Table 5 for a list of the exceptions.

Table 5. Special-Case Default Signal Functionality

Pin	Default Signal
$\overline{\text{FB\_BE/BWE}}$[3:0]	$\overline{\text{FB\_BE/BWE}}$[3:0]
$\overline{\text{FB\_CS}}$[3:0]	$\overline{\text{FB\_CS}}$[3:0]
$\overline{\text{FB\_OE}}$	$\overline{\text{FB\_OE}}$
$\overline{\text{FB\_TA}}$	$\overline{\text{FB\_TA}}$
FB_R/$\overline{\text{W}}$	FB_R/$\overline{\text{W}}$
$\overline{\text{FB\_TS}}$	$\overline{\text{FB\_TS}}$

Table 6. MCF5301*x* Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Reset								
$\overline{\text{RESET}}$	—	—	—	U	I	EVDD	41	M3
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	42	N1
Clock								
EXTAL	—	—	—	—	I	EVDD	49	T2
XTAL	—	—	—	U[3]	O	EVDD	50	T3
Mode Selection								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	55, 17	J5, G5
FlexBus								
FB_A[23:22]	—	$\overline{\text{FB\_CS}}$[3:2]	—	—	O	SDVDD	115, 114	P16, N16
FB_A[21:16]	—	—	—	—	O	SDVDD	113–108	R16, N14, N15, P15-13
FB_A[15:14]	—	SD_BA[1:0]	—	—	O	SDVDD	107, 106	R15, R14
FB_A[13:11]	—	SD_A[13:11]	—	—	O	SDVDD	105–103	N13, R12, R13
FB_A10	—	—	—	—	O	SDVDD	100	N12
FB_A[9:0]	—	SD_A[9:0]	—	—	O	SDVDD	99–97 95–89	P12, T14, T15, R11, P11, N11, T13, R10, T11, T12
FB_D[31:16]	—	SD_D[31:16]	—	—	I/O	SDVDD	208–198, 57–62, 64, 65	B3, A2, D6, C5, B4, A3, B5, C6, D12, C14, B14, C13, D11, B13, A14, A13
FB_D[15:0]	—	FB_D[31:16]	—	—	I/O	SDVDD	182–189, 177–170	B9, A9, A8, D7, B8, C8, D8, B7, C10, A10, B10, D10, C11, A11, B11, A12
FB_CLK	—	—	—	—	O	SDVDD	153	D13
$\overline{\text{FB\_BE/BWE}}$[3:0]	PBE[3:0]	SD_DQM[3:0]	—	—	O	SDVDD	197, 166, 179, 178	A4, B12, C9, D9
$\overline{\text{FB\_CS}}$[5:4]	PCS[5:4]	—	—	—	O	SDVDD	—	B6, C7
$\overline{\text{FB\_CS1}}$	PCS1	$\overline{\text{SD\_CS1}}$	—	—	O	SDVDD	5	D2
$\overline{\text{FB\_CS0}}$	PCS0	$\overline{\text{FB\_CS4}}$	—	—	O	SDVDD	6	C2
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	SDVDD	1	D4
$\overline{\text{FB\_TA}}$	PFBCTL2	—	—	U	I	SDVDD	3	B2
FB_R/$\overline{\text{W}}$	PFBCTL1	—	—	—	O	SDVDD	2	C3
$\overline{\text{FB\_TS}}$	PFBCTL0	$\overline{\text{DACK0}}$	—	—	O	SDVDD	4	D3
SDRAM Controller								
SD_A10	—	—	—	—	O	SDVDD	206	C4

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
SD_CAS	—	—	—	—	O	SDVDD	154	D15
SD_CKE	—	—	—	—	O	SDVDD	151	B15
SD_CLK	—	—	—	—	O	SDVDD	190	A7
SD_CLK	—	—	—	—	O	SDVDD	191	A6
SD_CS0	—	—	—	—	O	SDVDD	155	A15
SD_DQS[1:0]	—	—	—	—	O	SDVDD	196, 167	C12, A5
SD_RAS	—	—	—	—	O	SDVDD	152	C15
SD_SDR_DQS	—	—	—	—	I	SDVDD	207	D5
SD_WE	—	—	—	—	O	SDVDD	150	D14
External Interrupts Port 1[4,5]								
IRQ1DEBUG[7:4]	PIRQ1DEBUG [7:4]	DDATA[3:0]	—	—	I	EVDD	—	H1, H4-2
IRQ1DEBUG[3:0]	PIRQ1DEBUG [3:0]	PST[3:0]	—	—	I	EVDD	—	K14, H14, K15, J13
IRQ1FEC7	PIRQ1FEC7	RMII1_CRS_DV	MII0_CRS	—	I	EVDD	29	J1
IRQ1FEC6	PIRQ1FEC6	RMII1_RXER	MII0_RXCLK	—	I	EVDD	30	J2
IRQ1FEC5	PIRQ1FEC5	RMII1_TXEN	MII0_TXCLK	—	I	EVDD	31	K4
IRQ1FEC4	PIRQ1FEC4	RMII1_REF_CLK	—	D	I	EVDD	32	J3
IRQ1FEC[3:2]	PIRQ1FEC[3:2]	RMII1_RXD[1:0]	MII0_RXD[3:2]	—	I	EVDD	33, 34	J4, K1
IRQ1FEC[1:0]	PIRQ1FEC[1:0]	RMII1_TXD[1:0]	MII0_TXD[3:2]	—	I	EVDD	35, 36	K2, L1
External Interrupts Port 0[5]								
IRQ07	PIRQ07	—	—	U	I	EVDD	10	E4
IRQ06	PIRQ06	—	USB_CLKIN	U	I	EVDD	—	L13
IRQ04	PIRQ04	DREQ0	—	U	I	EVDD	19	D1
IRQ01	PIRQ01	DREQ1	—	U	I	EVDD	11	F4
Enhanced Secure Digital Host Controller								
SDHC_DAT3	PSDHC5	—	—	UD	I/O	EVDD	60	N4
SDHC_DAT[2:0]	PSDHC[4:2]	—	—	U	I/O	EVDD	61–63	R5, N6, N5
SDHC_CMD	PSDHC1	—	—	U	I/O	EVDD	59	R4
SDHC_CLK	PSDHC0	—	—	—	O	EVDD	58	R3

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Codec								
CODEC_ADCN	—	AMP_MICN	—	—	I		85	P10
CODEC_ADCP	—	AMP_MICP	—	—	I		84	P9
CODEC_BGRVREF	—	—	—	—	I		86	N9
CODEC_DACN	—	AMP_HSN	—	—	O		75	R7
CODEC_DACP	—	AMP_HSP	—	—	O		67	R6
CODEC_REGBYP	—	—	—	—	I		81	P6
CODEC_REFN	—	—	—	—	I		79	P8
CODEC_REFP	—	—	—	—	I		78	P7
CODEC_VAG	—	—	—	—	I		82	N7
Amplifiers								
AMP_HPDUMMY	—	—	—	—	O		—	R9
AMP_HPOUT	—	—	—	—	O		—	R8
AMP_SPKRN	—	—	—	—	O		—	T9
AMP_SPKRP	—	—	—	—	O		—	T7
Smart Card interface 1								
SIM1_DATA	PSIM14	SSI_TXD	U1TXD	UD	I/O	EVDD	141	E14
SIM1_VEN	PSIM13	SSI_RXD	U1RXD	UD	O	EVDD	142	D16
SIM1_RST	PSIM12	SSI_FS	$\overline{\text{U1RTS}}$	—	O	EVDD	144	E13
SIM1_PD	PSIM11	SSI_BCLK	$\overline{\text{U1CTS}}$	—	O	EVDD	145	E15
SIM1_CLK	PSIM10	SSI_MCLK	—	—	O	EVDD	143	F13
Smart Card interface 0								
SIM0_DATA	PSIM04	—	—	—	I/O	EVDD	—	L3
SIM0_VEN	PSIM03	—	—	—	O	EVDD	—	M2
SIM0_RST	PSIM02	—	—	—	O	EVDD	—	F16
SIM0_PD	PSIM01	—	—	—	O	EVDD	—	L14
SIM0_CLK	PSIM00	—	—	—	O	EVDD	—	M16
USB On-the-Go								
USBO_DM	—	—	—	—	O	USB VDD	148	C16
USBO_DP	—	—	—	—	O	USB VDD	149	B16

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
USB Host								
USBH_DM	—	—	—	—	O	USB VDD	—	B1
USBH_DP	—	—	—	—	O	USB VDD	—	C1
FEC 1								
RMII1_MDC	PFECI2C5	—	MII0_TXER	—		EVDD	22	E1
RMII1_MDIO	PFECI2C4	—	MII0_COL	—		EVDD	23	F1
FEC 0								
RMII0_CRS_DV	PFEC06	—	MII0_RXDV	—		EVDD	131	G16
RMII0_RXD[1:0]	PFEC0[5:4]	—	MII0_RXD[1:0]	—		EVDD	130, 129	H15, H16
RMII0_RXER	PFEC03	—	MII0_RXER	—		EVDD	127	J16
RMII0_TXD[1:0]	PFEC0[2:1]	—	MII0_TXD[1:0]	—		EVDD	125, 124	J15, J14
RMII0_TXEN	PFEC00	—	MII0_TXEN	D		EVDD	123	K16
RMII0_MDC	PFECI2C3	—	MII0_MDC	—		EVDD	133	G14
RMII0_MDIO	PFECI2C2	—	MII0_MDIO	—		EVDD	132	G15
Real Time Clock								
RTC_EXTAL	—	—	—	—	I	EVDD	—	P1
RTC_XTAL	—	—	—	—	O	EVDD	—	R1
Synchronous Serial Interface								
SSI_RXD	PSSI4	—	U1RXD	UD	I	EVDD	—	N3
SSI_TXD	PSSI3	—	U1TXD	UD	O	EVDD	—	P3
SSI_FS	PSSI2	—	$\overline{\text{U1RTS}}$	—	I/O	EVDD	—	R2
SSI_MCLK	PSSI1	—	SSI_CLKIN	—	O	EVDD	—	P4
SSI_BCLK	PSSI0	—	$\overline{\text{U1CTS}}$	—	I/O	EVDD	—	P5
I²C								
I2C_SCL	PFECI2C1	U2RXD	RMII1_MDC	U	I/O	EVDD	37	M1
I2C_SDA	PFECI2C0	U2TXD	RMII1_MDIO	U	I/O	EVDD	38	K3
DSPI								
DSPI_PCS3	PDSPI6	USBH_VBUS_EN	—	—	I/O	EVDD	—	P2
DSPI_PCS2	PDSPI5	USBH_VBUS_OC	—	—	I/O	EVDD	—	N2

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
DSPI_PCS1	PDSPI4	—	—	—	I/O	EVDD	140	F14
DSPI_PCS0/$\overline{SS}$	PDSPI3	$\overline{U2RTS}$	—	U	I/O	EVDD	137	G13
DSPI_SCK	PDSPI2	$\overline{U2CTS}$	—	—	I/O	EVDD	134	H13
DSPI_SIN	PDSPI1	U2RXD	—	—	I	EVDD	136	E16
DSPI_SOUT	PDSPI0	U2TXD	—	—	O	EVDD	135	F15
UARTs								
U2RXD	PUART5	—	—	—	I	EVDD	14	E2
U2TXD	PUART4	—	—	—	O	EVDD	18	F2
$\overline{U0CTS}$	PUART3	USBO_VBUS_EN	USB_PULLUP	—	I	EVDD	20	G4
$\overline{U0RTS}$	PUART2	USBO_VBUS_OC	—	—	O	EVDD	21	G3
U0RXD	PUART1	—	—	—	I	EVDD	27	G2
U0TXD	PUART0	—	—	—	O	EVDD	28	G1
DMA Timers								
T3IN	PTIMER3	T3OUT	IRQ03	—	I	EVDD	13	F3
T2IN	PTIMER2	T2OUT	IRQ02	—	I	EVDD	12	E3
T1IN	PTIMER1	T1OUT	$\overline{DACK1}$	—	I	EVDD	122	K13
T0IN	PTIMER0	T0OUT	CODEC_ALTCLK	—	I	EVDD	121	L16
BDM/JTAG[6]								
ALLPST	PDEBUG	—	—	—	O	EVDD	43	—
JTAG_EN	—	—	—	D	I	EVDD	64	M8
PSTCLK	—	TCLK	—	—	I	EVDD	65	T5
DSI	—	TDI	—	U	I	EVDD	66	T4
DSO	—	TDO	—	—	O	EVDD	120	M15
$\overline{BKPT}$	—	TMS	—	U	I	EVDD	119	M14
DSCLK	—	$\overline{TRST}$	—	U	I	EVDD	118	L15

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Test								
TEST	—	—	—	D	I	EVDD	146	F12
Power Supplies								
IVDD	—	—	—	—	—	—	16, 44, 69, 77, 128, 169, 193	E9, F8, F9, H5, H6, H11, H12, J6, J11, L8, L9
EVDD	—	—	—	—	—	—	9, 24, 26, 40, 47, 51, 54, 57, 74, 126, 139, 195	F5, G6, G11, G12, J12, K6, K11, K12, L5-7, L10-12, M5-7, M12
SD_VDD	—	—	—	—	—	—	7, 102, 116, 156, 163, 181, 208	E5, E6, E10-12, F6, F7, F10, F11
VDD_OSC_A_PLL	—	—	—	—	—	—	46	M4
VDD_USBO	—	—	—	—	—	—	147	E7
VDD_USBH	—	—	—	—	—	—	—	E8
VDD_RTC	—	—	—	—	—	—	—	
AVDD_CODEC	—	—	—	—	—	—	80	N8
AVDD_SPKR	—	—	—	—	—	—	—	T8
VDD_EPM	—	—	—	—	—	—	96	M9
VSTBY_SRAM	—	—	—	—	—	—	—	L2
VSTBY_RTC	—	—	—	—	—	—	—	L4
VSS	—	—	—	—	—	—	8, 15, 25, 39, 45, 48, 52, 53, 56, 68, 73, 76, 101, 117, 138, 168, 180, 192, 194	A1, A16, G7-10, H7-10, J7-10, K7-10, T1, T16
VSS_CODEC	—	—	—	—	—	—	83	N10
AVSS_SPKR_HDST	—	—	—	—	—	—	—	T6
AVSS_SPKR_HP	—	—	—	—	—	—	—	T10

1 Pull-ups are generally only enabled on pins with their primary function, except as noted.

2 Refers to pin's primary function.

3 Enabled only in oscillator bypass mode (internal crystal oscillator is disabled).

4 The edge port 1 signals are the primary functions on two sets of pins (IRQ1FEC*n* and IRQ1DEBUG*n*). If an IRQ1 function is configured on both pins, the IRQ1FEC*n* pin takes priority. The corresponding IRQ1DEBUG*n* pin is disconnected internally from the edge port 1 module.

5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

6 If JTAG_EN is asserted, these pins default to alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

4.2 Pinout—208 LQFP

The pinout for the 208 LQFP devices is shown in Figure 5 and Figure 6.

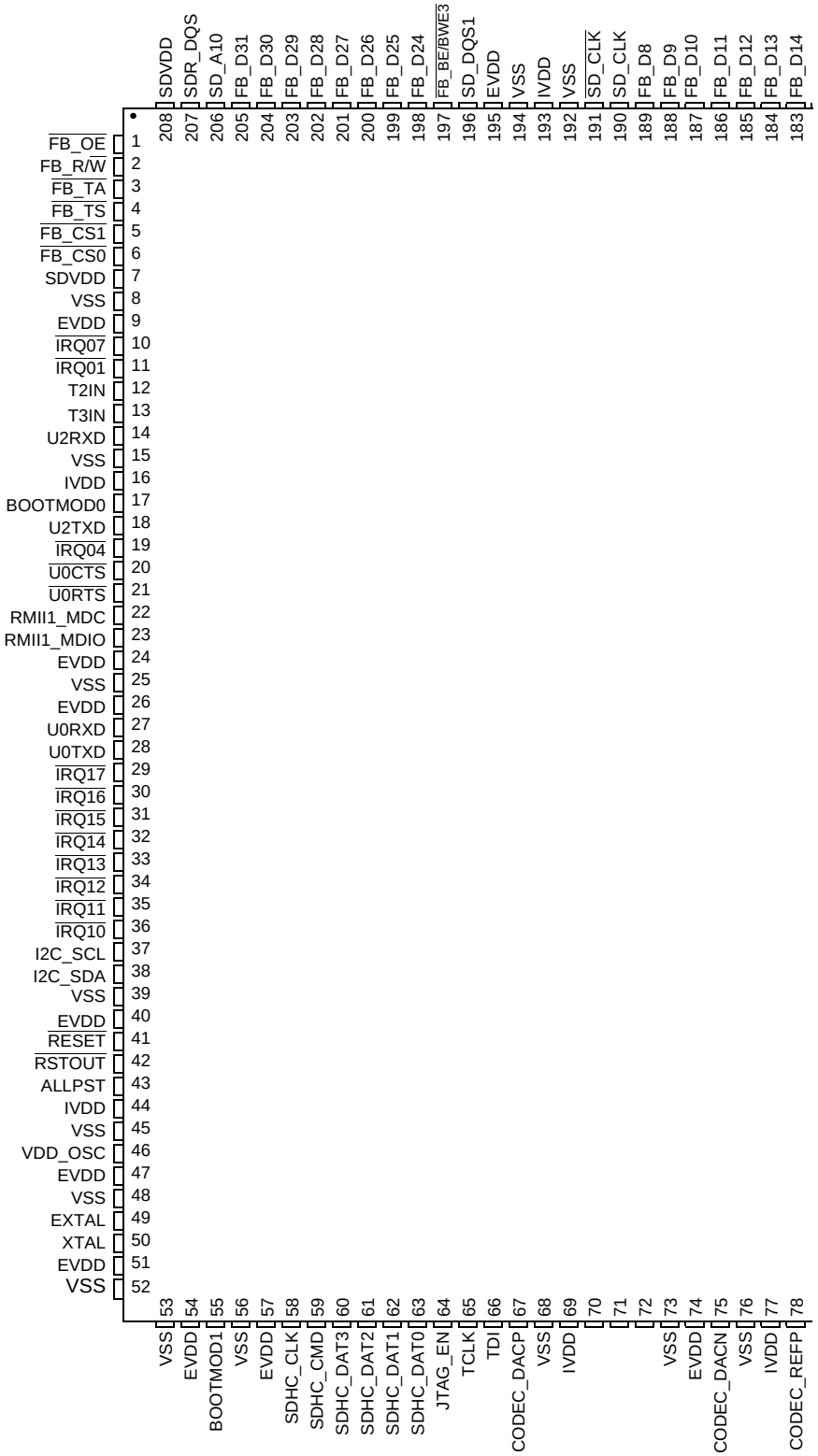


Figure 5. MCF53010, MCF53011, MCF53012, and MCF53013 Pinout Top View, Left (208 QFP)

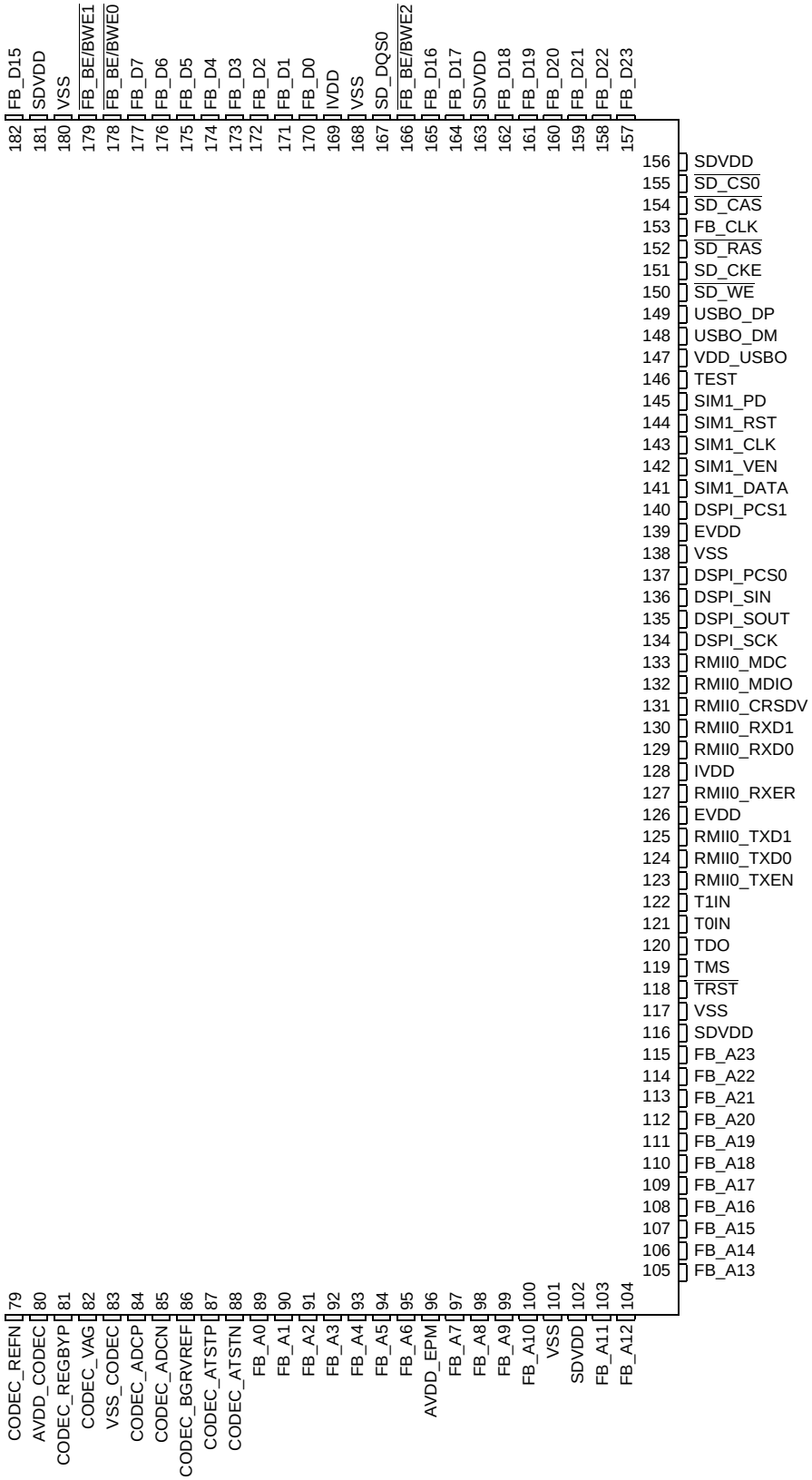


Figure 6. MCF53010, MCF53011, MCF53012, and MCF53013 Pinout Top View, Right (208 QFP)

4.3 Pinout–256 MAPBGA

The pinout for the MCF53014, MCF53015, MCF53016, and MCF53017 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FB_D 30	FB_D 26	FB_BE/ BWE3	SD_ DQS1	SD_ CLK	SD_ CLK	FB_D 13	FB_D 14	FB_D 6	FB_D 2	FB_D 0	FB_D 16	FB_D 17	SD_CS	VSS	A
B	USBH_ DM	FB_TA	FB_D 31	FB_D 27	FB_D 25	FB_CS5	FB_D 8	FB_D 11	FB_D 15	FB_D 5	FB_D 1	FB_BE/ BWE2	FB_D 18	FB_D 21	SD_ CKE	USBO_ DP	B
C	USBH_ DP	FB_CS0	FB_R/W	SD_A10	FB_D 28	FB_D 24	FB_CS4	FB_D 10	FB_BE/ BWE1	FB_D 7	FB_D 3	SD_ DQS2	FB_D 20	FB_D 22	SD_ RAS	USBO_ DM	C
D	IRQ04	FB_CS1	FB_TS	FB_OE	SD_SDR _DQS	FB_D 29	FB_D 12	FB_D 9	FB_BE/ BWE0	FB_D 4	FB_D 19	FB_D 23	FB_CLK	SD_ WE	SD_ CAS	SIM1_ VEN	D
E	RMII1_ MDC	U2RXD	T2IN	IRQ07	SDVDD	SDVDD	VDD_ USBO	VDD_ USBH	IVDD	SDVDD	SDVDD	SDVDD	SIM1_ RST	SIM1_ DATA	SIM1_ PD	DSPI_ SIN	E
F	RMII1_ MDIO	U2TXD	T3IN	IRQ01	EVDD	SDVDD	SDVDD	IVDD	IVDD	SDVDD	SDVDD	TEST	SIM1_ CLK	DSPI_ PCS1	DSPI_ SOUT	SIM0_ RST	F
G	U0TXD	U0RXD	U0RTS	U0CTS	BOOT MOD0	EVDD	VSS	VSS	VSS	VSS	EVDD	EVDD	DSPI_ PCS0	RMII0_ MDC	RMII0_ MDIO	RMII0_ CRSDV	G
H	IRQ1 DEBUG7	IRQ1 DEBUG4	IRQ1 DEBUG5	IRQ1 DEBUG6	IVDD	IVDD	VSS	VSS	VSS	VSS	IVDD	IVDD	DSPI_ SCK	IRQ1 DEBUG2	RMII0_ RXD1	RMII0_ RXD0	H
J	IRQ1 FEC7	IRQ1 FEC6	IRQ1 FEC4	IRQ1 FEC3	BOOT MOD1	IVDD	VSS	VSS	VSS	VSS	IVDD	EVDD	IRQ1 DEBUG0	RMII0_ TXD0	RMII0_ TXD1	RMII0_ RXER	J
K	IRQ1 FEC2	IRQ1 FEC1	I2C_ SDA	IRQ1 FEC5	NC	EVDD	VSS	VSS	VSS	VSS	EVDD	EVDD	T1IN	IRQ1 DEBUG3	IRQ1 DEBUG1	RMII0_ TXEN	K
L	IRQ1 FEC0	VSTBY_ SRAM	SIM0_ DATA	VSTBY_ RTC	EVDD	EVDD	EVDD	IVDD	IVDD	EVDD	EVDD	EVDD	IRQ06	SIM0_ PD	TRST	T0IN	L
M	I2C_ SCL	SIM0_ VEN	RESET	VDD_ OSC_A_ PLL	EVDD	EVDD	EVDD	JTAG_ EN	VDD_ EPM	NC	NC	EVDD	NC	TMS	TDO	SIM0_ CLK	M
N	RST OUT	DSPI_ PCS2	SSI_ RXD	SDHC_ DAT3	SDHC_ DAT0	SDHC_ DAT1	CODEC _VAG	AVDD_ CODEC	CODEC _BGR VREF	VSS_ CODEC	FB_A4	FB_A10	FB_A13	FB_A20	FB_A19	FB_A22	N
P	RTC_ EXTAL	DSPI_ PCS3	SSI_ TXD	SSI_ MCLK	SSI_ BCLK	CODEC _REG BYP	CODEC _REFP	CODEC _REFN	CODEC _ADCP	CODEC _ADCN	FB_A5	FB_A9	FB_A16	FB_A17	FB_A18	FB_A23	P
R	RTC_ XTAL	SSI_FS	SDHC_ CLK	SDHC_ CMD	SDHC_ DAT2	CODEC _DACP	CODEC _DACN	AMP_ HP OUT	AMP_ HP DUMMY	FB_A2	FB_A6	FB_A12	FB_A11	FB_A14	FB_A15	FB_A21	R
T	VSS	EXTAL	XTAL	TDI	TCLK	AVSS_ SPKR_ HDST	AMP_ SPKRP	AVDD_ SPKR	AMP_ SPKRN	AVSS_ SPKR_ HP	FB_A1	FB_A0	FB_A3	FB_A8	FB_A7	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 7. MCF53014, MCF53015, MCF53016, and MCF53017 Pinout (256 MAPBGA)

5 Preliminary Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5301*x* microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	–0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	–0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	–0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	–0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	–0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L – T_H)	–40 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

1 Functional operating conditions are given in Section 5.4, “DC Electrical Specifications.” Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > EV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Insure external EV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 8. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	208 LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	36[1,2]	38[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	32[1,2]	33[1,2]	°C/W
Junction to board		θ_{JB}	25[3]	29[3]	°C/W
Junction to case		θ_{JC}	14[4]	11[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	3[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 9. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with JEDEC JESD22-A114 specification.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 10. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.08	1.32	V
SRAM Standby Voltage	$SRAMV_{STBY}$	1.08	1.32	V
RTC Standby Voltage	$RTCV_{STBY}$	3.0	3.6	V
PLL Supply Voltage	$PLLV_{DD}$	3.0	3.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.70 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	$0.51 \times EV_{DD}$	$EV_{DD} + 0.3$	V
CMOS Input Low Voltage	EV_{IL}	$V_{SS} - 0.3$	$0.42 \times EV_{DD}$	V
CMOS Output High Voltage I_{OH} = –2.0 mA	EV_{OH}	$0.8 \times EV_{DD}$	—	V
CMOS Output Low Voltage I_{OL} = 2.0 mA	EV_{OL}	—	$0.2 \times EV_{DD}$	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 $SDV_{DD} \times 0.7$ Vref+0.15 2	 SDV_{DD}+0.3 SDV_{DD}+0.3 $SDV_{DD} + 0.3$	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 –0.3 –0.3 $V_{SS} - 0.3$	 $SDV_{DD} \times 0.3$ Vref+0.15 0.8	V

Table 10. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 SDVDD × 0.9 SDV_{DD} – 0.35 2.9	 — — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 SDV_{DD} × 0.1 0.35 0.4	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–2.5	2.5	µA
Weak Internal Pull-Up/Pull-down Device Current[1]	I_{APU}	10	315	µA
Selectable Weak Internal Pull-Up/Pull-down Device Current[2]	I_{APU}	25	150	µA
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 Refer to the signals section for pins having weak internal pull-up devices.
3 This parameter is characterized before qualification rather than 100% tested.

5.4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 8 should be connected between the board V_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

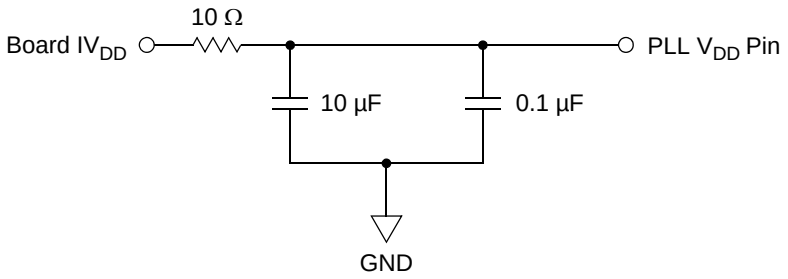


Figure 8. System PLL V_{DD} Power Filter

5.4.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 2 should be connected between the board EV_{DD} or IV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

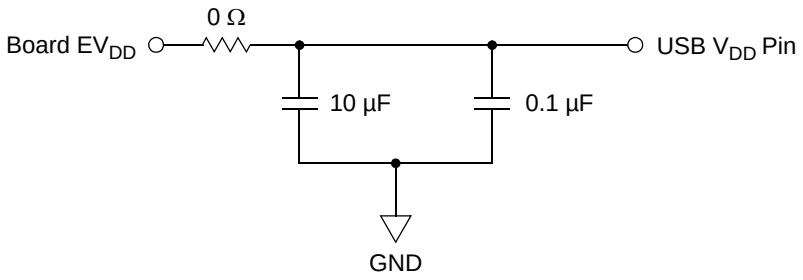


Figure 9. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

5.4.3 Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

5.4.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must powered up. IV_{DD} should not lead the EV_{DD}, SDV_{DD} or $PLLV_{DD}$ by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

5.4.3.2 Power Down Sequence

If IV_{DD}/$PLLV_{DD}$ are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLLV_{DD}$ power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/$PLLV_{DD}$ to 0 V.
2. Drop EV_{DD}/SDV_{DD} supplies.

5.5 Oscillator and PLL Electrical Characteristics

Table 11. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 14 14	 25[1] 48[1]	 MHz MHz
2	Core frequency CLKOUT Frequency[2]	f_{sys} $f_{sys/3}$	488×10^{-6} 163×10^{-6}	240 80	MHz MHz
3	Crystal Start-up Time[3, 4]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 $E_{VDD}/2$ + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} – 0.4 $E_{VDD}/2$ – 0.4	 V V
7	PLL Lock Time [3, 6]	t_{lpll}	—	750	us
8	Duty Cycle of reference [3]	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
12	Crystal capacitive load	C_L	—	See crystal spec	
13	Discrete load capacitance for XTAL	C_{L_XTAL}	—	$2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[7]	pF
14	Discrete load capacitance for EXTAL	C_{L_EXTAL}	—	$2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[7]	pF
17	CLKOUT Period Jitter, [3, 4, 7, 8, 9] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 TBD TBD	 % $f_{sys/3}$ % $f_{sys/3}$
18	Frequency Modulation Range Limit [3, 10, 11] (f_{sys}Max must not be exceeded)	C_{mod}	0.8	2.2	%$f_{sys/3}$
19	VCO Frequency. $f_{vco} = (f_{ref} \times PFD)/4$	f_{vco}	200	667	MHz

1 The maximum allowable input clock frequency when booting with the PLL enabled is 24MHz. For higher input clock frequencies the processor must boot in LIMP mode to avoid violating the maximum allowable CPU frequency.
2 All internal registers retain data at 0 Hz.
3 This parameter is guaranteed by characterization before qualification rather than 100% tested.
4 Proper PC board layout procedures must be followed to achieve specifications.
5 This parameter is guaranteed by design rather than 100% tested.
6 This specification is the PLL lock time only and does not include oscillator start-up time..
7 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

10 Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100kHz.

11 Modulation range determined by hardware design.

5.6 External Interface Timing Characteristics

Table 12 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 12 are shown in Figure 11 and Figure 12.

* The timings are also valid for inputs sampled on the negative clock edge.

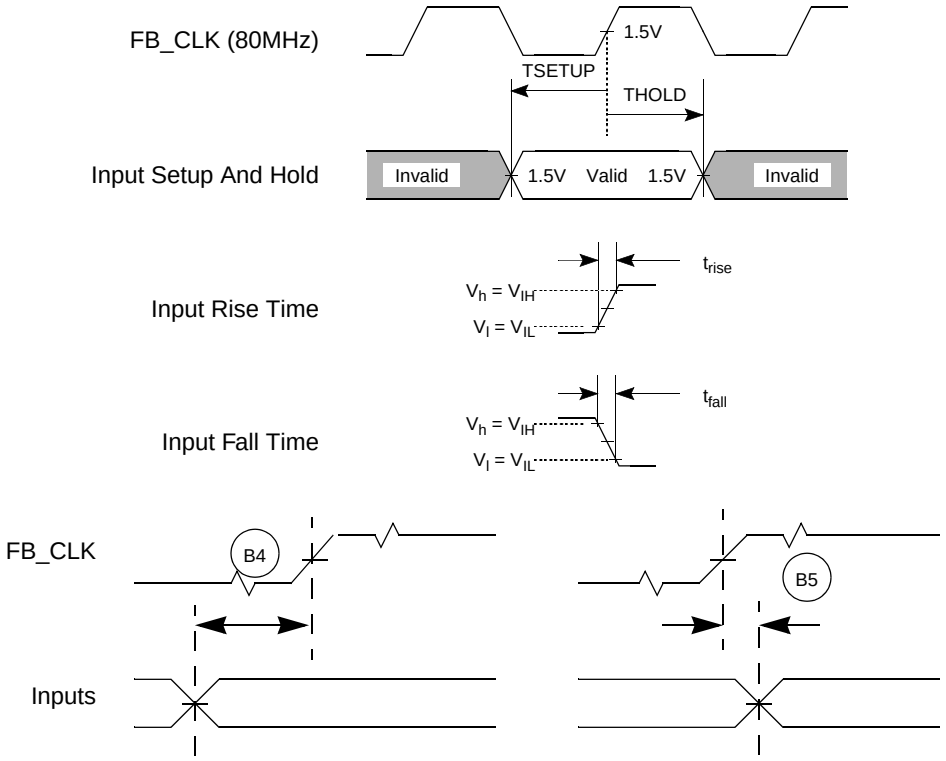


Figure 10. General Input Timing Requirements

5.6.1 FlexBus

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{FB\_CS}$[5:0]) which can be configured to be distributed between the FlexBus or SDRAM memory interfaces.

Chip-select, FB_CS0 can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is 1‘compatible with common ROM/flash memories.

5.6.1.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the system clock.

Table 12. FlexBus AC Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		—	80	Mhz	$f_{sys/3}$
FB1	Clock Period (FB_CLK)	t_{FBCK}	12.5	—	ns	t_{cyc}
FB2	Address, Data, and Control Output Valid (A[23:0], D[31:0], FB_CS[5:0], R/W, TS, BE/BWE[3:0] and OE)	$t_{FBCHDCV}$	—	7.0	ns	1
FB3	Address, Data, and Control Output Hold (A[23:0], D[31:0], FB_CS[5:0], R/W, TS, BE/BWE[3:0], and OE)	$t_{FBCHDCI}$	1	—	ns	1, 2
FB4	Data Input Setup	t_{DVFBCH}	3.5	—	ns	
FB5	Data Input Hold	t_{DIFBCH}	0	—	ns	
FB6	Transfer Acknowledge (TA) Input Setup	t_{CVFBCH}	4	—	ns	
FB7	Transfer Acknowledge (TA) Input Hold	t_{CIFBCH}	0	—	ns	

1 Timing for chip selects only applies to the FB_CS[5:0] signals. Please see Section 5.7.2, “DDR SDRAM AC Timing Characteristics” for SD_CS[3:0] timing.

2 The FlexBus supports programming an extension of the address hold. Please consult the *MCF5301x Reference Manual* for more information.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

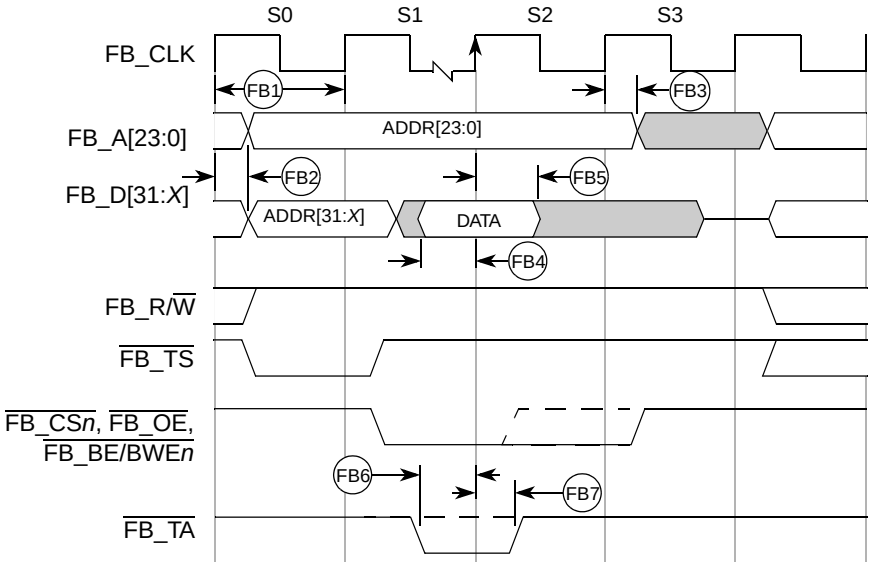


Figure 11. FlexBus Read Timing

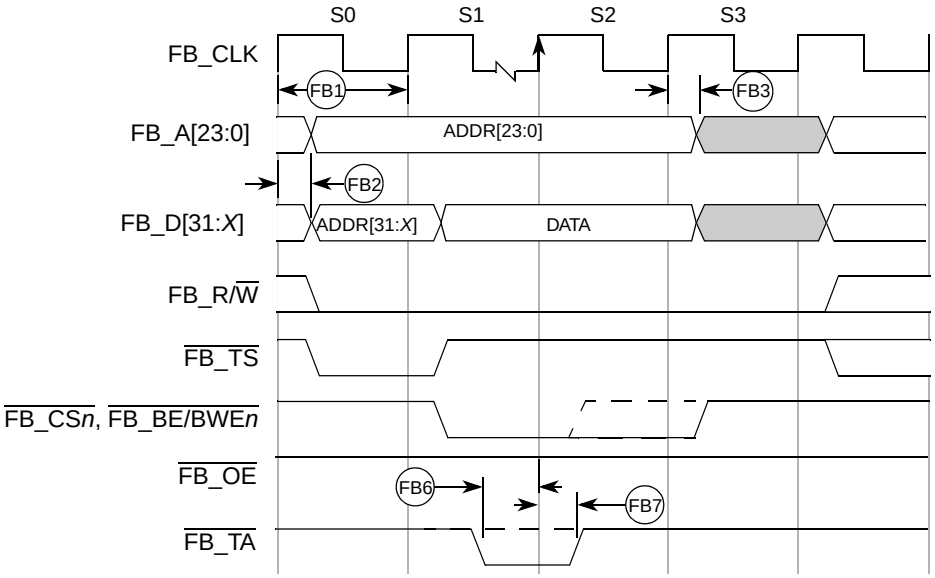


Figure 12. Flexbus Write Timing

5.7 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports either standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time.

5.7.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SD_DQS on read cycles. The device's SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must still be supplied to the device for each data beat of an SDR read. The processor accomplishes this by asserting a signal named SD_SDR_DQS during

read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SD_SDR_DQS signal and its usage.

Table 13. SDR Timing Specifications

Symbol	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of operation		50	80	Mhz	1
SD1	Clock period	t_{SDCK}	12.5	20	ns	2
SD2	Pulse width high	t_{SDCKH}	0.45	0.55	SD_CLK	3
SD3	Pulse width low	t_{SDCKH}	0.45	0.55	SD_CLK	4
SD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] output valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	
SD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] output hold	$t_{SDCHACI}$	2.0	—	ns	
SD6	SD_SDR_DQS output valid	t_{DQSOV}	—	Self timed	ns	5
SD7	SD_DQS[3:0] input setup relative to SD_CLK	$t_{DQVSDCH}$	0.25 × SD_CLK	0.40 × SD_CLK	ns	6
SD8	SD_DQS[3:2] input hold relative to SD_CLK	$t_{DQISDCH}$	Does not apply. 0.5×SD_CLK fixed width.			7
SD9	Data (D[31:0]) input setup relative to SD_CLK (reference only)	t_{DVSDCH}	0.25 × SD_CLK	—	ns	8
SD10	Data input hold relative to SD_CLK (reference only)	t_{DISDCH}	1.0	—	ns	
SD11	Data (D[31:0]) and data mask (SD_DQM[3:0]) output valid	$t_{SDCHDMV}$	—	0.75 × SD_CLK + 0.5	ns	
SD12	Data (D[31:0]) and data mask (SD_DQM[3:0]) output hold	$t_{SDCHDMI}$	1.5	—	ns	

1 The device supports same frequency of operation for both FlexBus and SDRAM clock operates as that of the internal bus clock. Please see the PLL chapter of the *MCF5301x Reference Manual* for more information on setting the SDRAM clock rate.
2 SD_CLK is one SDRAM clock in (ns).
3 Pulse width high plus pulse width low cannot exceed min and max clock period.
4 Pulse width high plus pulse width low cannot exceed min and max clock period.
5 SD_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SD_DQS will only pulse during a read cycle and one pulse will occur for each data beat.
6 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS will only pulse during a read cycle and one pulse will occur for each data beat.
7 The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.
8 Since a read cycle in SDR mode still uses the DQS circuit within the device, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens will result in successful SDR reads. The input setup spec is just provided as guidance.

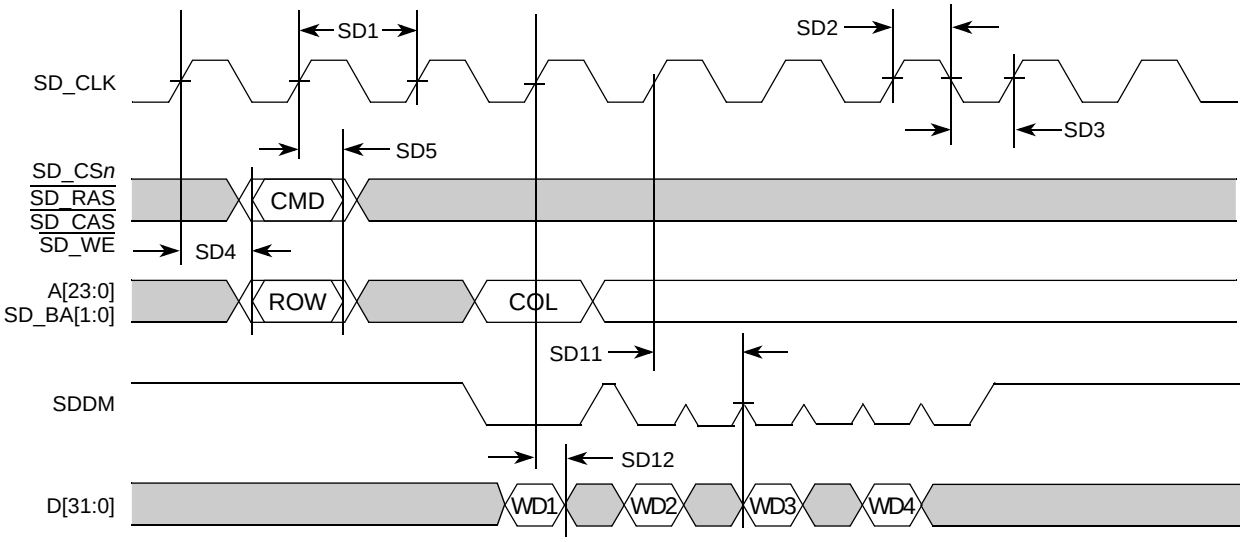


Figure 13. SDR Write Timing

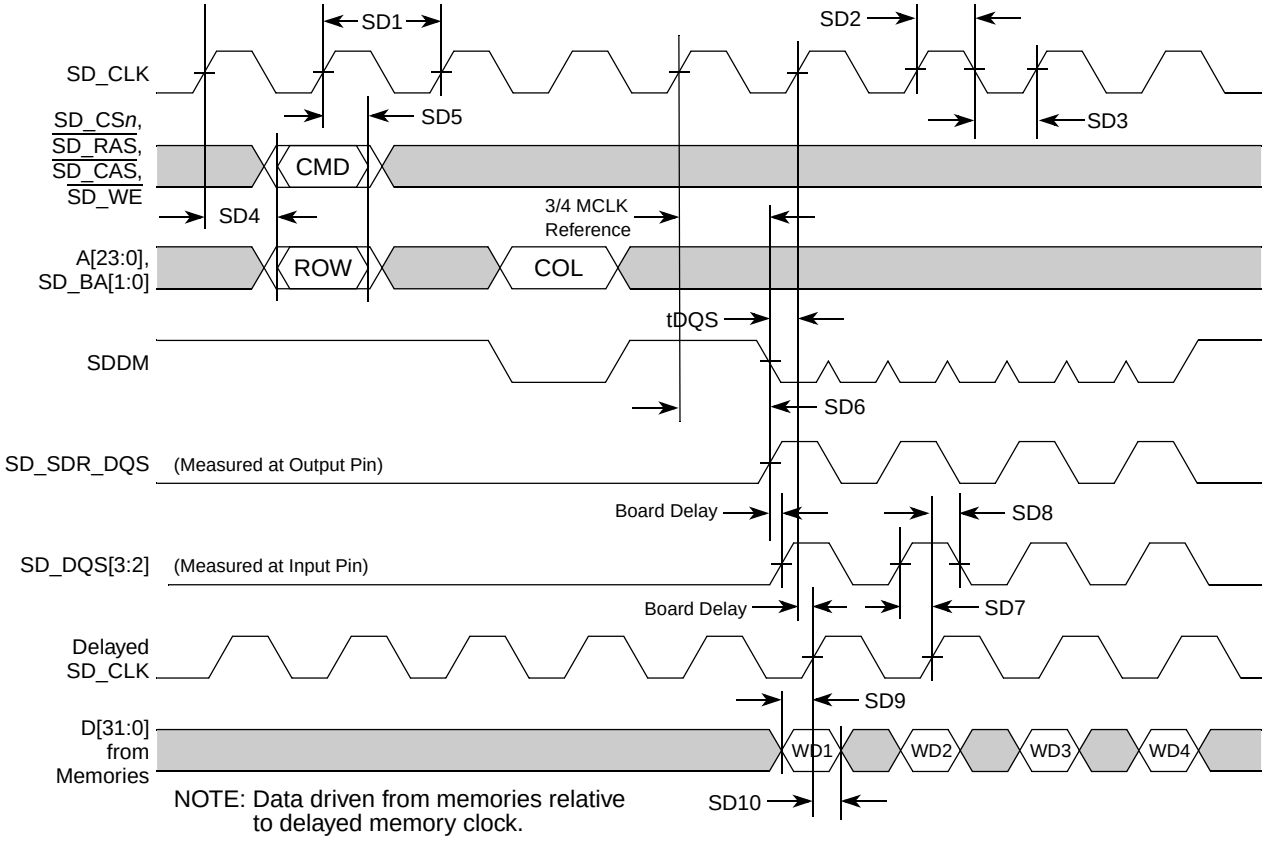


Figure 14. SDR Read Timing

5.7.2 DDR SDRAM AC Timing Characteristics

When the SDRAM controller is configured for DDR SDRAM, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes. The following timing numbers are subject to change at anytime, and are only provided to aid in early board design.

Table 14. DDR Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation	t_{DDCK}	50	80	Mhz	1
DD1	Clock Period	t_{DDSK}	12.5	20	ns	2
DD2	Pulse Width High	t_{DDCKH}	0.45	0.55	SD_CLK	3
DD3	Pulse Width Low	t_{DDCKL}	0.45	0.55	SD_CLK	3
DD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	4
DD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] Output Hold	$t_{SDCHACI}$	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition	t_{CMDVDQ}	—	1.25	SD_CLK	
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode)	t_{DQDMV}	1.5	—	ns	5 6
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)	t_{DQDMI}	1.0	—	ns	7
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{DVDQ}	—	1	ns	8
DD10	Input Data Hold Relative to DQS.	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns	9
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns	
DD12	DQS input read preamble width	t_{DQRPRE}	0.9	1.1	SD_CLK	
DD13	DQS input read postamble width	t_{DQRPST}	0.4	0.6	SD_CLK	
DD14	DQS output write preamble width	t_{DQWPRE}	0.25	—	SD_CLK	
DD15	DQS output write postamble width	t_{DQWPST}	0.4	0.6	SD_CLK	

1 The frequency of operation is either 2x or 4x the FB_CLK frequency of operation. FlexBus and SDRAM clock operate at the same frequency as the internal bus clock.

2 SD_CLK is one SDRAM clock in (ns).

3 Pulse width high plus pulse width low cannot exceed min and max clock period.

4 Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.

5 This specification relates to the required input setup time of today's DDR memories. The device's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory will be in violation. SD_D[31:24] is relative to SD_DQS3, SD_D[23:16] is relative to SD_DQS2, SD_D[15:8] is relative to SD_DQS1, and SD_D[7:0] is relative SD_DQS0.

6 The first data beat will be valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats will be valid for each subsequent DQS edge.

7 This specification relates to the required hold time of today's DDR memories. SD_D[31:24] is relative to SD_DQS3, SD_D[23:16] is relative to SD_DQS2, SD_D[15:8] is relative to SD_DQS1, and SD_D[7:0] is relative SD_DQS0.

8 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

9 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

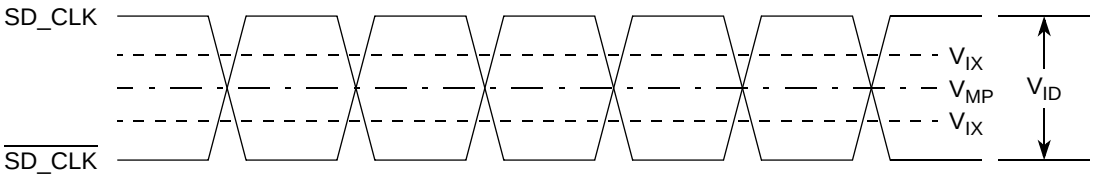


Figure 15. SD_CLK and SD_CLK Crossover Timing

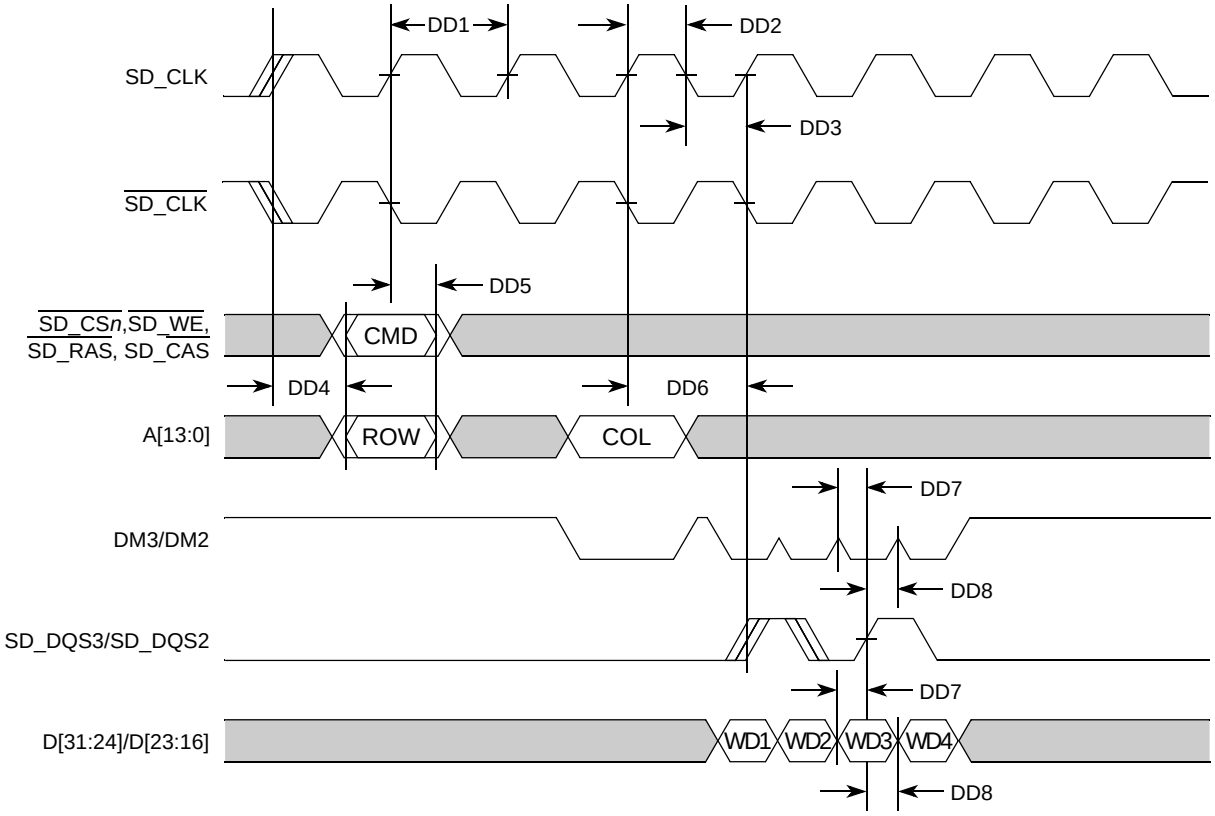


Figure 16. DDR Write Timing

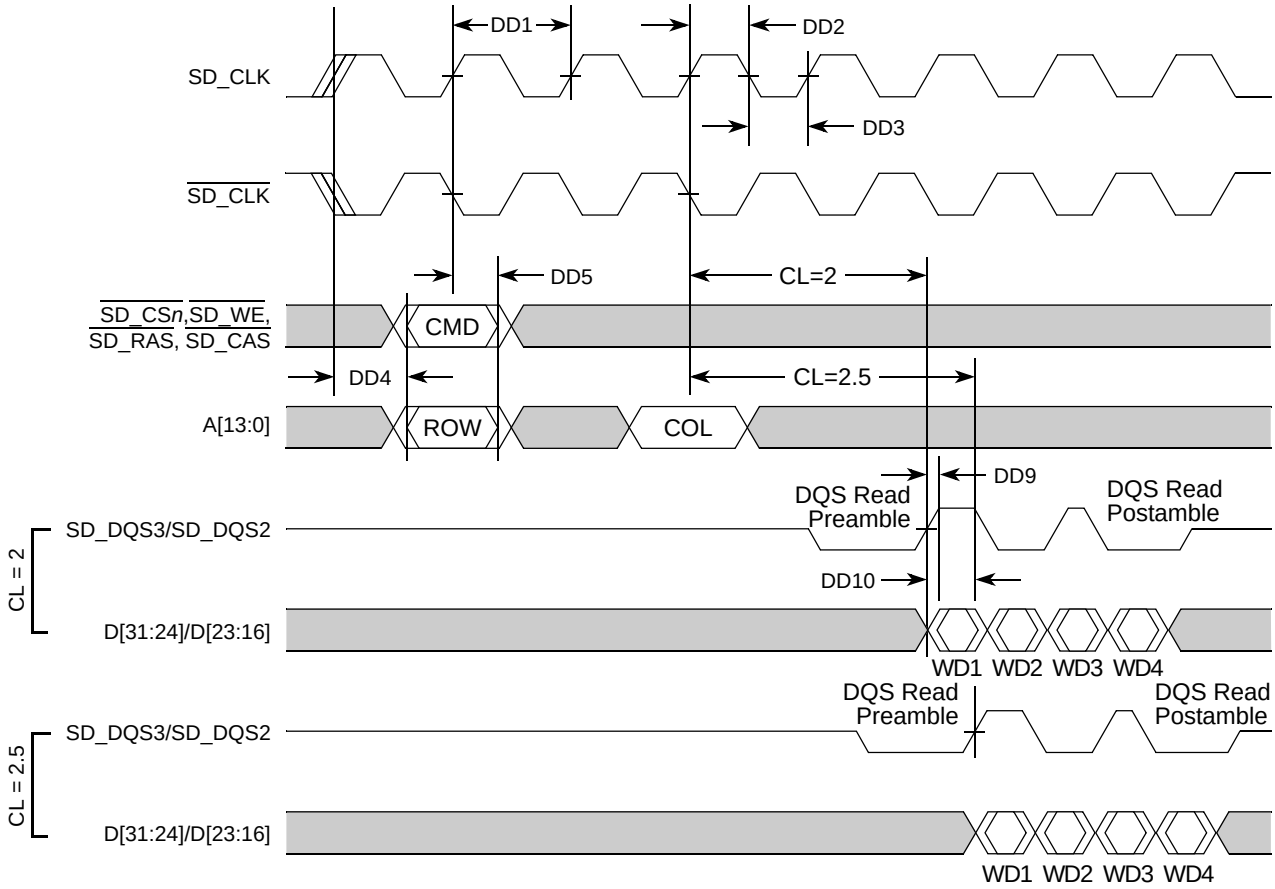


Figure 17. DDR Read Timing

5.8 General Purpose I/O Timing

Table 15. GPIO Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	FB_CLK High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	t_{PVCH}	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

1 GPIO pins include: $\overline{IRQn}$, PWM, UART, and Timer pins.

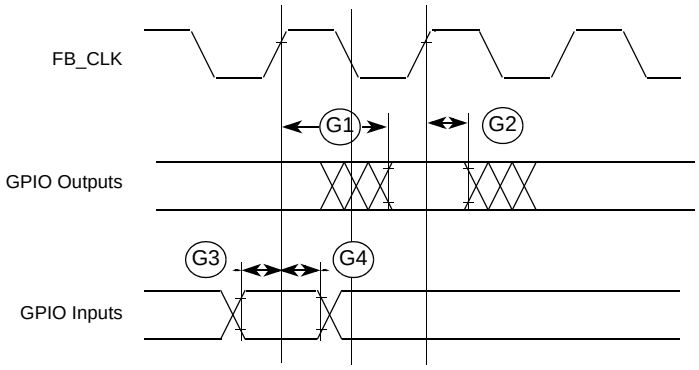


Figure 18. GPIO Timing

5.9 Reset and Configuration Override Timing

Table 16. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

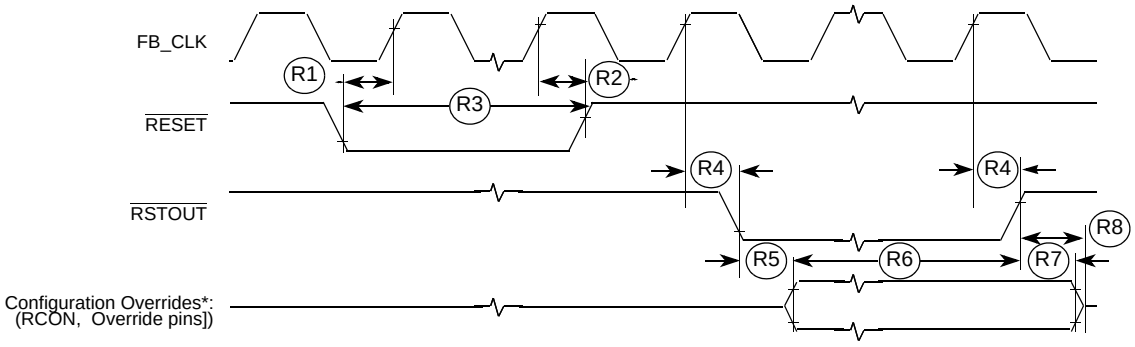


Figure 19. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF5301x Reference Manual* for more information.

5.10 USB On-The-Go

The MCF53017 device is compliant with industry standard USB 2.0 specification.

5.11 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 17. SSI Timing - Master Modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S1	SSI_MCLK cycle time	t_{MCLK}	$8 \times t_{SYS}$	—	ns	2
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}	
S3	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns	3
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}	
S5	SSI_BCLK to SSI_FS output valid		—	15	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	15	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedence		–2	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		10	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

1 All timings specified with a capactive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (SYSCLK).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of SYSCLK. If the SYSCLK is used, the minimum divider is 6. If the SSI_CLKIN input is used, the programmable dividers must be set to ensure that SSI_BCLK does not exceed 4 x f_{SYS}.

Table 18. SSI Timing — Slave Modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S11	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	t_{BCLK}	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	15	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedence		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		10	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

1 All timings specified with a capactive load of 25pF.

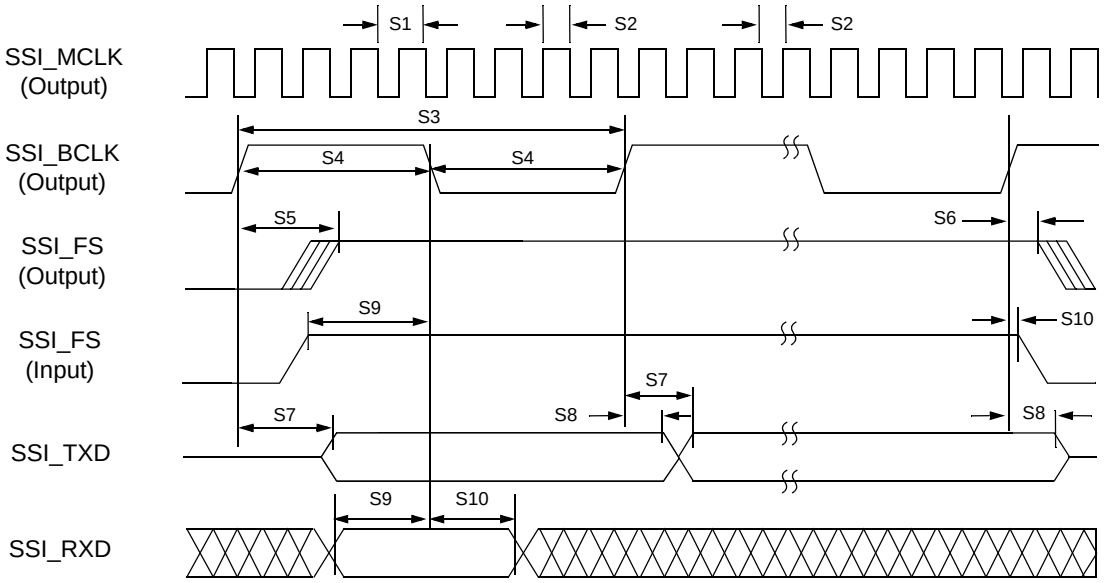


Figure 20. SSI Timing — Master Modes

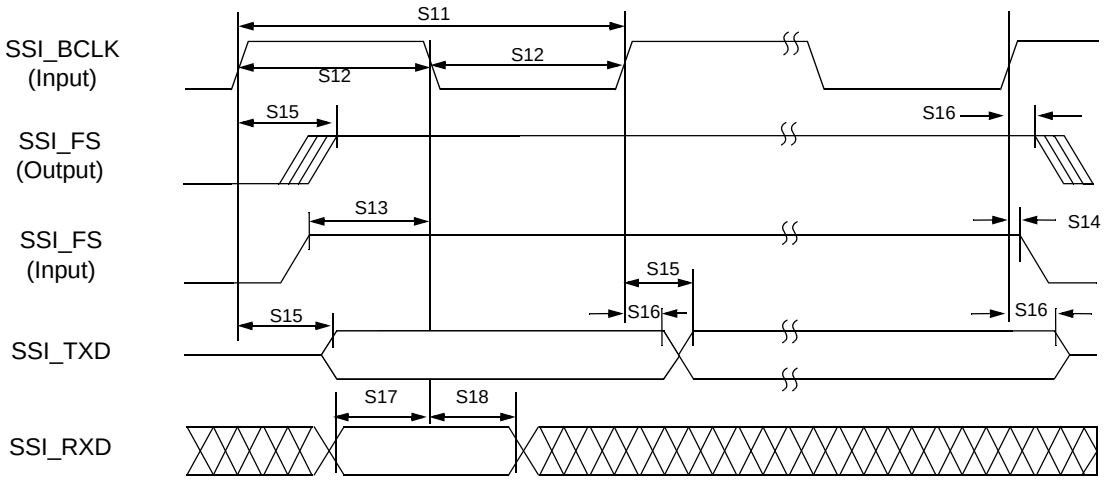


Figure 21. SSI Timing — Slave Modes

5.12 I²C Input/Output Timing Specifications

Table 19 lists specifications for the I²C input timing parameters shown in Figure 22.

Table 19. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

Table 19. I²C Input Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Units
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 20 lists specifications for the I²C output timing parameters shown in Figure 22.

Table 20. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 20. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 20 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 22 shows timing for the values in Table 20 and Table 19.

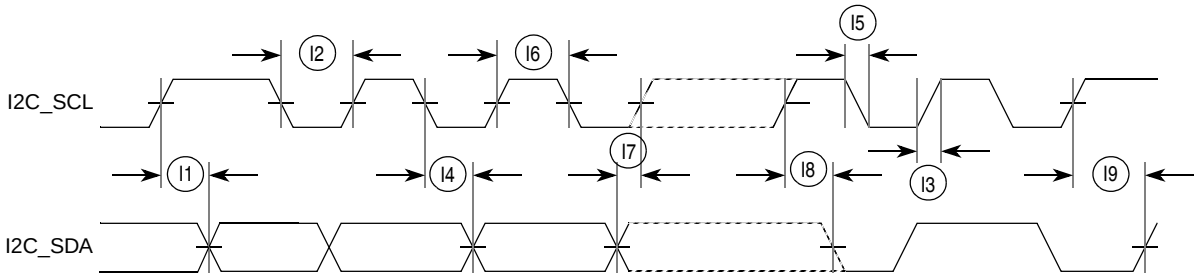


Figure 22. I²C Input/Output Timings

5.13 Fast Ethernet AC Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

5.13.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for both MII and 7-Wire style interfaces for a range of transceiver devices.

Table 21. Receive Signal Timing

Num	Characteristic	MII Mode		RMII Mode		Unit
		Min	Max	Min	Max	
E1	RXD[n:0], RXDV, RXER to RXCLK setup[1]	5	—	4	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold[1]	5	—	2	—	ns
E3	RXCLK pulse width high	35%	65%	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	35%	65%	RXCLK period

1 In MII mode, n = 3; In RMII mode, n = 1

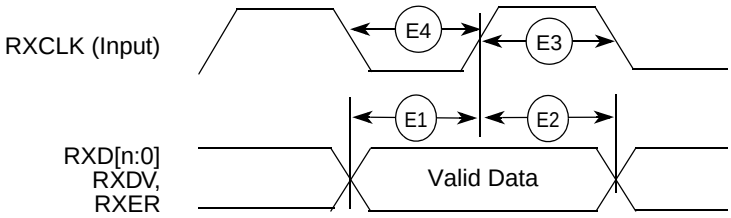


Figure 23. MII Receive Signal Timing Diagram

5.13.2 Transmit Signal Timing Specifications

Table 22. Transmit Signal Timing

Num	Characteristic	MII Mode		RMII Mode		Unit
		Min	Max	Min	Max	
E5	TXCLK to TXD[n:0], TXEN, TXER invalid[1]	5	—	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid[1]	—	25	—	10	ns
E7	TXCLK pulse width high	35%	65%	35%	65%	t_{TXCLK}
E8	TXCLK pulse width low	35%	65%	35%	65%	t_{TXCLK}

1 In MII mode, n = 3; In RMII mode, n = 1

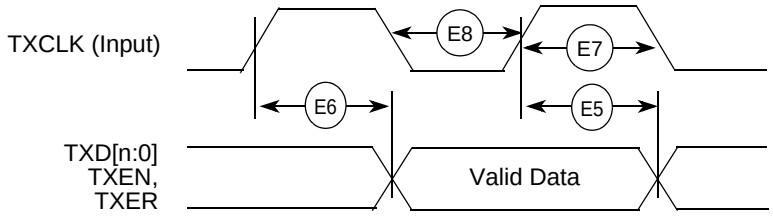


Figure 24. MII Transmit Signal Timing Diagram

5.13.3 Asynchronous Input Signal Timing Specifications

Table 23. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

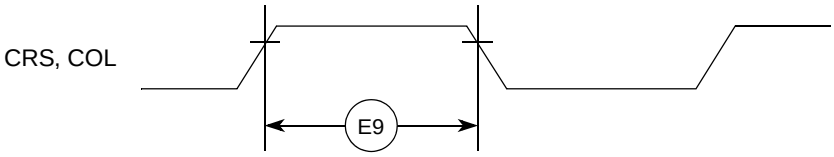


Figure 25. MII Async Inputs Timing Diagram

5.13.4 MII Serial Management Timing Specifications

Table 24. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

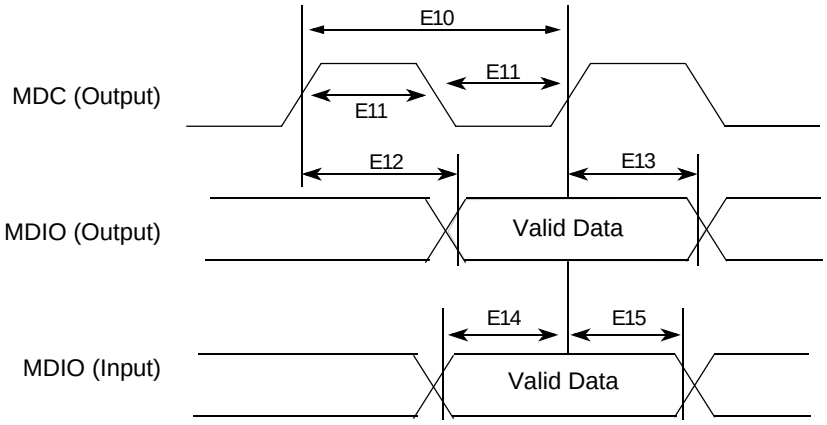


Figure 26. MII Serial Management Channel TIming Diagram

5.14 32-Bit Timer Module Timing Specifications

Table 25 lists timer module AC timings.

Table 25. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.15 DSPI Timing Specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with both master and slave operations. Many of the transfer attributes are programmable. Table 26 provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF5301x Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 26. DSPI Module AC Timing Specifications[1]

Name	Characteristic	Symbol	Min	Max	Unit	Notes
DS1	DSPI_SCK Cycle Time	t_{SCK}	4 x t_{SYS}	—	ns	2
DS2	DSPI_SCK Duty Cycle	—	(tsck ÷ 2) – 2.0	(tsck ÷ 2) + 2.0	ns	3
Master Mode						
DS3	DSPI_PCS*n* to DSPI_SCK delay	t_{CSC}	(2 × t_{SYS}) – 1.5	—	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* delay	t_{ASC}	(2 × t_{SYS}) – 3.0	—	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	—	—	5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	—	–5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	—	9	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	—	0	—	ns	
Slave Mode						
DS9	DSPI_SCK to DSPI_SOUT valid	—	—	4	ns	

Table 26. DSPI Module AC Timing Specifications[1] (continued)

Name	Characteristic	Symbol	Min	Max	Unit	Notes
DS10	DSPI_SCK to DSPI_SOUT invalid	—	0	—	ns	
DS11	DSPI_SIN to DSPI_SCK input setup	—	2	—	ns	
DS12	DSPI_SCK to DSPI_SIN input hold	—	7	—	ns	
DS13	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	—	20	ns	
DS14	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	—	18	ns	

1 Timings shown are for DMCR[MTFE] = 0 (classic SPI) and DCTAR*n*[CPHA] = 0. Data is sampled on the DSPI_SIN pin on the odd-numbered DSPI_SCK edges and driven on the DSPI_SOUT pin on even-numbered DSPI edges.

2 When in master mode, the baud rate is programmable in DCTAR*n*[DBR], DCTAR*n*[PBR], and DCTAR*n*[BR].

3 This specification assumes a 50/50 duty cycle setting. The duty cycle is programmable in DCTAR*n*[DBR], DCTAR*n*[CPHA], and DCTAR*n*[PBR].

4 The DSPI_PCS*n* to DSPI_SCK delay is programmable in DCTAR*n*[PCSSCK] and DCTAR*n*[CSSCK].

5 The DSPI_SCK to DSPI_PCS*n* delay is programmable in DCTAR*n*[PASC] and DCTAR*n*[ASC].

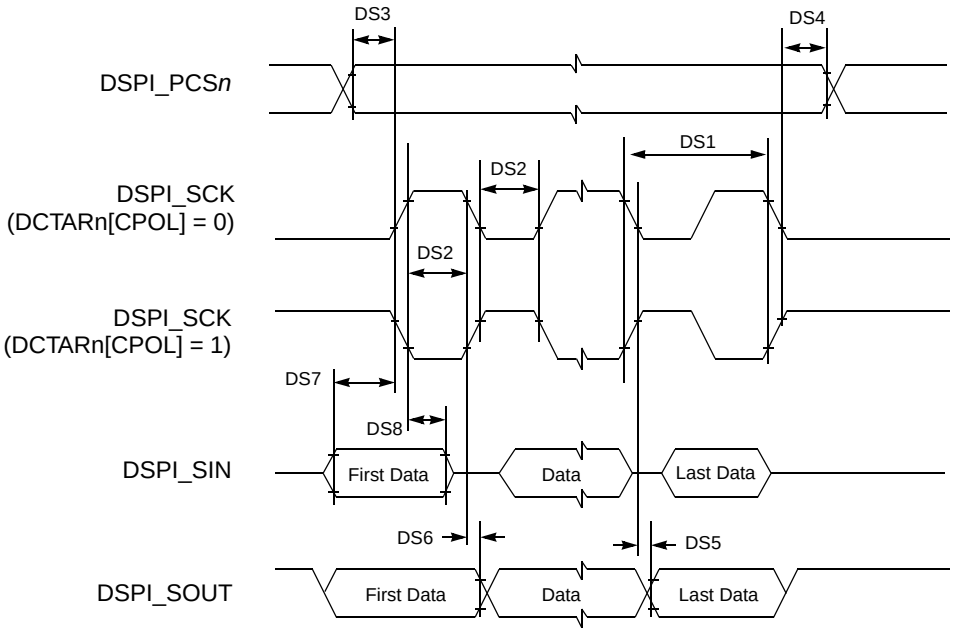


Figure 27. DSPI Classic SPI Timing — Master Mode

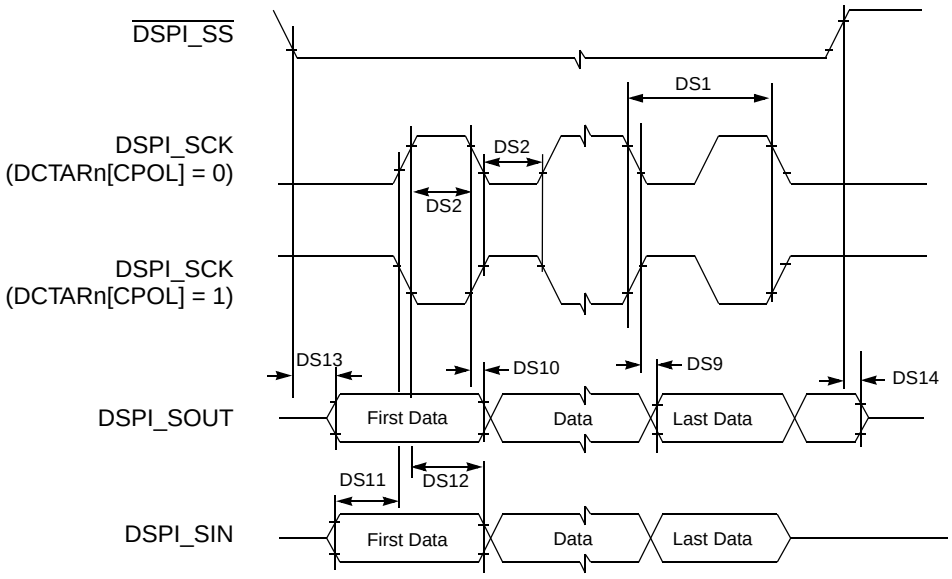


Figure 28. DSPI Classic SPI Timing — Slave Mode

5.16 eSDHC Electrical Specifications

This section describes the electrical information of the eSDHC.

5.16.1 eSDHC Timing

Figure 29 depicts the timing of eSDHC, and Table 29 lists the eSDHC timing characteristics.

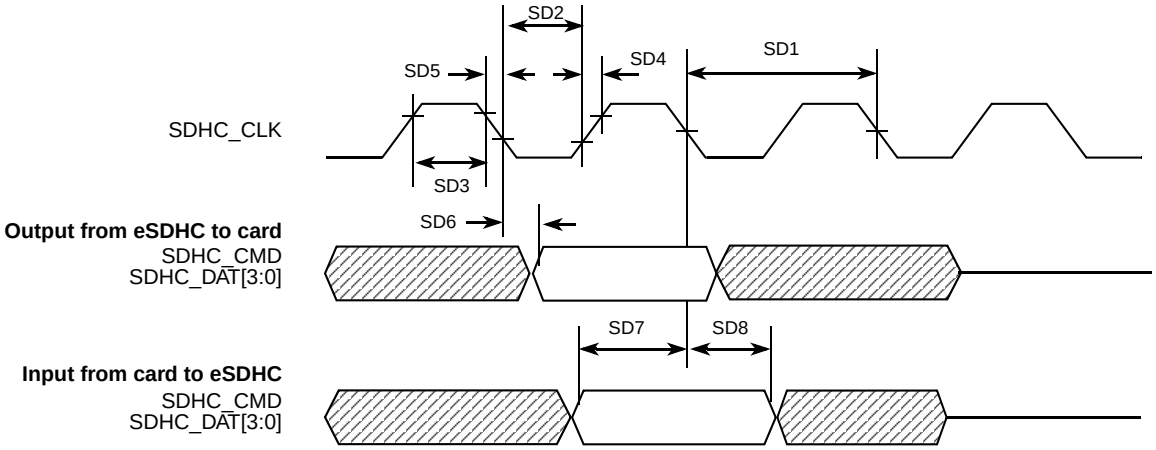


Figure 29. eSDHC Timing

Table 27. eSDHC Interfacde Timing Specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed)	f_{PP}[2]	0	25	MHz
	Clock Frequency (MMC Full Speed)	f_{PP}[3]	0	20	MHz
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output / Card Inputs SDHC_CMD, SDHC_DAT (Reference to SDHC_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–5	5	ns
eSDHC Input / Card Outputs SDHC_CMD, SDHC_DAT (Reference to SDHC_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	4	—	ns
SD8	eSDHC Input Hold Time	t_{IH}	0	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value from 0 to 25 MHz.
3 In normal data transfer mode for MMC card, clock frequency can be any value from 0 to 20 MHz.
4 In card identification mode, card clock must be 100 kHz – 400 kHz, voltage ranges from 2.7 to 3.6 V.

5.16.2 eSDHC Electrical DC Characterisics

Table 28 lists the eSDHC electrical DC characteristics.

Table 28. MMC/SD Interface Electrical Specifications

Num	Parameter	Design Value	Min	Max	Unit	Condition/Remark
General						
1	Peak Voltage on All Lines	—	–0.3	V_{DD} + 0.3	V	
All Inputs						
2	Input Leakage Current	—	–10	10	uA	
All Outputs						
3	Output Leakage Current	—	–10	10	uA	
Power Supply						
4	Supply Voltage (HV card)	3.1	2.7	3.6	V	for high voltage cards, must provide this voltage for card initialization
5	Supply Voltage (LV card)	1.8	1.65	1.95	V	for low voltage cards

Table 28. MMC/SD Interface Electrical Specifications (continued)

Num	Parameter	Design Value	Min	Max	Unit	Condition/Remark
5	Power Up Time	—	—	250	ms	
6	Supply Current	—	100	200	mA	
Bus Signal Line Load						
7	Pull-up Resistance	47	10	100	kohm	Internal PU
8	Open Drain Resistance	NA	NA	NA	kohm	For MMC cards only
Open Drain Signal Level						For MMC cards only
9	Output High Voltage	—	V_{DD} – 0.2	—	V	I_{OH} = –100 µA
10	Output Low Voltage	—	—	0.3	V	I_{OL}= 2 mA
Bus Signal Levels						
11	Output HIGH Voltage	—	0.75 x V_{DD}	—	V	I_{OH} = –100 µA @V_{DD} min
12	Output LOW Voltage	—	—	0.125 x V_{DD}	V	I_{OL} = 100 µA @V_{DD} min
13	Input HIGH Voltage	—	0.625 x V_{DD}	V_{DD} + 3	V	
14	Input LOW Voltage	—	V_{SS} – 0.3	0.25 x V_{DD}	V	

5.17 SIM Electrical Specifications

Each SIM card interface consist of a total of 12 pins (two separate ports of six pins each. Mostly one port with 5 pins is used).

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data, like a standard UART. All six (or five when a bidirectional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other. There are no required timing relationships between the signals in normal mode. However, there are some in reset and power down sequences.

5.17.1 General Timing Requirements

Figure 30 shows the timing of the SIM module, and Table 29 lists the timing parameters.

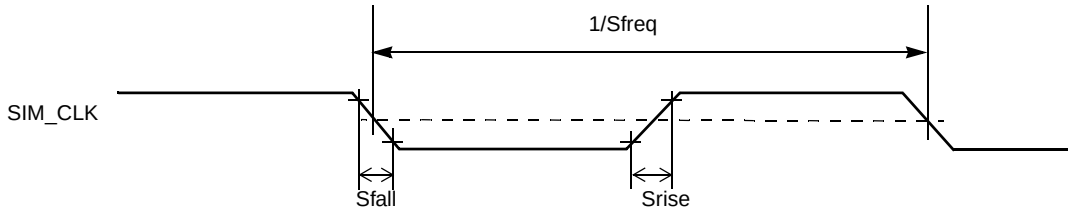


Figure 30. SIM Clock Timing Diagram

Table 29. SIM Timing Specification—High Drive Strength

Num	Description	Symbol	Min	Max	Unit
1	SIM Clock Frequency (SIM_CLK)[1]	S_{freq}	0.01	5 (Some new cards may reach 10)	MHz
2	SIM_CLK Rise Time [2]	S_{rise}	–	20	ns
3	SIM_CLK Fall Time [3]	S_{fall}	–	20	ns
4	SIM Input Transition Time (RX, SIM_PD)	S_{trans}	–	25	ns

1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

5.17.2 Reset Sequence

5.17.2.1 Cards with Internal Reset

The reset sequence for this kind of SIM card is as follows (see Figure 31):

- After powerup, the clock signal is enabled on SIM_CLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40,000 clock cycles after T0.

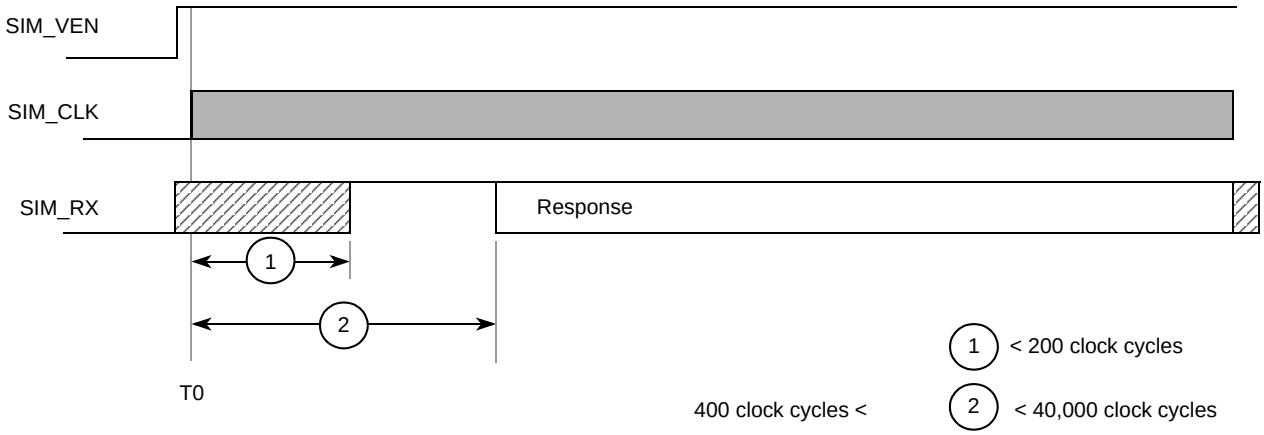


Figure 31. Internal-Reset Card Reset Sequence

5.17.2.2 Cards with Active-Low Reset

The sequence of reset for this kind of card is as follows (see Figure 32):

1. After powerup, the clock signal is enabled on SIM_CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. SIM_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
4. SIM_RST is set high (time T1)
5. SIM_RST must remain high for at least 40,000 clock cycles after T1 and a response must be received on RX between 400 and 40,000 clock cycles after T1.

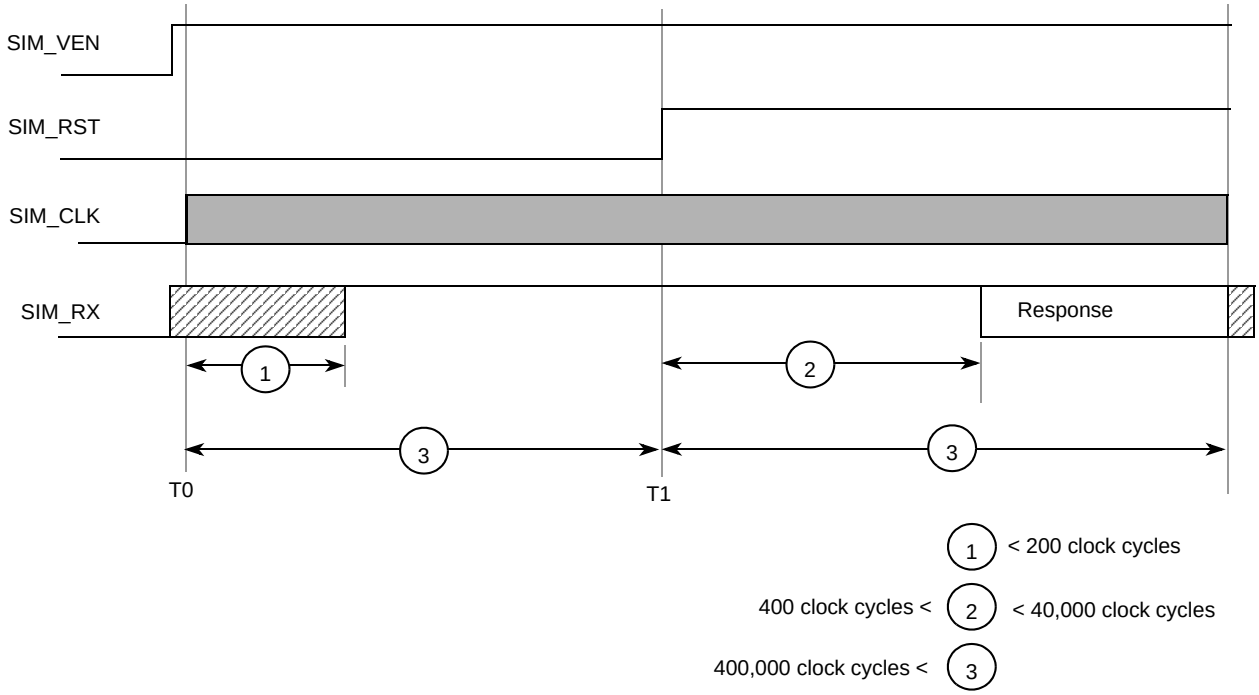


Figure 32. Active-Low-Reset Card Reset Sequence

5.17.3 Power Down Sequence

Power down sequence for SIM interface is as follows:

1. SIM_PD port detects the removal of the SIM card
2. SIM_RST goes low
3. SIM_CLK goes low
4. SIM_TX goes low
5. SIM_VEN goes low

Each of these steps is completed in one CKIL period (usually 32 kHz). Power-down may be started in response to a card-removal detection or launched by the processor. Figure 33 and Table 30 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

Table 30. Timing Requirements for Power Down Sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9 ÷ f_{CKIL}	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8 ÷ f_{CKIL}	1.2	µs
3	SIM reset to SIM Voltage Enable Low	$S_{rst2ven}$	2.7 ÷ f_{CKIL}	1.8	µs
4	SIM Presence Detect to SIM reset Low	S_{pd2rst}	0.9 ÷ f_{CKIL}	25	ns

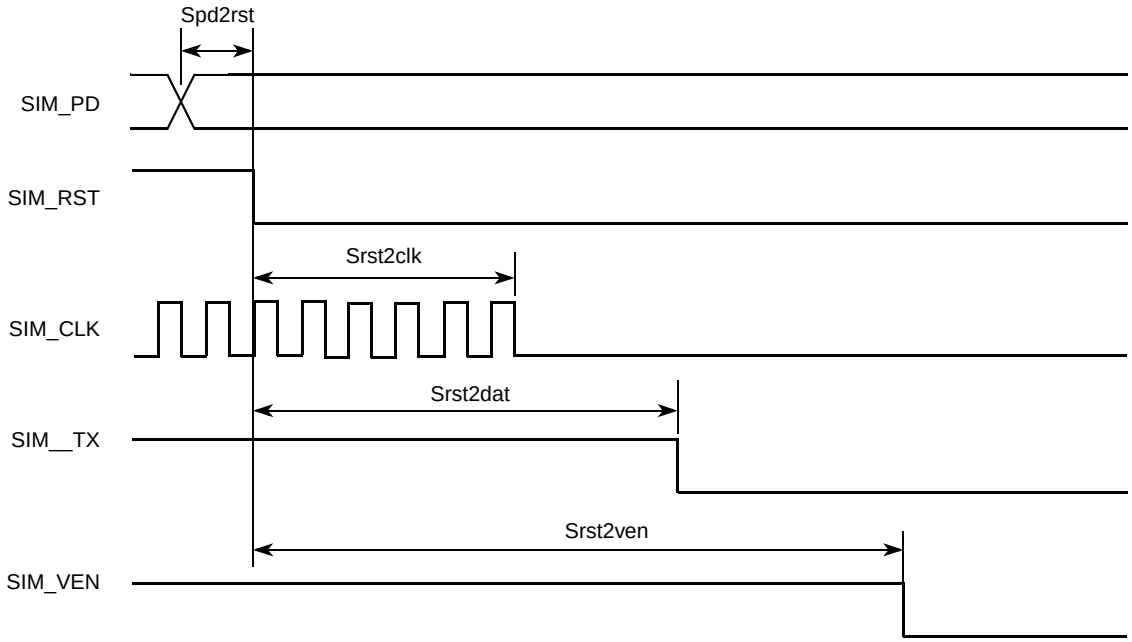


Figure 33. SmartCard Interface Power-Down AC Timing

5.18 IIM/Fusebox Electrical Specifications

Table 31. IIM/Fusebox Timing Characteristics

Num	Description	Symbol	Min	Max	Unit
1	Program time for eFuse[1]	$t_{program}$	125	—	µs

[1] The program length is defined by the value defined in IIM_FCR[PRG_LENGTH] of the IIM module. The value to program is based on a 32 kHz clock source (4 ÷ 32 kHz = 125 µs)

5.19 Voice Codec

The voice codec function is analog-to-digital and digital-to-analog conversion of the voice signal. The following section contains detailed electrical specifications for the analog and digital parts' performance. The voice codec is powered down when not enabled for power consumption.

Table 32 shows the voice codec general specifications.

Table 32. Voice Codec General Specifications

Parameter	Condition	Min	Typ	Max	Units
CODEC Input clock CODEC_CLK	VCLK[2:0]=0 VCLK[2:0]=1,2 VCLK[2:0]=3 VCLK[2:0]=4 VCLK[2:0]=5 VCLK[2:0]=6 VCLK[2:0]=7	— — — — — — —	16.8 19.44 20.0 24.0 26.0 28.0 30.0	— — — — — — —	MHz MHz MHz MHz MHz MHz MHz
VAG input Voltage	No Load, AVDD (CODEC_REGBYP) = 2.5V	1.225	1.325	1.425	V
Ref_Codec_p		TBD	1.665	TBD	V
Ref_Codec_n		TBD	0.985	TBD	V
VAG External Cap		—	0.1	—	µF
avoco_ref_codec_p External Cap		—	0.1	—	µF
avoco_ref_codec_n External Cap		—	0.1	—	µF
avoco_vagout_codec External Cap		—	0.1	—	µF
Codec Analog Supply Current (includes Rx and Tx paths)	AVDD (CODEC_REGBYP) = 2.5V, operational	—	5	6	mA
	Power-down mode	—	—	5	µA
Codec Digital Supply Current[1]	Operational mode	—	—	1	mA
Response to input ON/OFF (settling time at turn on)		—	—	1	ms

1 More accurate estimation will be given after some progress in design.

5.19.1 Voice Codec ADC Specifications

Voice coding function includes a 50 kHz second-order, low-pass anti-aliasing filter, an analog-to-digital converter, digital filters for decimation, band-passing, frequency ripple compensation, and DSP interface logic. The audio input A/D converter converts the incoming signal to 13-bit two's-compliment linear PCM words at an 8 or 8.1 kHz rate. Following the A/D converter, the signal is digitally filtered, low-pass, and selectable high-pass. Table 33 shows the voice coding specifications.

Table 33. Voice Codec ADC Specifications[1]

Parameter	Condition	Min	Typ	Max	Units
Power Supply Rejection Ratio with respect to AVDD (CODEC_REGBYP)[2]	20Hz to 100kHz, with 100 mV_{pp} noise applied to AVDD, with an external VAG cap	50	60	—	dB
Peak Input	(+3dBm0)[3] on an individual differential pin (ADC_P or ADC_M)	VAG–0.34	—	VAG+0.34	V
Tx AC Input Impedance	f=1.02kHz	100	—	—	kΩ
Absolute Gain	0dBm0@1.02kHz	–1.0	—	1.0	dB

Table 33. Voice Codec ADC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Gain vs. Signal	Relative to –10dBm0 @1.02kHz +3 to –40dBm0 –40 to –50dBm0 –50 to –55dBm0	 –0.25 –1.2 –1.3	 — — —	 0.25 1.2 1.3	 dB dB dB
Total Distortion (noise and harmonic) (300Hz – 20kHz Noise BW in 300Hz – 4kHz measured BW out)	1.02kHz tone (linear) +2dBm0[4] 0dBm0 –6dBm0 –10dBm0 –20dBm0 –30dBm0 –40dBm0 –45dBm0 –55dBm0	 57 60 60 55 45 35 25 20 15	 60 64 70 65 55 45 35 30 20	 — — — — — — — — —	 dB dB dB dB dB dB dB dB dB
Idle Channel Noise[5]	Psophometric Weighting at the output	—	—	–72	dBm0p
Digital Offset[6]		—	—	5	%Full Scale
Frequency Response VCIHPF = logic high	Relative to 0dBm0@1.02kHz 50Hz 60Hz[7] 200Hz 300 to 3000Hz 3400Hz[8] 4000Hz 4600Hz	 –8 –0.5 –1.0 — — — —	 — — — — — — —	 –25 –23 –0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB dB
Frequency Response VCIHPF=logic low	Relative to 0dBm0@1.02kHz 50Hz 200Hz 300 to 3000Hz 3400Hz[9] 4000Hz 4600Hz	 –0.5 –0.5 –0.5 –1.0 — —	 — — — — — —	 +0.5 +0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB
Inband Spurious	1.02kHz @ 0dBm0, 300 to 3kHz	—	—	–48	dB
Crosstalk D/A to A/D	D/A = 0 dBm0 @1.02kHz Measured while stimulated w/ 2667Hz @–50dBm0	—	—	–75	dB
Intermodulation Distortion	Two frequencies of amplitudes –4 to –21 dBm0 from the range 300 to 3400Hz	—	—	–41	dB

Table 33. Voice Codec ADC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Filter Group Delay VCIHPF=logic high CODEC_CLK=26MHz (Relative to 1.6kHz)	500Hz < f < 600Hz 600Hz < f < 800Hz 800Hz < f < 1kHz 1kHz < f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	— — — — — — —	— — — — — — —	260 155 57 15 95 135 190	µS µS µS µS µS µS µS
Filter Group Delay VCIHPF=logic low CODEC_CLK=26MHz (Relative to 1.6kHz)	f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	–40 0 — —	— — — —	0 100 150 200	µS µS µS µS
Filter Absolute Group Delay VCIHPF=logic high	f=1.6kHz	—	—	300	µS
Filter Absolute Group Delay VCIHPF=logic low	f=1.6kHz	—	—	235	µS
Out of Band input fold-in spurious	with 0dBm0 input signal from 4.6 kHz to 8.4 kHz	—	—	–50	dB

1 All analog signals are referenced to VAG unless otherwise noted.

2 Power Supply Rejection Ratio is for Longjing IC only. Total PSRR from battery to output is obtained by summing the PSRR from Neptune to the one from the Regulator in Seaweed. It is assumed that the regulators in Seaweed will have a minimum PSRR of 45 dB.

3 For A/D differential input (ADC_P - ADC_M) 0dBm0 = 340mV$_{rms}$.
The codec output will not “foldback” or oscillate if overdriven, but clip.

4 The digital word corresponding to +3dBm0 is ‘0111111111111’b. Therefore if the audio level is set to +3dBm0, any variation in gain could cause large distortion if the digital number exceeds ‘0111111111111’b. For this reason the maximum recommended signal for low distortion is +3dBm0 – (Absolute Gain Error) = +2dBm0.

5 GSM Spec = –64 0dB.

6 This value is a preliminary target. The final number will be specified after obtaining the production statistical data.

7 Small frequency response deviation from straight line in the 60:200 Hz range is acceptable by spec requirements.

8 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

9 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

Figure 34 and Figure 35 show the filter frequency response for the audio signal for voice coding path. (All filter frequencies increase by 8.1/8.0 if VCLK is selected to generate f_{SYNC}=8.1kHz).

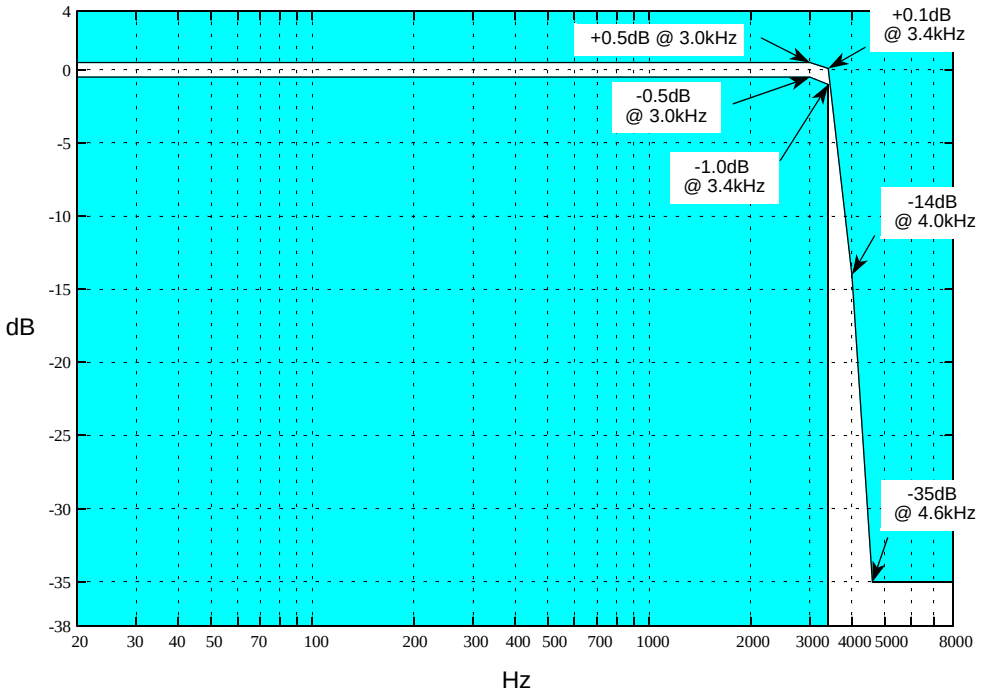


Figure 34. Voice Signal Frequency Response Requirements at the ADC Path (VCIHPF=0, LPF Alone Without HPF)

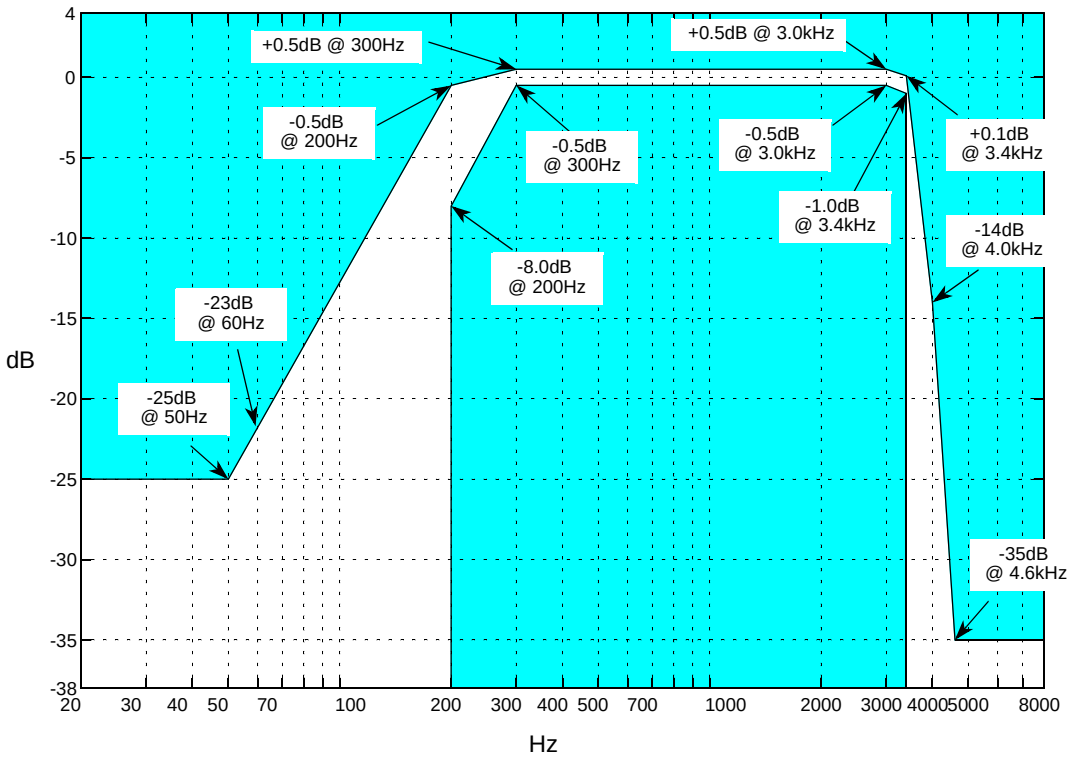


Figure 35. Voice Signal Frequency Response Requirements at the ADC Path (VCIHPF=1, HPF and LPF Together)

5.19.2 Voice Codec DAC Specifications

Voice-decoding function includes frequency ripple compensation, interpolation, digital-to-analog conversion, and anti-imaging filter. The input signal for the voice-decoding function is in linear 16-bit two's compliment PCM words at an 8 kHz or 8.1 kHz rate. Table 34 shows the voice decoding specifications.

Table 34. Voice Codec DAC Specifications[1]

Parameter	Condition	Min	Typ	Max	Units
Output Level	+3dbm0[2] (clipping level) on an individual differential output pin (CODEC_DACP or CODEC_DACN)	VAG–0.5	—	VAG+0.5	V
Output Source Impedance	10kΩ Load	—	100	—	Ω
Output Power Supply Rejection Ratio	20Hz to 100kHz with 100 mVrms, noise applied to AVDD (CODEC_REGBYP)	50	60	—	dBa
Absolute Gain	0dBm0@1.02kHz	–1.0	—	1.0	dB
Gain vs. Signal	–10dBm0@1.02kHz +3 to –40dBm0 –40 to –50dB –50 to –55dBm0	 –0.25 –1.2 –1.3	 — — —	 0.25 1.2 1.3	 dB dB dB

Table 34. Voice Codec DAC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Total Distortion (4 kHz noise BW in 300 Hz – 20 kHz measured BW out)	1.02 kHz tone (linear) +2 dBm0 0 dBm0 –6 dBm0 –10 dBm0 –20 dBm0 –30 dBm0 –40 dBm0 –45 dBm0 –55 dBm0	 57 60 60 55 45 35 25 20 15	 60 64 70 65 55 45 35 30 20	 — — — — — — — — —	 dB dB dB dB dB dB dB dB dB
Idle Channel Noise[3] (At CODEC out)	A weighted to 20kHz	—	–78	–73	dBm0
	8kHz, 30Hz BW, D/A = zero code	No spurious			
Differential offset	T_A = 70 °C T_A = 25 °C	— —	— —	40 30	mV
Frequency Response VCOHPF = logic high (Min. limit valid for CODEC_CLK=26MHz)	Relative to 0dBm0@1.02kHz 50Hz 60Hz[4] 200Hz 300–3000Hz 3400Hz[5] 4000Hz 4600Hz	 — — –8 –0.5 –0.8 — —	 — — — — — — —	 –25 –23 –0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB dB
Frequency Response VCOHPF = logic low (Min. limit valid for CODEC_CLK=26MHz)	Relative to 0dBm0@1.02kHz 50Hz 200Hz 300–3000Hz 3400Hz[6] 4000Hz 4600Hz	 –0.5 –0.5 –0.5 –0.8 — —	 — — — v — —	 +0.5 +0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB
Inband Spurious	1.02kHz @ 0dBm0, 300 to 3kHz	—	—	–48	dB
Out-of-Band Spurious (Interpolation Image Suppression)	300 to 3400Hz @ 0dBm0 input 4600 to 7600Hz 7600 to 8400Hz 8400 to 20,000Hz	—	—	 –50 –50 –50	 dB dB dB
Crosstalk A/D to D/A	A/D = 0dBm0 @1.02kHz	—	—	–75	dB
Intermodulation Distortion	Two frequencies. of amplitudes –4 to –21 dBm0 from the range 300 to 3400Hz	—	—	–41	dB

Table 34. Voice Codec DAC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Filter Group Delay VCOHPF = logic high CODEC_CLK=26 MHz (Relative to 1.6kHz)	500Hz < f < 600Hz 600Hz < f < 800Hz 800Hz < f < 1kHz 1kHz < f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	— — — — — — —	— — — — — — —	300 200 70 30 95 135 190	µs µs µs µs µs µs µs
Filter Group Delay VCOHPF = logic low CODEC_CLK=26 MHz (Relative to 1.6kHz)	f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	–40 0 — —	— — — —	0 100 160 200	µs µs µs µs
Filter Absolute Group Delay VCOHPF = logic high	f=1.6kHz	—	—	350	µs
Filter Absolute Group Delay VCOHPF = logic low	f=1.6kHz	—	—	320	µs

1 All analog signals are referenced to VAG unless otherwise noted. Output is 0dbm0 unless noted.

2 For D/A differential output (CODEC_DACP - CODEC_DACN) 0dBm0 = 500 mV_{rms}.

3 GSM Spec = –64.

4 Small frequency response deviation from straight line in the 60:200 Hz range is acceptable by spec requirements.

5 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

6 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

Figure 36 and Figure 37 show the filter frequency response for the audio signal for voice decoding. The requirements for the decoding path at 3.4 kHz are slightly different from the coding path. (All filter frequencies increase by 8.1/8.0 if VCLK is selected to generate f_{SYNC} = 8.1 kHz).

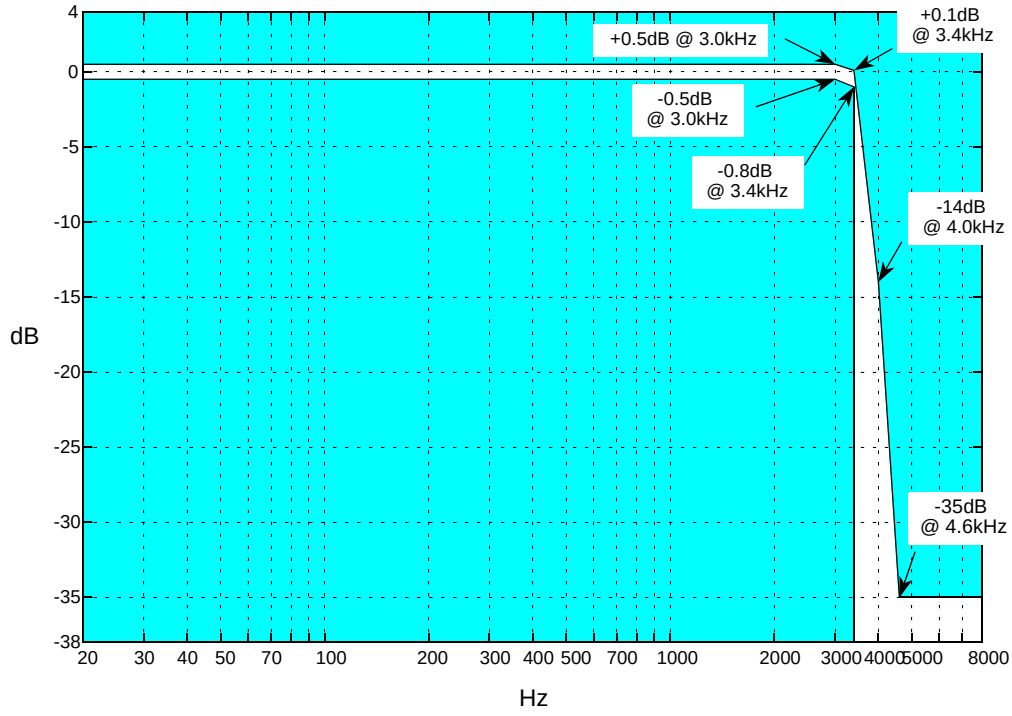


Figure 36. Voice Signal Frequency Response Requirements at the DAC Path (VCOHPF=0, LPF Alone Without HPF)

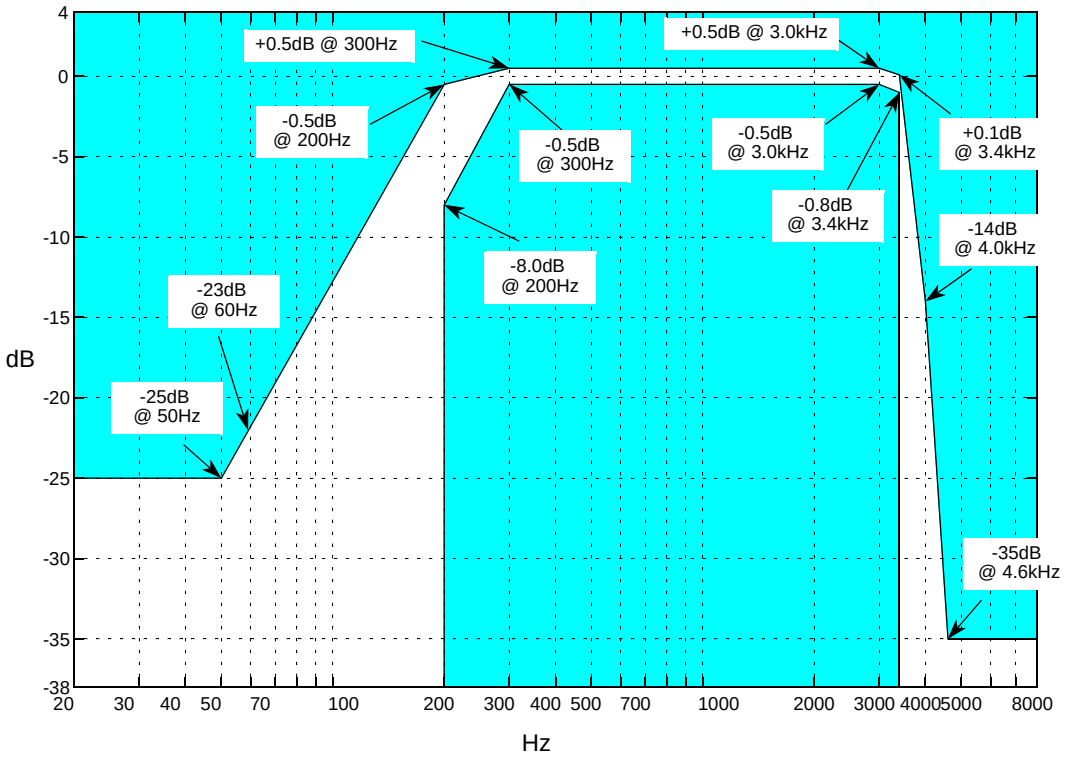


Figure 37. Voice Signal Frequency Response Requirements at the DAC Path (VCOHPF=1, HPF and LPF Together)

5.20 Integrated Amplifiers

5.20.1 Speaker Amplifier

The speaker amplifier boosts the power from the DAC and drives the speaker. It also provides analog volume control to optimize the noise performance of the entire channel. Table 35 shows the specifications for the speaker amplifier.

Table 35. Speaker Amplifier Specifications

Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current			—	800	—	μA
Shutdown Current			—	TBD	—	
Input Reference Offset			—	2	5	mV
Max Output Power	F_{in} = 1kHz, THD+N = 1%, R_L = 4Ω		—	600	—	mW
Total Harmonic Distortion (THD)	Gain = 0dB, R_L = 4Ω, F_{in} = 1kHz	Full Power, 500mW	—	0.050	—	%
		Half Power, 250mW	—	0.050	—	
	Gain = 0dB, R_L = 4Ω, F_{in} = 4kHz	Full Power, 500mW	—	0.1	—	
		Half Power, 250mW	—	0.1	—	
Integrated Output Noise	Gain = 0dB, BW = 20Hz – 20kHz		—	15	—	μV

Table 35. Speaker Amplifier Specifications (continued)

Parameter	Conditions		Min	Typ	Max	Units
Signal to Noise Ratio (SNR)	Gain = 0dB, V_{OUT} = 1.4V_{RMS}, BW = 20Hz – 20kHz		—	99	—	dB
Power Supply Rejection Ratio (PSRR)	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 217Hz	—	60	—	dB
		f = 1kHz	—	60	—	
		f = 4kHz	—	60	—	
Max. Cap Load Drive	No Sustained Oscillations		—	300	—	pF
Output SC Current			—	625	—	mA
Gain Error	Gain = –45,–21, –6, 0, 4, 6 dB		—	±0.5	—	dB

5.20.2 Handset Amplifier

The handset amplifier boosts the power from the DAC and drives the handset. It also provides analog volume control to optimize the noise performance of the entire channel. Table 36 shows the specifications for handset amplifier.

Table 36. Handset Amplifier Specifications

Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current			—	800	—	µA
Shutdown Current			—	TBD	—	
Input Reference Offset			—	2	5	mV
Max. Output Power	F_{in} = 1kHz, THD + N = 1%, R_L = 8Ω		—	300	—	mW
Total Harmonic Distortion (THD)	Gain = 0dB, R_L = 8Ω, F_{in} = 1kHz	Full Power, 250mW	—	0.050	—	%
		Half Power, 125mW	—	0.050	—	
	Gain = 0dB, R_L = 8Ω, F_{in} = 4kHz	Full Power, 250mW	—	0.1	—	
		Half Power, 125mW	—	0.050	—	
Integrated Output Noise	Gain = 0dB, BW = 20Hz – 20kHz		—	15	—	µV
Signal to Noise Ratio (SNR)	Gain = 0dB, V_{OUT} = 1.4V_{RMS} , BW = 20Hz – 20kHz		—	99	—	dB
Power Supply Rejection Ratio (PSRR)	Gain = 0dB, Vripple = 200mVpp	f = 217Hz	—	60	—	dB
		f = 1kHz	—	60	—	
		f = 4kHz	—	60	—	
Maximum Cap Load Drive	No Sustained Oscillations		—	300	—	pF
Output SC Current			—	325	—	mA
Gain Error	Gain = –45, –21, –6, 0, 4, 6 dB		—	±0.5	—	dB

5.20.3 Headphone Amplifier

The headphone amplifier boosts the power from the DAC and drives the headphone. It also provides analog volume control to optimize the noise performance of the entire channel. Table 37 shows the specifications for the microphone amplifier.

Table 37. Headphone Amplifier Specifications

Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current			—	600	—	µA
Shutdown Current			—	TBD	—	
Input Reference Offset			—	2	5	mV
Output Power	F_{in} = 1kHz, THD+N = 1%, R_L = 16Ω		—	40	—	mW
Total Harmonic Distortion (THD)	Gain = 0dB, R_L = 16Ω, BW = 200Hz – 4kHz	Full Power, 31.25mW	—	0.05	—	%
		Half Power, 16.5mW	—	0.05	—	
Integrated Output Noise	Gain = 0dB, BW = 20Hz – 20kHz		—	15	—	µV
Signal to Noise Ratio (SNR)	Gain = 0dB, V_{OUT} = 0.7V_{RMS} , BW = 20Hz – 20kHz		—	93	—	dB
Power Supply Rejection Ratio (PSRR)	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 217Hz	—	60	—	dB
		f = 1kHz	—	60	—	
		f = 4kHz	—	60	—	
Maximum Cap Load Drive	No Sustained Oscillations		—	300	—	pF
Output SC Current			—	150	—	mA
Gain Error	Gain = –45, –21, –12, –6, –2, 0 dB		—	±0.5	—	dB

5.20.4 Microphone Amplifier

The microphone amplifier boosts the signal from the microphone and provides it to the ADC. The gain control present in the microphone amplifier helps in optimizing the noise performance of the entire channel. Table 38 shows the specifications for the microphone amplifier.

Table 38. Microphone Amplifier Specifications

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current		—	500	—	µA
Shutdown Current		—	TBD	—	
Input Reference Offset		—	2	5	mV

Table 38. Microphone Amplifier Specifications (continued)

Parameter	Conditions		Min	Typ	Max	Units
Total Harmonic Distortion (THD)	Gain = 0dB, Fin = 1k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	%
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 20dB, Fin = 1k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 0dB, Fin = 4k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 20dB, Fin = 4k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
Integrated Output Noise	BW = 20Hz – 20kHz	Gain = 0dB	—	12	—	µV
		Gain = 20dB	—	40	—	
Signal to Noise Ratio (SNR)	V_{OUT} = 0.5V_{RMS}, BW = 20Hz – 20kHz	Gain = 0dB	—	92.4	—	dB
		Gain = 20dB	—	81.9	—	
THD plus Noise	V_{OUT} = 0.35V_{RMS}, BW = 20Hz – 20kHz	Gain = 0dB	—	80	—	dB
		Gain = 20dB	—	80	—	
Power Supply Rejection Ratio	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 1kHz	—	60	—	dB
		f = 4kHz	—	60	—	
Commom Mode Rejection Ratio	Gain = 0dB, V_{ripple} = 100mV_{pp}	f = 1kHz	—	50	—	dB
		f = 4kHz	—	50	—	
Gain Error	Gain = 0, 6, 9.56, 15.56, 20, 24, 29.56, 39.9 dB		—	±0.5	—	dB
Input Impedance	Depends on the Gain Setting		1.5	—	24.0	kΩ

5.21 JTAG and Boundary Scan Timing

Table 39. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/3}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns

Table 39. JTAG and Boundary Scan Timing (continued)

Num	Characteristics[1]	Symbol	Min	Max	Unit
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

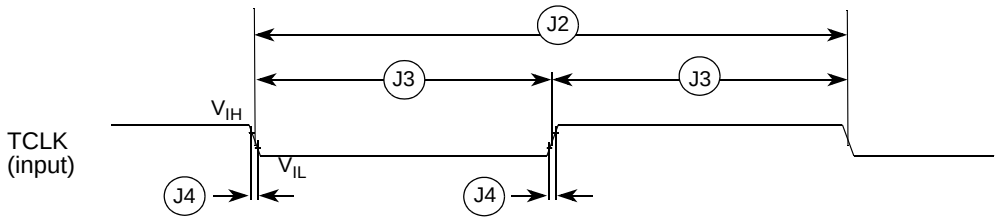


Figure 38. Test Clock Input Timing

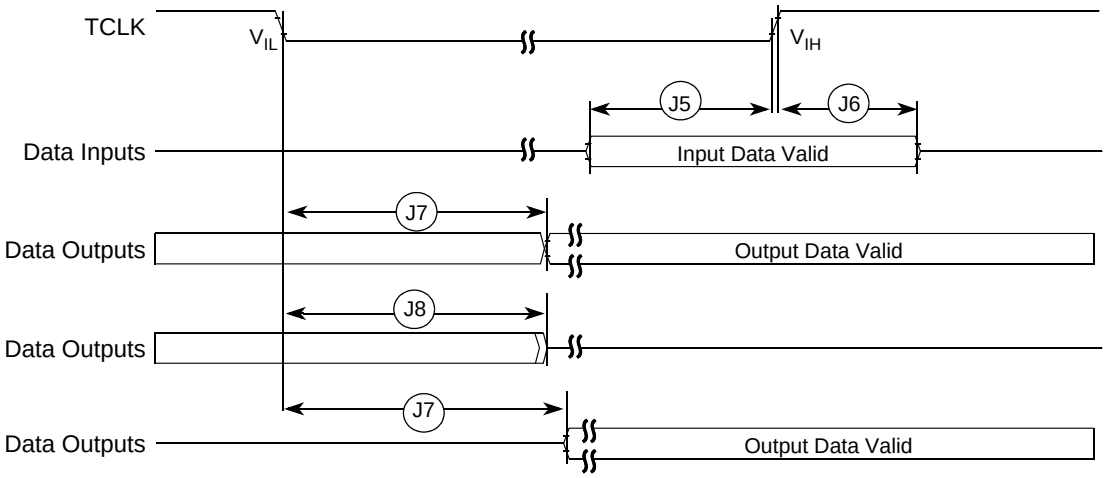


Figure 39. Boundary Scan (JTAG) Timing

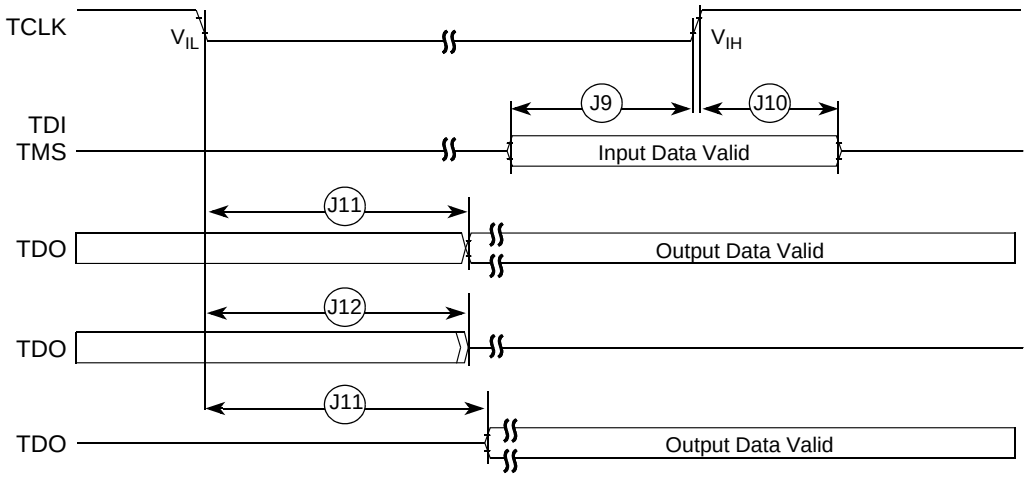


Figure 40. Test Access Port Timing

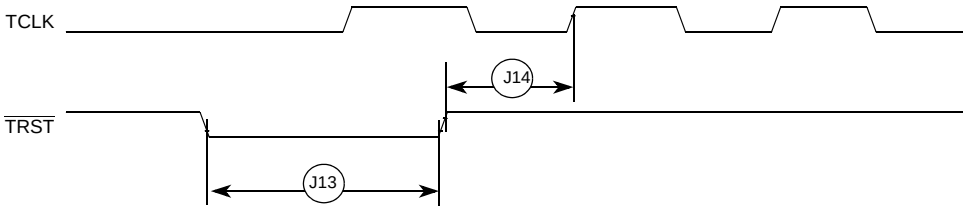


Figure 41. TRST Timing

5.22 Debug AC Timing Specifications

Table 40 lists specifications for the debug AC timing parameters shown in Figure 42.

Table 40. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	1.5	1.5	t_{SYS}
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

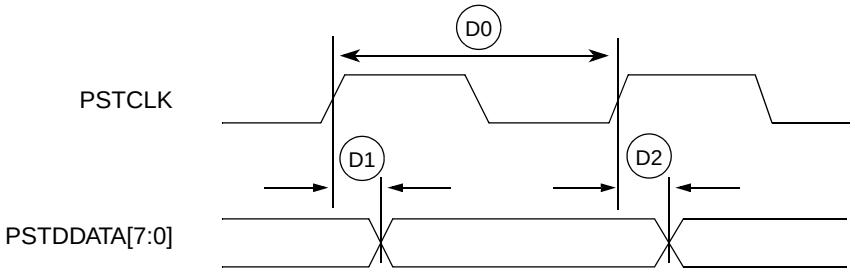


Figure 42. Real-Time Trace AC Timing

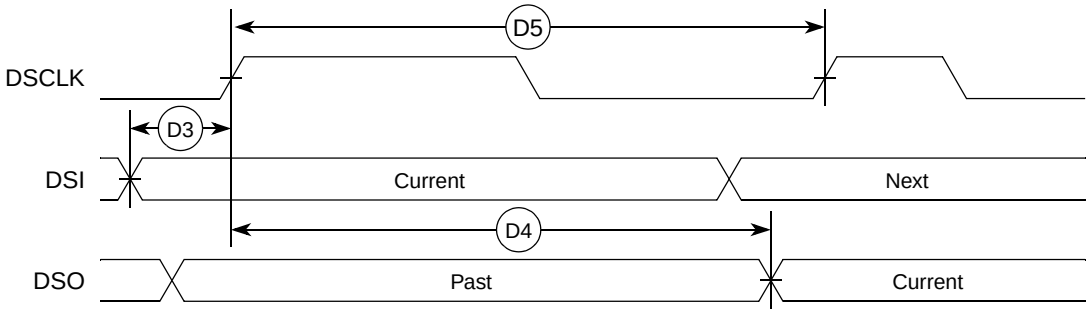


Figure 43. BDM Serial Port AC Timing

6 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/coldfire. The following table lists the package case number per device. Use these numbers in the web page keyword search engine to find the latest package outline drawings.

Table 41. Package Information

Device	Package Type	Case Outline Number
MCF53010	208 LQFP	98ASS23458W
MCF53011		
MCF53012		
MCF53013		
MCF53014	256 MAPBGA	98ARH98219A
MCF53015		
MCF53016		
MCF53017		

7 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.

8 Revision History

Table 42 summarizes revisions to this document.

Table 42. Revision History

Revision	Date	Location	Changes
3	12 Aug 2009	—	Initial public revision
4	10 Feb 2010	Table 8 Table 41	Added thermal characteristics for 208LQFP package Added 208LQFP case outline number
5	3 Mar 2010	Table 2	Added non-J suffixed part numbers for the 256MAPBGA package

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