

NE5517

PIN DESCRIPTION

Pin No.	Symbol	Description
1	I_{ABCa}	Amplifier Bias Input A
2	D_a	Diode Bias A
3	$+IN_a$	Non-inverted Input A
4	$-IN_a$	Inverted Input A
5	VO_a	Output A
6	V_-	Negative Supply
7	$IN_{BUFFERa}$	Buffer Input A
8	$VO_{BUFFERa}$	Buffer Output A
9	$VO_{BUFFERb}$	Buffer Output B
10	$IN_{BUFFERb}$	Buffer Input B
11	V_+	Positive Supply
12	VO_b	Output B
13	$-IN_b$	Inverted Input B
14	$+IN_b$	Non-inverted Input B
15	D_b	Diode Bias B
16	I_{ABCb}	Amplifier Bias Input B

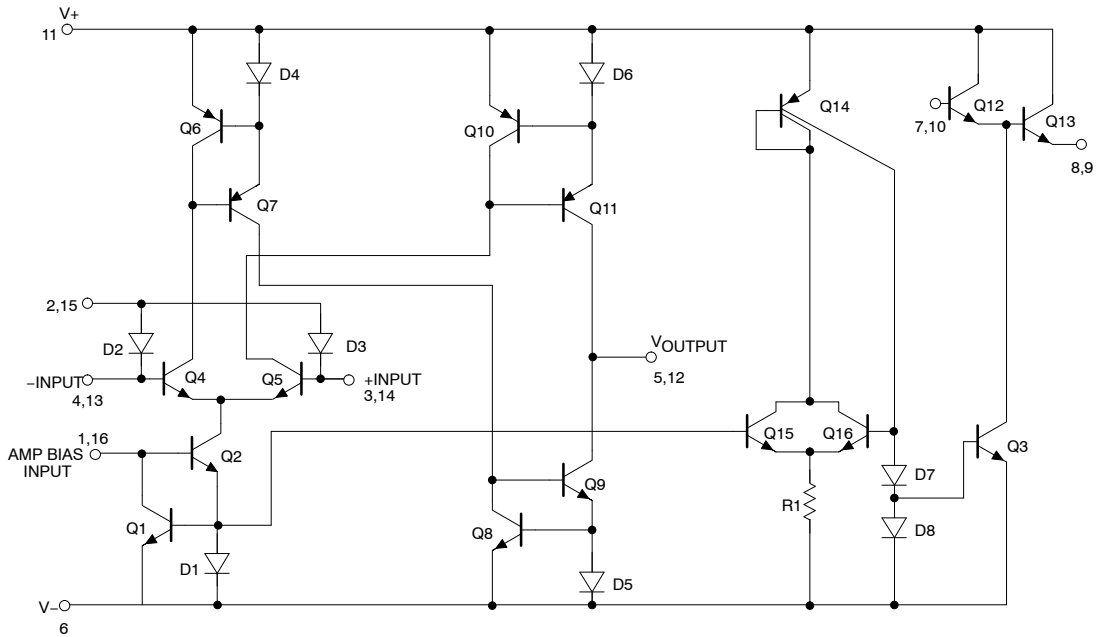
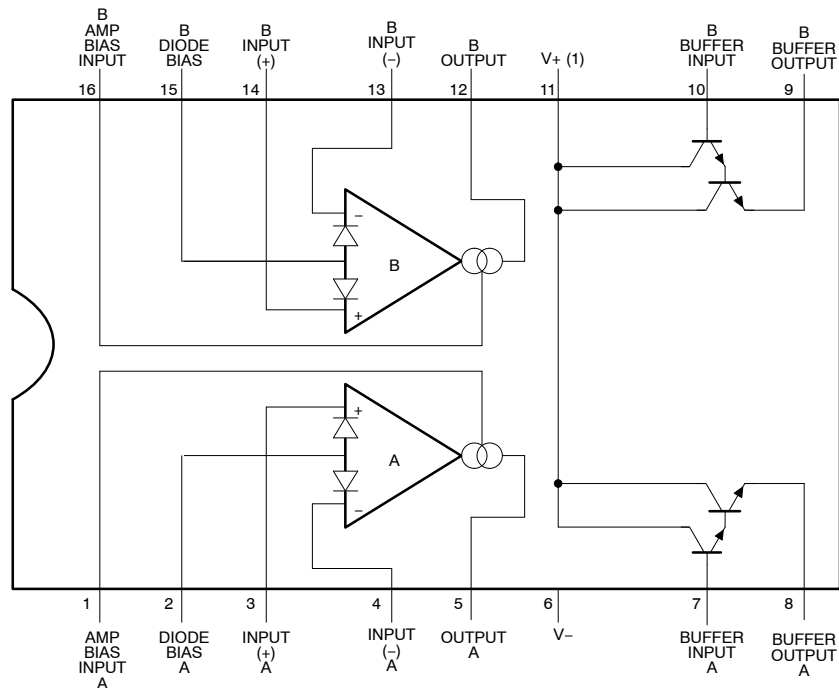


Figure 1. Circuit Schematic

NE5517



NOTE: V_+ of output buffers and amplifiers are internally connected.

Figure 2. Connection Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (Note 1)	V_S	44 V_{DC} or ± 22	V
Power Dissipation, $T_{amb} = 25\text{ }^\circ\text{C}$ (Still Air) (Note 2)	P_D	1125	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	140	$^\circ\text{C}/\text{W}$
Differential Input Voltage	V_{IN}	± 5.0	V
Diode Bias Current	I_D	2.0	mA
Amplifier Bias Current	I_{ABC}	2.0	mA
Output Short-Circuit Duration	I_{SC}	Indefinite	
Buffer Output Current (Note 3)	I_{OUT}	20	mA
Operating Temperature Range	T_{amb}	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$	$^\circ\text{C}$
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
DC Input Voltage	V_{DC}	+ V_S to - V_S	
Storage Temperature Range	T_{stg}	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$	$^\circ\text{C}$
Lead Soldering Temperature (10 sec max)	T_{slid}	230	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- For selections to a supply voltage above $\pm 22\text{ V}$, contact factory.
- The following derating factors should be applied above 25 $^\circ\text{C}$
D package at 7.1 mW/ $^\circ\text{C}$.
- Buffer output current should be limited so as to not exceed package dissipation.

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ELECTRICAL CHARACTERISTICS (Note 4)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	Overtemperature Range $I_{ABC} = 5.0 \mu A$	V_{OS}		0.4 0.3	5.0 5.0	mV
$\Delta V_{OS}/\Delta T$	Avg. TC of Input Offset Voltage			7.0		$\mu V/^{\circ}C$
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 μA			0.5	5	mV
Input Offset Change	$5.0 \mu A \leq I_{ABC} \leq 500 \mu A$	V_{OS}		0.1		mV
Input Offset Current		I_{OS}		0.1	0.6	μA
$\Delta I_{OS}/\Delta T$	Avg. TC of Input Offset Current			0.001		$\mu A/^{\circ}C$
Input Bias Current	Overtemperature Range	I_{BIAS}		0.4 1.0	5.0 8.0	μA
$\Delta I_B/\Delta T$	Avg. TC of Input Current			0.01		$\mu A/^{\circ}C$
Forward Transconductance	Overtemperature Range	g_M	6700 5400	9600	13000	μmho
g_M Tracking				0.3		dB
Peak Output Current	$R_L = 0, I_{ABC} = 5.0 \mu A$ $R_L = 0, I_{ABC} = 500 \mu A$ $R_L = 0, \text{Overtemperature Range}$	I_{OUT}	350 300	5.0 500	650	μA
Peak Output Voltage Positive Negative	$R_L = \infty, 5.0 \mu A \leq I_{ABC} \leq 500 \mu A$ $R_L = \infty, 5.0 \mu A \leq I_{ABC} \leq 500 \mu A$	V_{OUT}	+12 -12	+14.2 -14.4		V
Supply Current	$I_{ABC} = 500 \mu A$, both channels	I_{CC}		2.6	4.0	mA
V_{OS} Sensitivity Positive Negative	$\Delta V_{OS}/\Delta V_+$ $\Delta V_{OS}/\Delta V_-$			20 20	150 150	$\mu V/V$
Common-mode Rejection Ratio		CMRR	80	110		dB
Common-mode Range			± 12	± 13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 kHz			100		dB
Differential Input Current	$I_{ABC} = 0$, Input = ± 4.0 V	I_{IN}		0.02	100	nA
Leakage Current	$I_{ABC} = 0$ (Refer to Test Circuit)			0.2	100	nA
Input Resistance		R_{IN}	10	26		k Ω
Open-loop Bandwidth		B_W		2.0		MHz
Slew Rate	Unity Gain Compensated	SR		50		V/ μs
Buffer Input Current	5	$I_{N_{BUFFER}}$		0.4	5.0	μA
Peak Buffer Output Voltage	5	$V_{O_{BUFFER}}$	10			V
ΔV_{BE} of Buffer	Refer to Buffer V_{BE} Test Circuit (Note 6)			0.5	5.0	mV

4. These specifications apply for $V_S = \pm 15$ V, $T_{amb} = 25^{\circ}C$, amplifier bias current (I_{ABC}) = 500 μA , Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

5. These specifications apply for $V_S = \pm 15$ V, $I_{ABC} = 500 \mu A$, $R_{OUT} = 5.0$ k Ω connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

6. $V_S = \pm 15$, $R_{OUT} = 5.0$ k Ω connected from Buffer output to $-V_S$ and $5.0 \mu A \leq I_{ABC} \leq 500 \mu A$.

TYPICAL PERFORMANCE CHARACTERISTICS

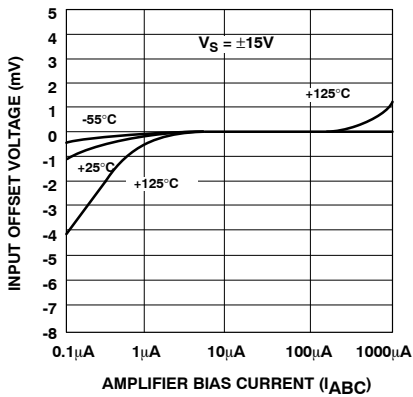


Figure 3. Input Offset Voltage

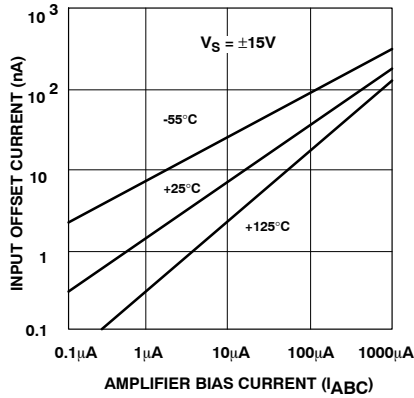


Figure 4. Input Bias Current

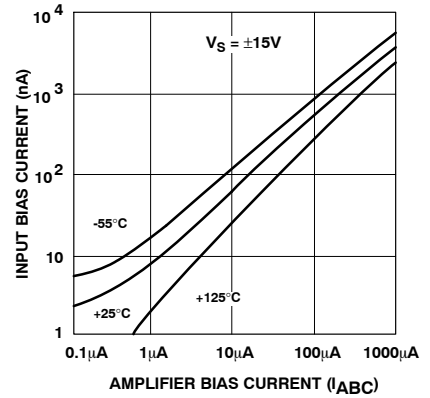


Figure 5. Input Bias Current

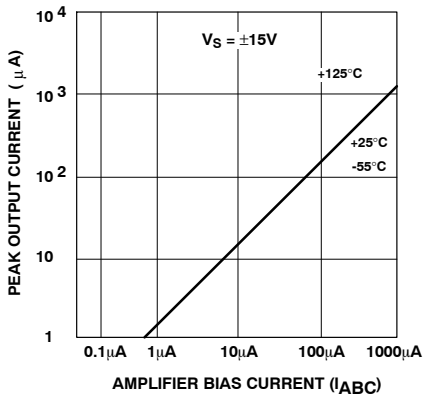


Figure 6. Peak Output Current

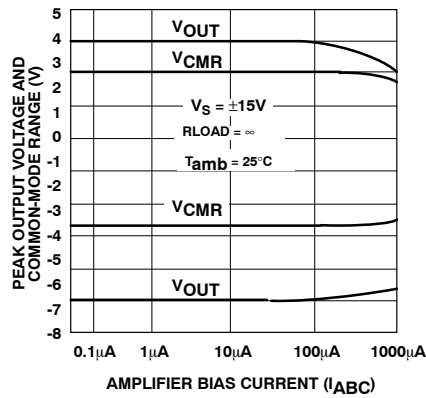


Figure 7. Peak Output Voltage and Common-Mode Range

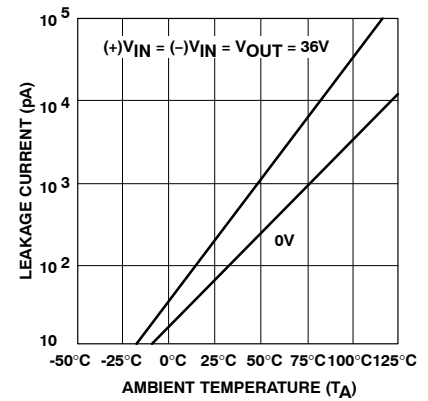


Figure 8. Leakage Current

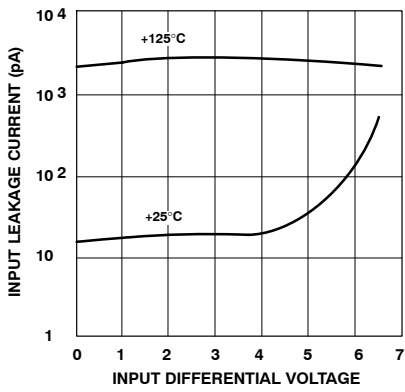


Figure 9. Input Leakage

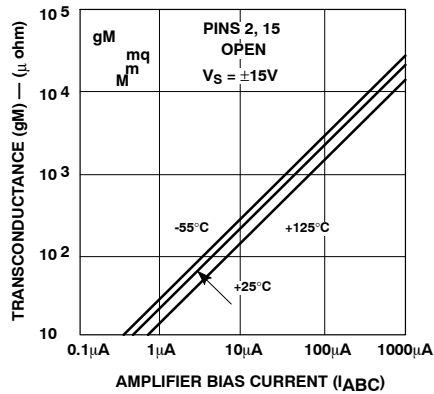


Figure 10. Transconductance

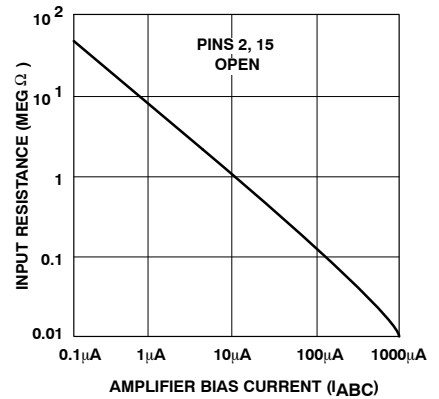


Figure 11. Input Resistance

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

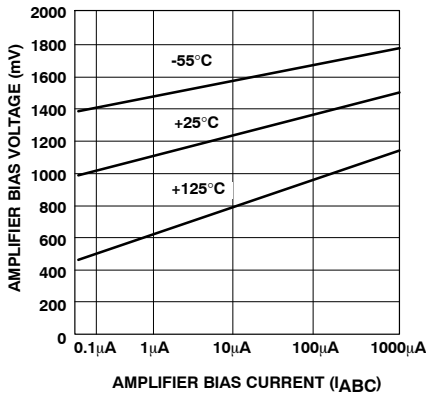


Figure 12. Amplifier Bias Voltage vs. Amplifier Bias Current

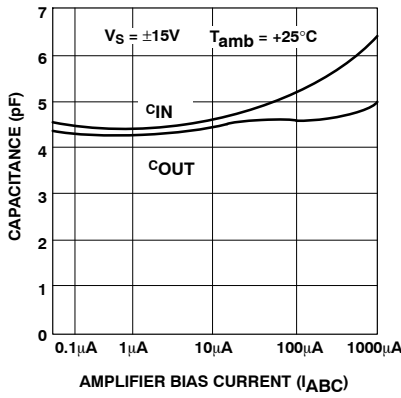


Figure 13. Input and Output Capacitance

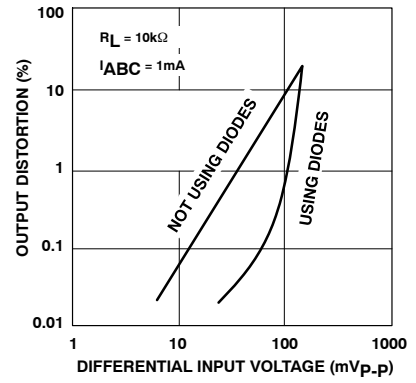


Figure 14. Distortion vs. Differential Input Voltage

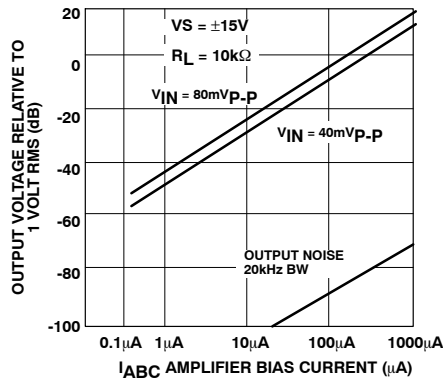


Figure 15. Voltage vs. Amplifier Bias Current

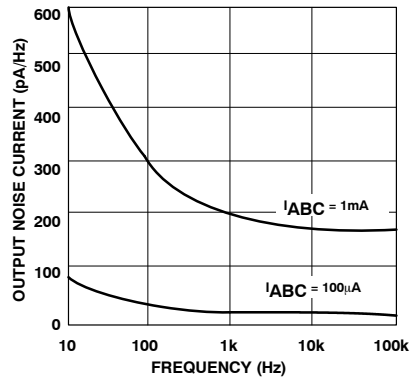


Figure 16. Noise vs. Frequency

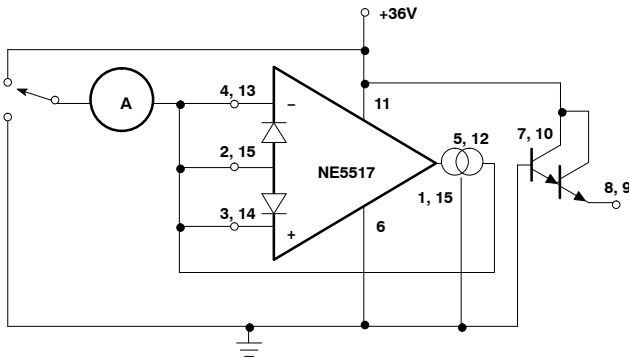


Figure 17. Leakage Current Test Circuit

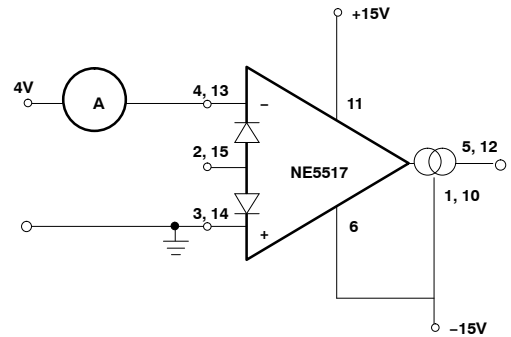


Figure 18. Differential Input Current Test Circuit

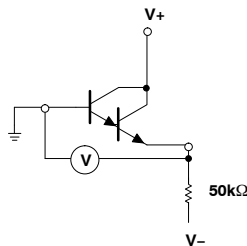


Figure 19. Buffer V_{BE} Test Circuit

APPLICATIONS

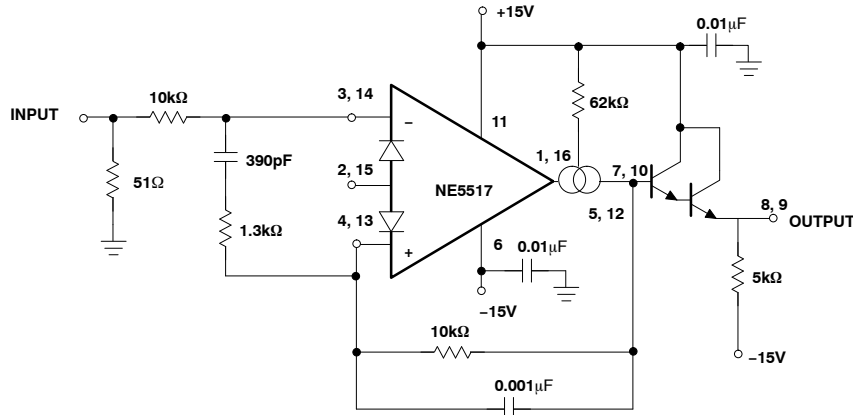


Figure 20. Unity Gain Follower

CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 21.

Transconductance Amplifier

The transistor pair, Q₄ and Q₅, forms a transconductance stage. The ratio of their collector currents (I₄ and I₅, respectively) is defined by the differential input voltage, V_{IN}, which is shown in Equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (\text{eq. 1})$$

Where V_{IN} is the difference of the two input voltages
 KT ≅ 26 mV at room temperature (300°k).

Transistors Q₁, Q₂ and diode D₁ form a current mirror which focuses the sum of current I₄ and I₅ to be equal to amplifier bias current I_B:

$$I_4 + I_5 = I_B \quad (\text{eq. 2})$$

If V_{IN} is small, the ratio of I₅ and I₄ will approach unity and the Taylor series of ln function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \quad (\text{eq. 3})$$

$$\text{and } I_4 \cong I_5 \cong I_B$$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{1/2 I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN} \quad (\text{eq. 4})$$

$$I_5 - I_4 = V_{IN} \frac{(I_B^q)}{2KT}$$

The remaining transistors (Q₆ to Q₁₁) and diodes (D₄ to D₆) form three current mirrors that produce an output current equal to I₅ minus I₄. Thus:

$$V_{IN} \left(\frac{I_B^q}{2KT} \right) = I_O \quad (\text{eq. 5})$$

The term $\frac{(I_B^q)}{2KT}$ is then the transconductance of the amplifier and is proportional to I_B.

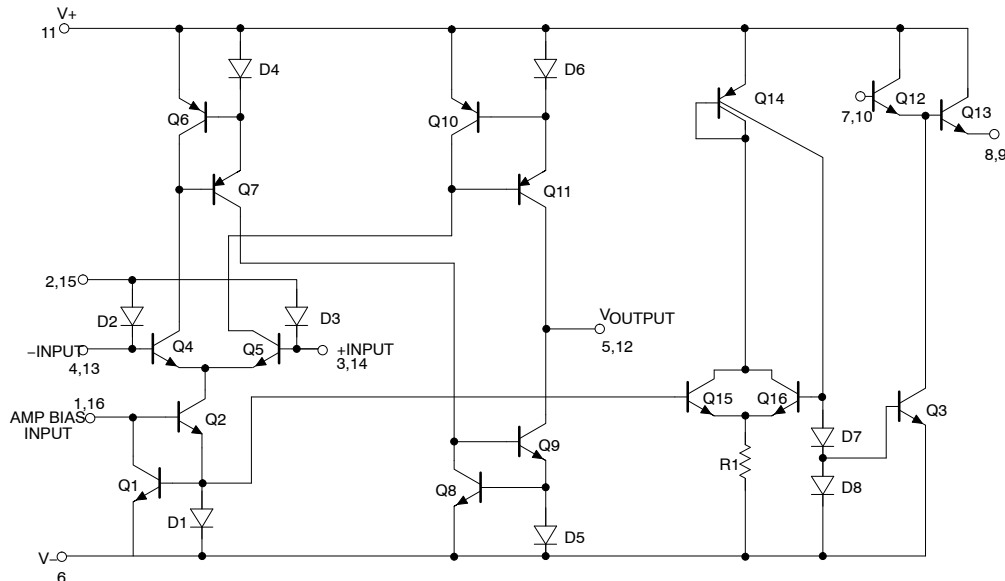


Figure 21. Circuit Diagram of NE5517

Linearizing Diodes

For V_{IN} greater than a few millivolts, Equation 3 becomes invalid and the transconductance increases non-linearly. Figure 22 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D_2 and D_3 are biased with current sources and the input signal current is I_S . Since $I_4 + I_5 = I_B$ and $I_5 - I_4 = I_0$, that is: $I_4 = (I_B - I_0)$, $I_5 = (I_B + I_0)$

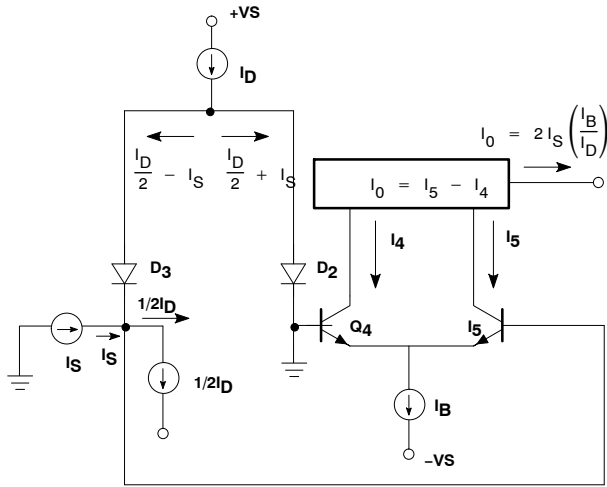


Figure 22. Linearizing Diode

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{T}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{1/2(I_B + I_0)}{1/2(I_B - I_0)} \quad (\text{eq. 6})$$

$$I_0 = I_S \frac{2I_B}{I_D} \text{ for } |I_S| < \frac{I_D}{2}$$

The only limitation is that the signal current should not exceed I_D .

Impedance Buffer

The upper limit of transconductance is defined by the maximum value of I_B (2.0 mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At low values of I_B , a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q_{14} , Q_{15} , Q_{16} , D_7 , D_8 , and R_1) suits the need.

APPLICATIONS

Voltage-Controlled Amplifier

In Figure 23, the voltage divider R_2 , R_3 divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \cdot \frac{R_3}{R_2 + R_3} \cdot g_M$$

$$V_{OUT} = I_{OUT} \cdot R_L$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot g_M \cdot R_L$$

$$(3) g_M = 19.2 I_{ABC}$$

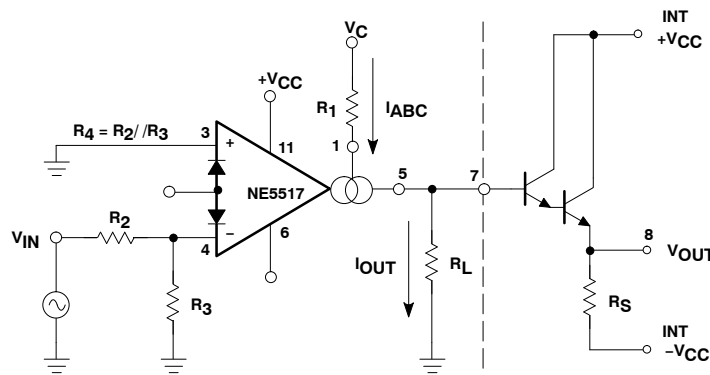
(g_M in μmhos for I_{ABC} in mA)

Since g_M is directly proportional to I_{ABC} , the amplification is controlled by the voltage V_C in a simple way.

When V_C is taken relative to $-V_{CC}$ the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2 V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the NE5517.



TYPICAL VALUES: $R_1 = 47k\Omega$
 $R_2 = 10k\Omega$
 $R_3 = 200\Omega$
 $R_4 = 200\Omega$
 $R_L = 100k\Omega$
 $R_S = 47k\Omega$

Figure 23.

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Stereo Amplifier With Gain Control

Figure 24 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3 dB is easy to achieve. With the potentiometer, R_P , the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510 Ω resistors.

Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to I_{ABC} , the amplification of a signal can be controlled easily. The output current is the product from transconductance \times input voltage. The circuit is effective up to approximately 200 kHz. Modulation of 99% is easy to achieve.

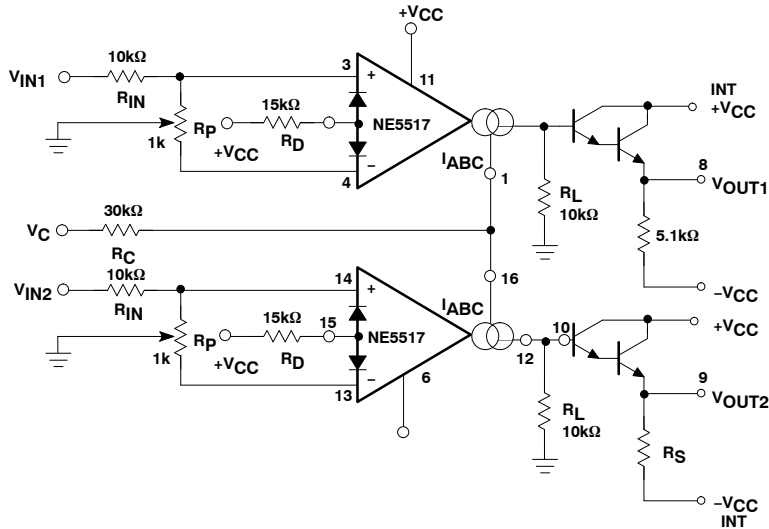


Figure 24. Gain-Controlled Stereo Amplifier

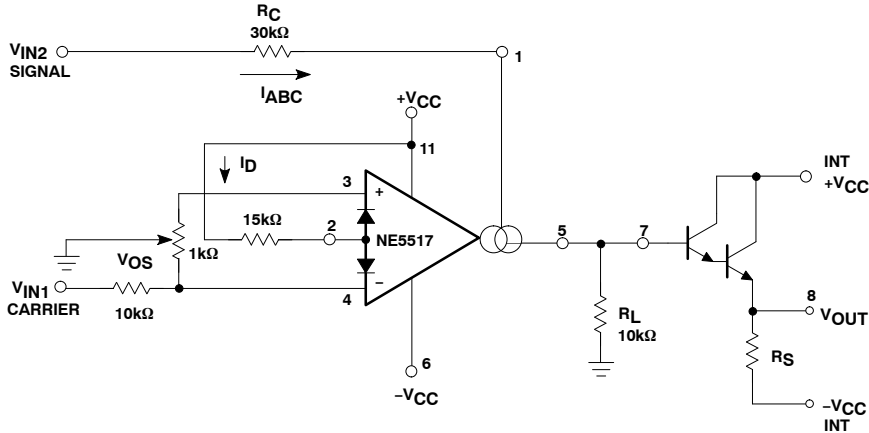


Figure 25. Amplitude Modulator

Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 26 shows how this is done. A voltage presented at the R_X terminals forces a voltage at the input. This voltage is multiplied by g_M and thereby forces a current through the R_X terminals:

$$R_x = \frac{R + R_A}{g_M + R_A}$$

where g_M is approximately 19.21 μ MHOs at room temperature. Figure 27 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

Voltage-Controlled Filters

Figure 28 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until X_C/g_M is equal to R/R_A . Then, the frequency response rolls off at a 6dB per octave with the -3 dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 29. Higher order filters can be made using additional amplifiers as shown in Figures 30 and 31.

Voltage-Controlled Oscillators

Figure 32 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2.0 Hz to 200 kHz is possible by varying I_{ABC} from 1.0 mA to 10 μ A.

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential input voltage is not allowed to be above 5.0 V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 33.

APPLICATION HINTS

To hold the transconductance g_M within the linear range, I_{ABC} should be chosen not greater than 1.0 mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to -2.0 mA. In this application, however, the current range is set through R_{REF} (10 k Ω) to 0 to -1.0 mA.

$$I_{DACMAX} = 2 \cdot \frac{V_{REF}}{R_{REF}} = 2 \cdot \frac{5V}{10k\Omega} = 1mA$$

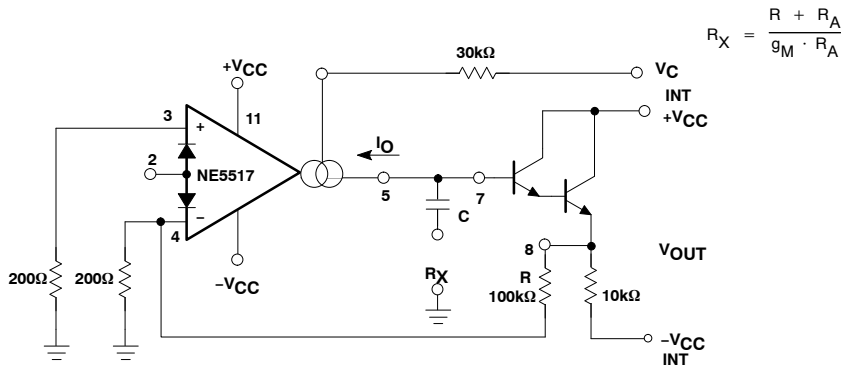


Figure 26. VCR

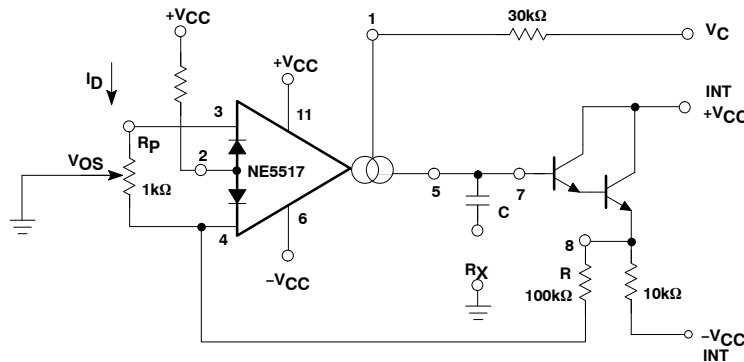
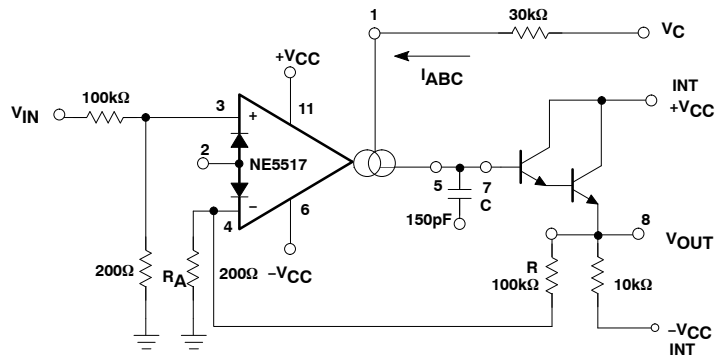


Figure 27. VCR with Linearizing Diodes

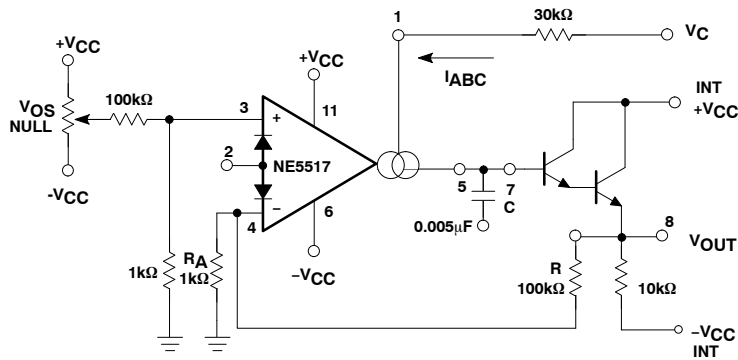
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NOTE:

$$f_O = \frac{R_A g_M}{g(R + R_A) 2\pi C}$$

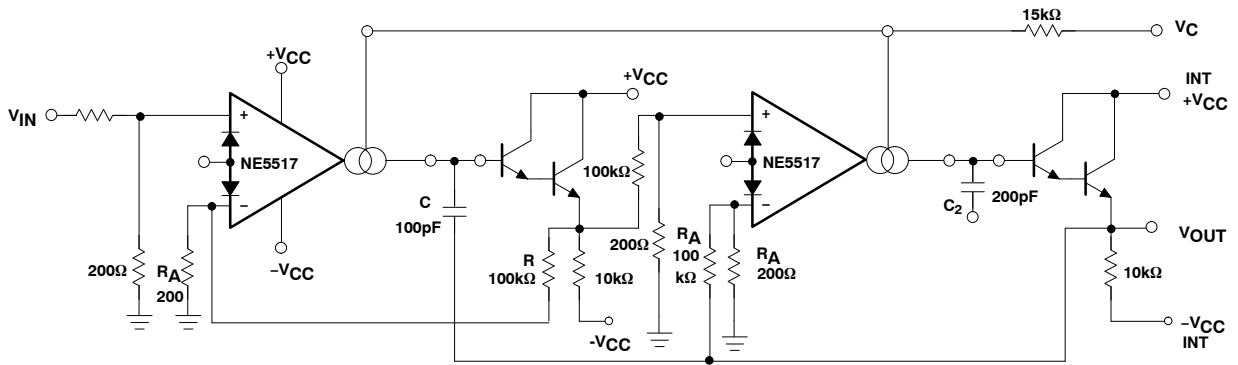
Figure 28. Voltage-Controlled Low-Pass Filter



NOTE:

$$f_O = \frac{R_A g_M}{g(R + R_A) 2\pi C}$$

Figure 29. Voltage-Controlled High-Pass Filter



NOTE:

$$f_O = \frac{R_A g_M}{(R + R_A) 2\pi C}$$

Figure 30. Butterworth Filter - 2nd Order

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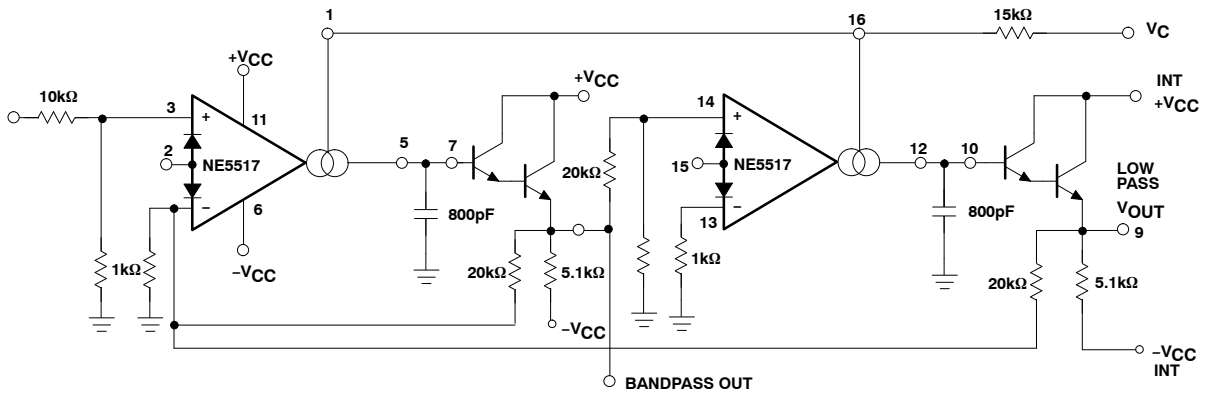


Figure 31. State Variable Filter

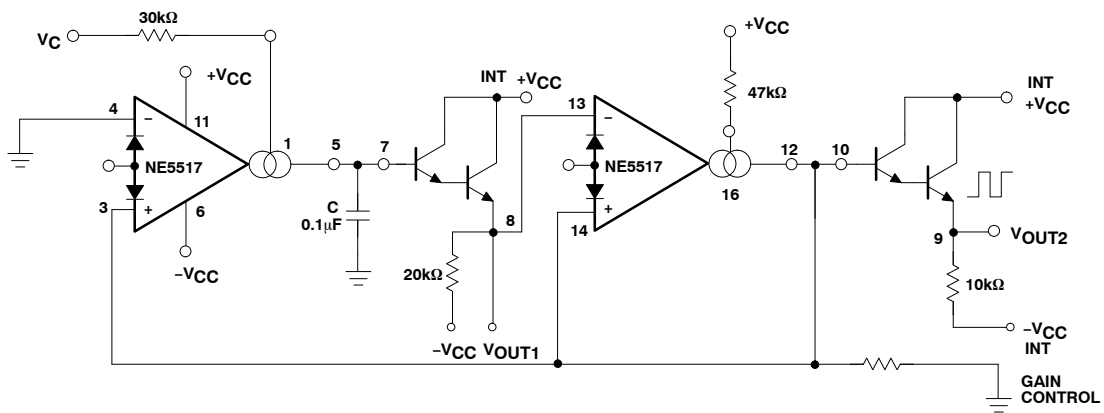


Figure 32. Triangle-Square Wave Generator (VCO)

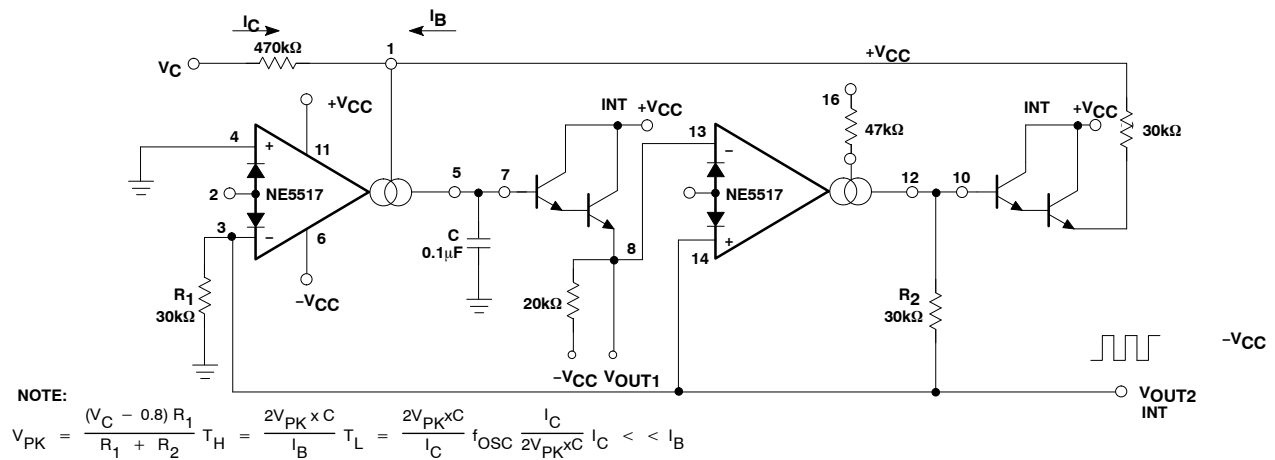


Figure 33. Sawtooth Pulse VCO

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ORDERING INFORMATION

Device	Temperature Range	Package	Shipping†
NE5517DR2G	0 to +70 °C	SOIC-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- | | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> | |

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